NEC

MOS FIELD EFFECT POWER TRANSISTOR
2SK1796

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK1796 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
  $R_{DS(on)} \leqq 1.2\ \Omega$ (V_{GS} = 10 V, I_D = 5 A)
- Low C_{iss} C_{iss} = 2 500 pF TYP.
- Built-in G-S Gate Protection Diode
- High Avalanche Capability Ratings

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

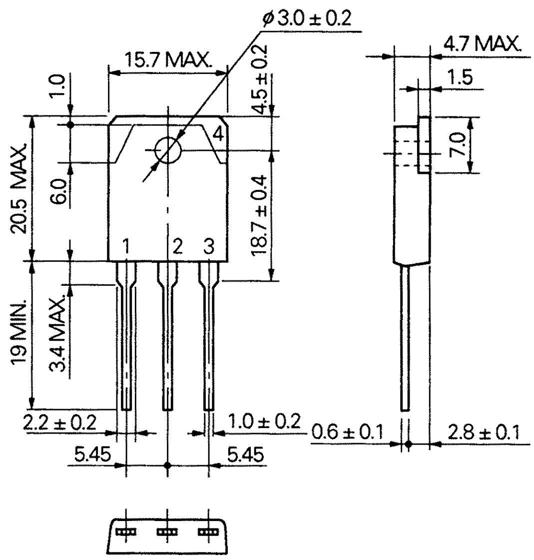
ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Drain to Source Voltage	V_{DSS}	900	V
Gate to Source Voltage	V_{GSS}	±30	V
Drain Current (DC)	$I_{D(DC)}$	±10	A
Drain Current (pulse)	$I_{D(pulse)}$*	±20	A
Total Power Dissipation (T_c = 25 °C)	P_T	150	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C
Single Avalanche Current	I_{AS}**	10	A
Single Avalanche Energy	E_{AS}**	60	mJ

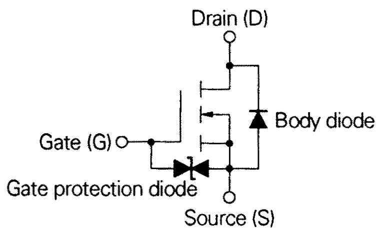
* PW ≦ 10 μs, Duty Cycle ≦ 1 %

** Starting T_{ch} = 25 °C, R_G = 25 Ω, V_{GS} = 20 V → 0

PACKAGE DIMENSIONS
(in millimeters)



1. Gate
2. Drain
3. Source
4. Fin (Drain)

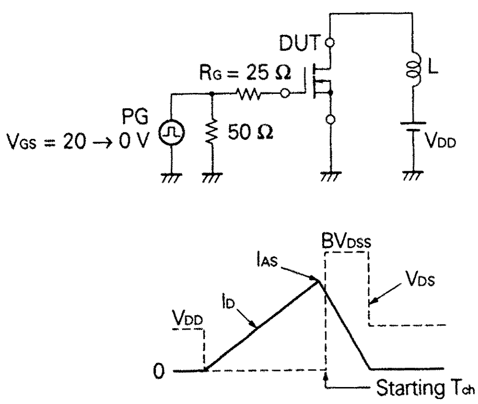


Document No. TC-2442
Date Published August 1993 M
Printed in Japan

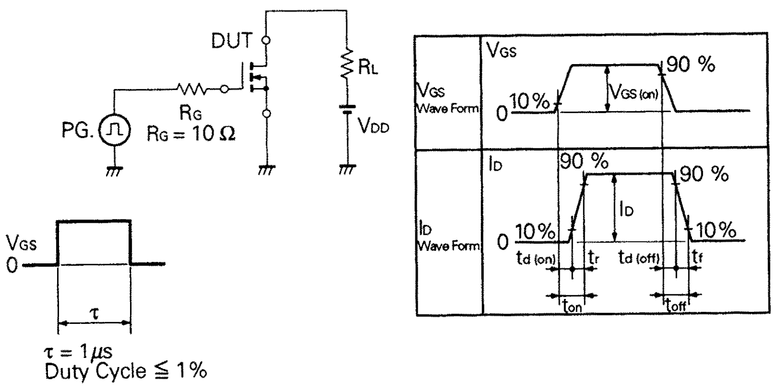
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$		1.0	1.2	Ω	V_{GS} = 10 V, I_D = 5 A
Gate to Source Cutoff Voltage	$V_{GS(off)}$	2.5		3.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance	$\|y_{fs}\|$	1.5	7.5		S	V_{DS} = 20 V, I_D = 5 A
Drain Leakage Current	I_{DSS}			100	μA	V_{DS} = 900 V, V_{GS} = 0
Gate to Source Leakage Current	I_{GSS}			±10	μA	V_{GS} = ±30 V, V_{DS} = 0
Input Capacitance	C_{iss}		2 500		pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
Output Capacitance	C_{oss}		370		pF	
Reverse Transfer Capacitance	C_{rss}		120		pF	
Turn-On Delay Time	$t_{d(on)}$		40		ns	$V_{GS(on)}$ = 10 V V_{DD} = 150 V I_D = 5 A, R_G = 10 Ω R_L = 30 Ω
Rise Time	t_r		50		ns	
Turn-Off Delay Time	$t_{d(off)}$		190		ns	
Fall Time	t_f		40		ns	
Total Gate Charge	Q_G		90		nC	V_{GS} = 10 V I_D = 10 A V_{DD} = 720 V
Gate to Source Charge	Q_{GS}		18		nC	
Gate to Drain Charge	Q_{GD}		38		nC	
Diode Forward Voltage	$V_{F(S-D)}$		0.9		V	I_F = 10 A, V_{GS} = 0
Reverse Recovery Time	t_{rr}		790		ns	I_F = 10 A di/dt = 50 A/μs
Reverse Recovery Charge	Q_{rr}		6.6		μC	

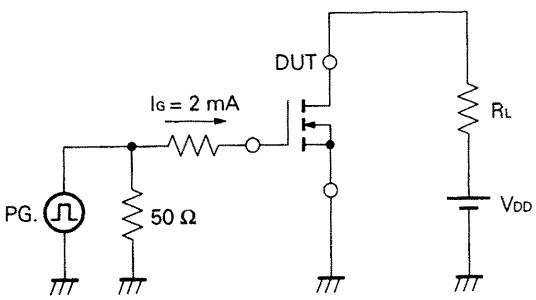
Test Circuit 1: Avalanche Capability



Test Circuit 2: Switching Time

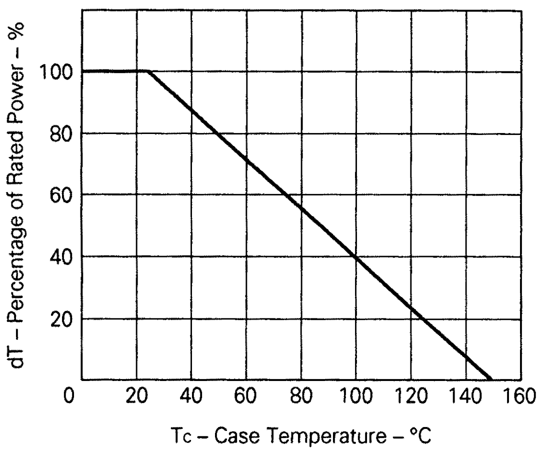


Test Circuit 3: Gate Charge

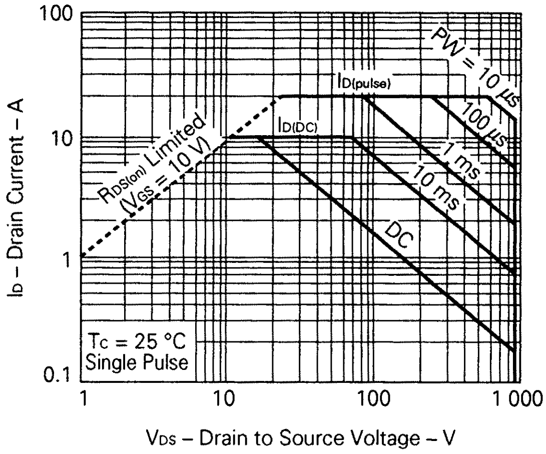


TYPICAL CHARACTERISTICS (Ta = 25 °C)

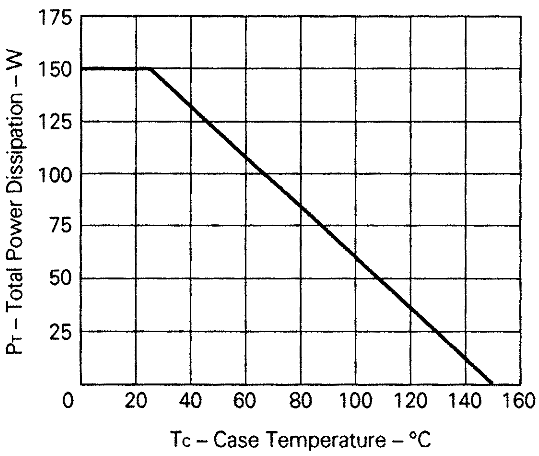
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



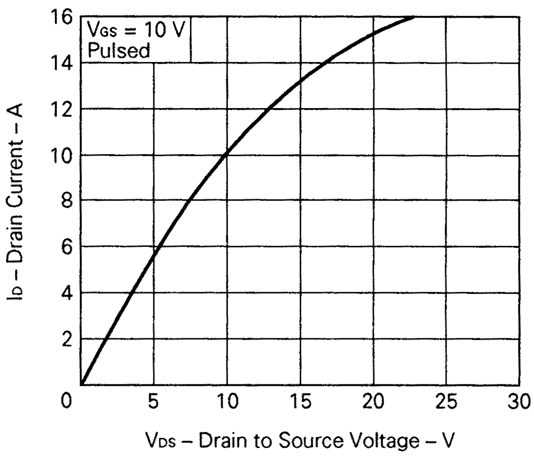
FORWARD BIAS SAFE OPERATING AREA



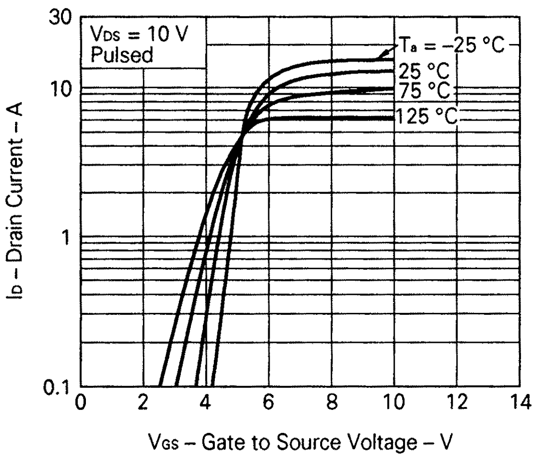
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

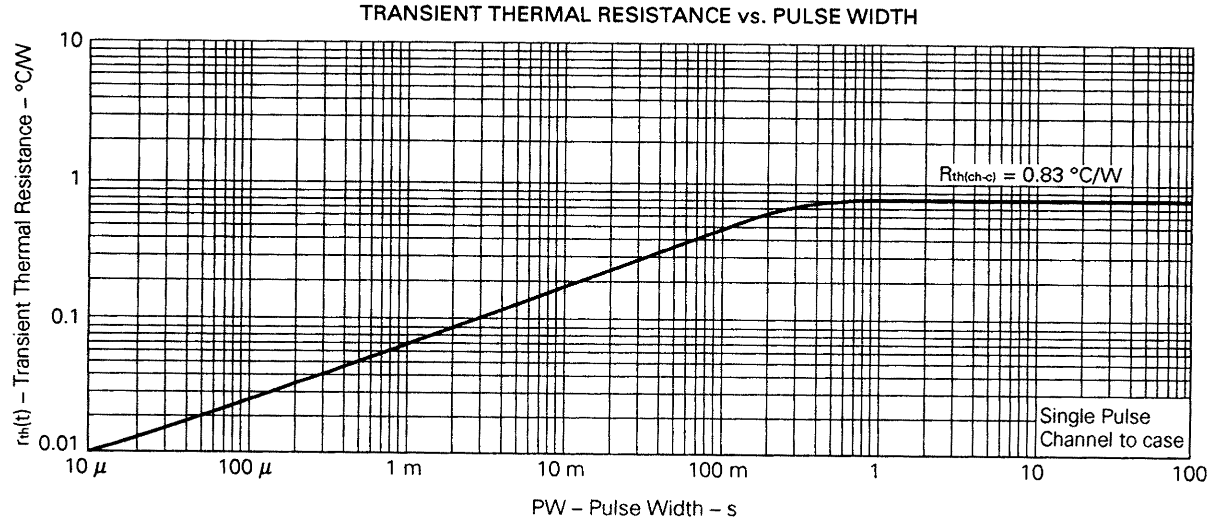


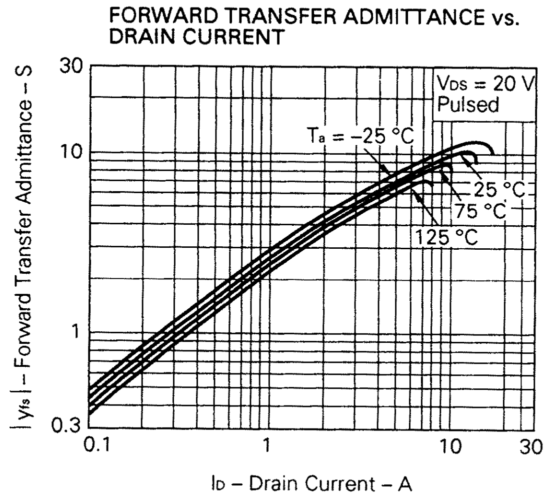
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

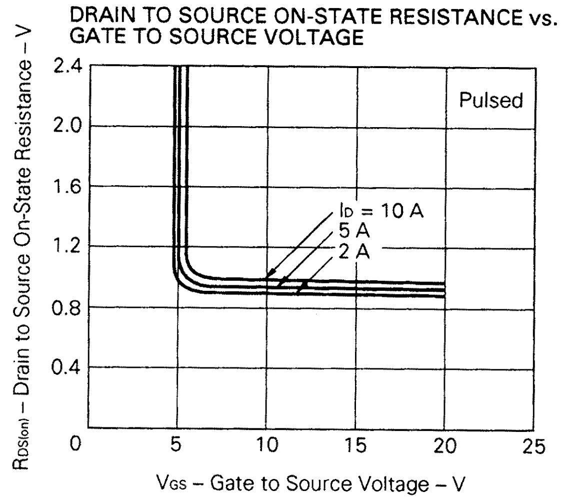


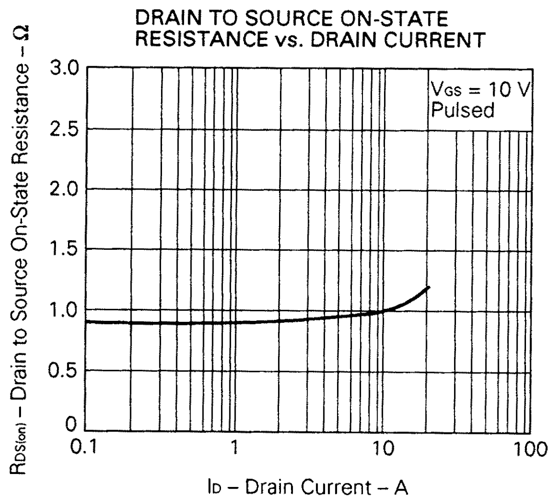
TRANSFER CHARACTERISTICS

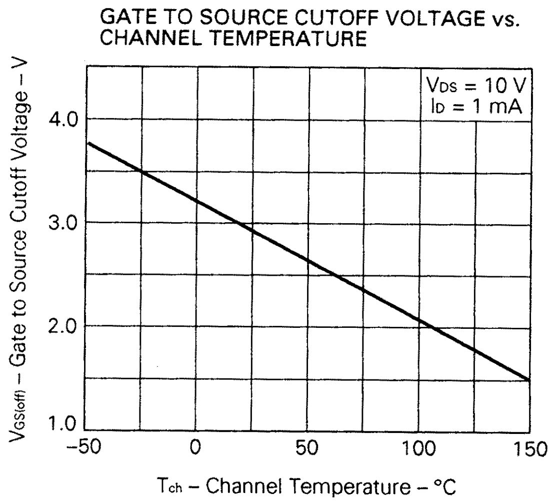



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH
rth(t) – Transient Thermal Resistance – °C/W
10
1
0.1
0.01
Rth(ch-c) = 0.83 °C/W
Single Pulse
Channel to case
10 μ
100 μ
1 m
10 m
100 m
1
10
100
PW – Pulse Width – s

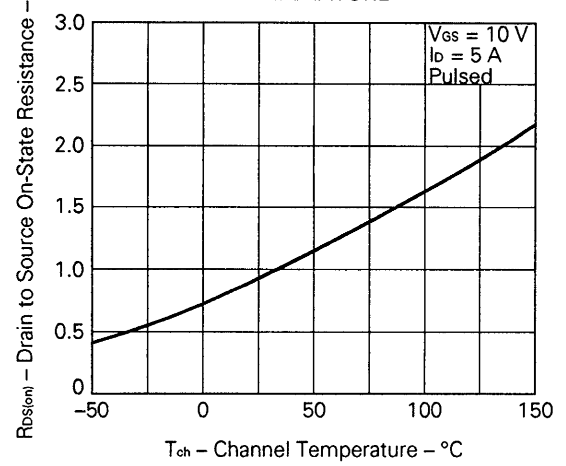

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT
| yfs | – Forward Transfer Admittance – S
30
10
1
0.3
VDS = 20 V
Pulsed
Ta = −25 °C
25 °C
75 °C
125 °C
0.1
1
10
30
ID – Drain Current – A


DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE
RDS(on) – Drain to Source On-State Resistance – V
2.4
2.0
1.6
1.2
0.8
0.4
Pulsed
ID = 10 A
5 A
2 A
0
5
10
15
20
25
VGS – Gate to Source Voltage – V

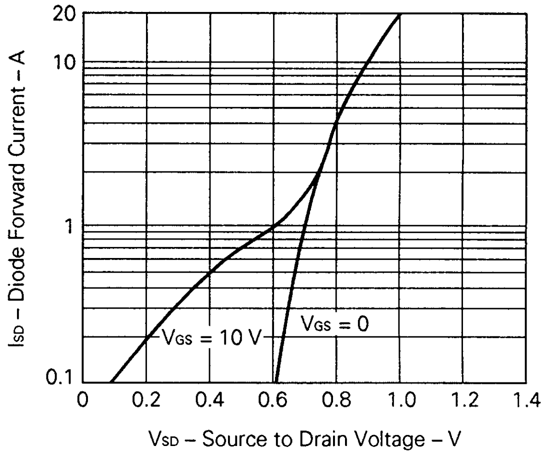

DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT
RDS(on) – Drain to Source On-State Resistance – Ω
3.0
2.5
2.0
1.5
1.0
0.5
0
VGS = 10 V
Pulsed
0.1
1
10
100
ID – Drain Current – A


GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE
VGS(off) – Gate to Source Cutoff Voltage – V
4.0
3.0
2.0
1.0
VDS = 10 V
ID = 1 mA
−50
0
50
100
150
Tch – Channel Temperature – °C

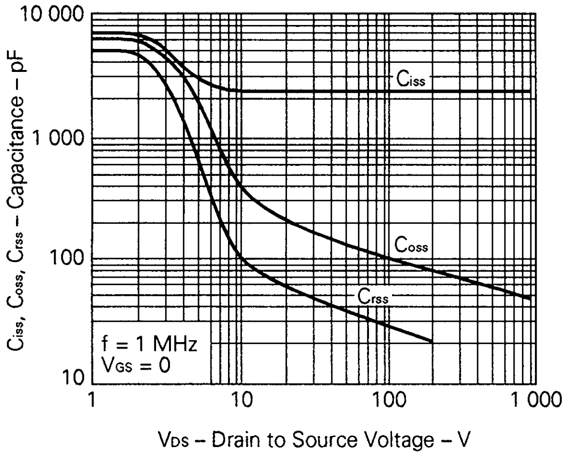
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



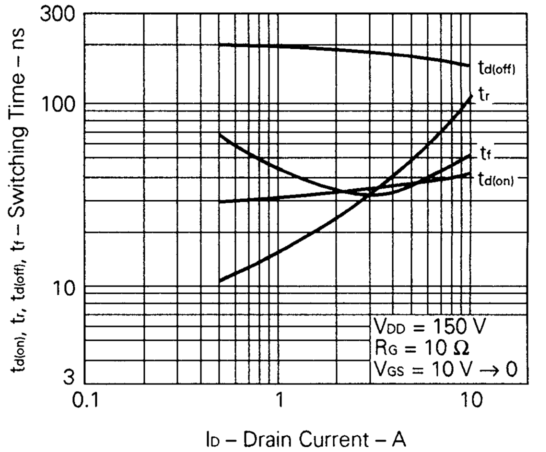
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



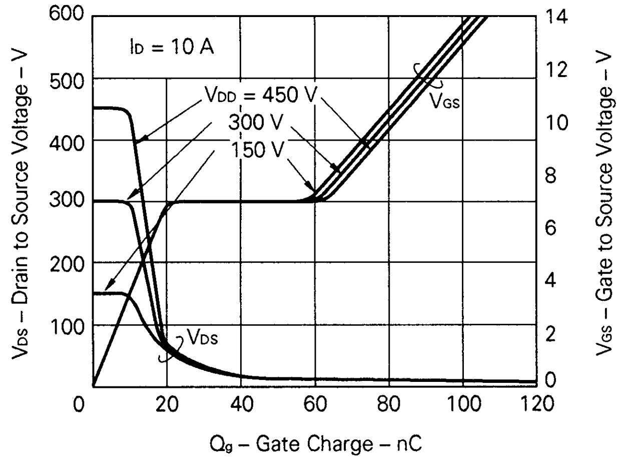
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



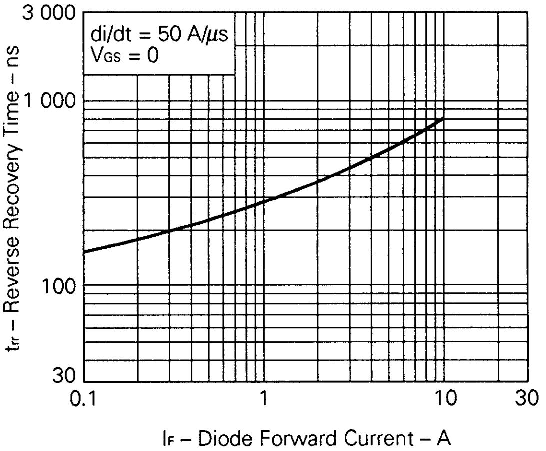
SWITCHING CHARACTERISTICS



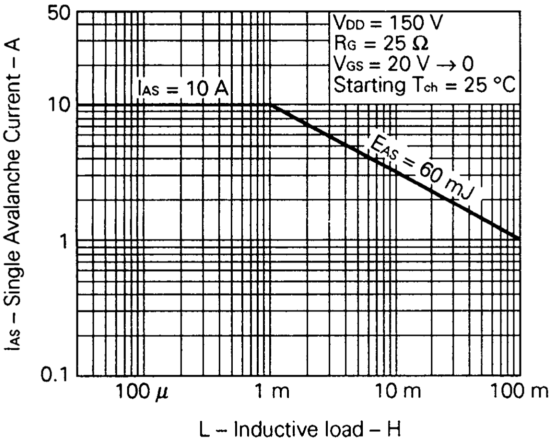
DYNAMIC INPUT CHARACTERISTICS



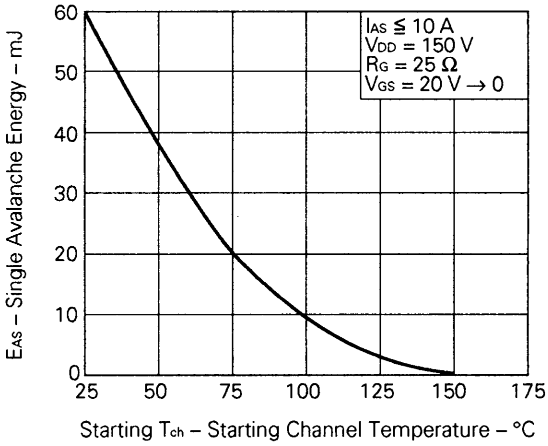
REVERSE RECOVERY TIME vs. REVERSE DRAIN CURRENT



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY vs. STARTING CHANNEL TEMPERATURE



Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

[MEMO]

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