



Programmable FIR Filter

AT76C002

Features

- 16 Multiplier-Accumulators
- 16 Bit Data and 12 Bit Coefficients, 32 Bit Internal Accuracy
- 16 Banks of 12 Bit Coefficients
- 16 Taps at 33 MHz
- Up to 32 Taps for Symmetrical or Interleaved Zeroed Coefficient Filters at 33 MHz
- Up to 63 Taps for Symmetrical Halfband Filters at 33 MHz
- Programmable Decimation by 2, 4, 8 or 16
- Cascadable Keeping Symmetry Advantages
- Output Gain Multiplier
- Programmable Microprocessor Interface
- 208-pin QFP Package

Description

The AT76C002 FIR filter contains 16 multiplier-accumulators which enable it to implement a 16th order non-symmetrical FIR filter or a 32nd order symmetrical FIR filter, operating at 33 MHz. Furthermore, it can be configured to implement a 64th order filter where the even order coefficients are zero, also running at 33 MHz. The incoming samples are 16 bit coded, the coefficients are 12 bit coded and the internal accuracy is 32 bits.

The AT76C002 contains 16 banks of 2 bit coefficients that can be selected in one clock cycle. These banks can also be used to perform decimation by 2, 4, 8 or 16 using FIR filters from 32 taps up to 256 taps. In decimation mode, the symmetry capabilities cannot be used.

In order to implement long FIR filters at the highest frequency (i.e. 33 MHz) the circuit can be cascaded, with no limits except the internal accuracy. Symmetry properties can be used in cascade mode. This halves the number of cascaded circuits to implement symmetrical filters.

In order to increase the accuracy of the intermediate results, the AT76C002 includes an output gain multiplier which enables the whole 12 bit dynamic of the coefficients to be used. Cascadability cannot be used in decimation mode.

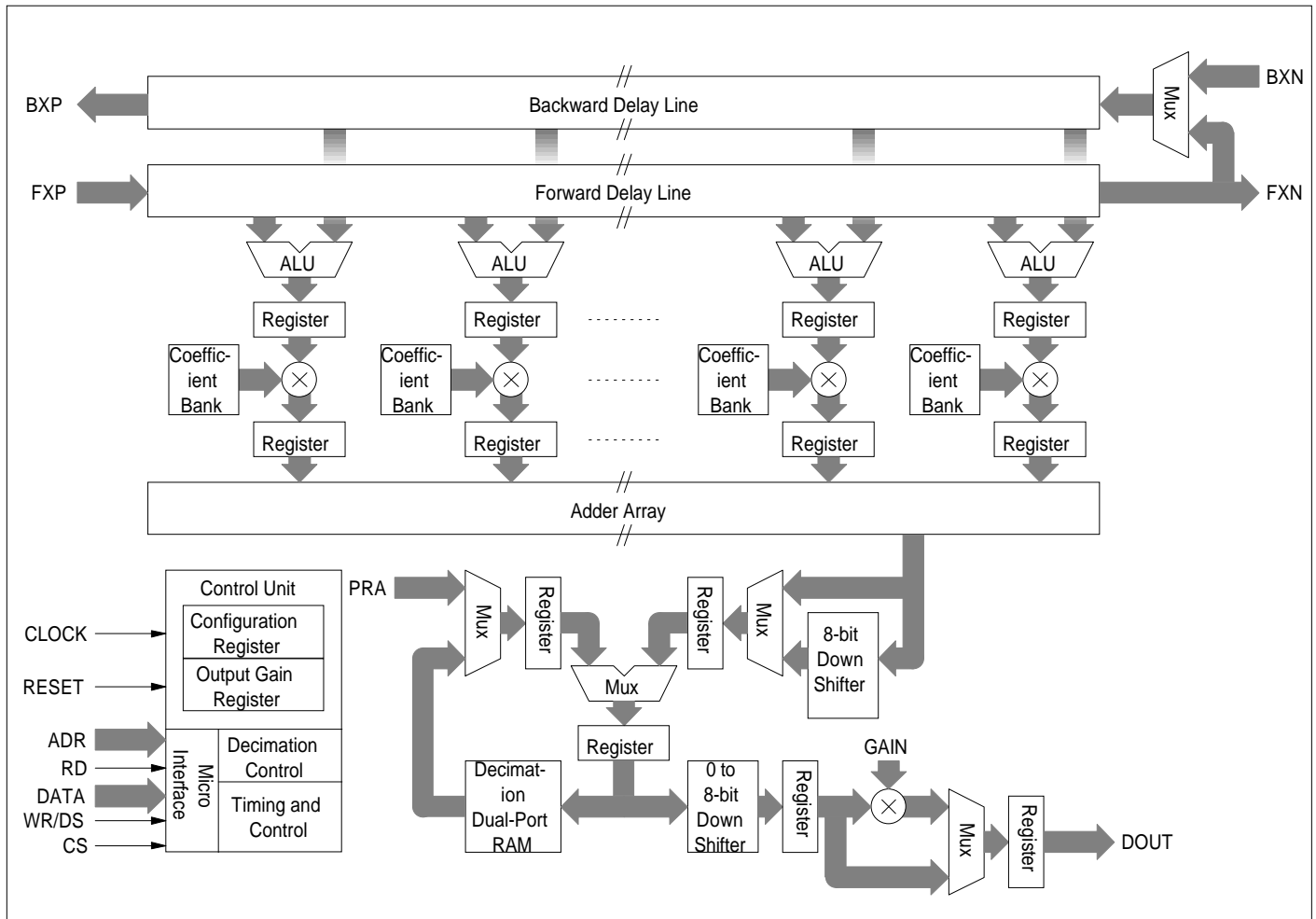
The AT76C002 includes a 16 bit microprocessor interface that can be configured to be Intel or Motorola compatible.

Applications

- High sample rate digital filtering
- Image processing
- Video processing
- Matrix multiplication



Block Diagram



Internal Structure

FIR Structure

The AT76C002 is built around an array of 16 17x12 multiplier-accumulators, a forward and a backward delay line which enable FIR filters of up to 32 taps to be implemented with odd and even symmetry. FIR filters with interleaved zeroed coefficients (such as half-band filters) are handled in an efficient way since a 64 tap half-band symmetrical FIR can be implemented in only one device.

Coefficient Banks

The AT76C002 contains 16 banks of 12 bit coefficients that can be selected by writing to an internal register. The 12 bit coefficients are loaded using the 16 bit microprocessor data bus where the least significant 12 bits are for the coefficient and the most significant 4 bits are for the address within the bank. The bank number is selected by writing to a configuration register.

Decimation

Using these coefficient banks, the AT76C002 can implement decimation filters by 2, 4, 8 or 16, the output rate being 2, 4, 8 or 16 times lower than the input rate. The value of the decimation is programmed in an internal configuration register using the microprocessor interface. Using the SEN Sample Enable input signal, the circuit can handle a variable incoming data rate.

Cascadability

The AT76C002 can be cascaded in order to implement long high-rate FIR filters. Even in a cascaded structure, the AT76C002 can efficiently handle symmetrical and interleaved zeroed coefficient FIR filters, by cascading both forward and backward delay lines. In that way, a 128 tap symmetrical FIR filter or a 256 tap symmetrical half-band FIR filter would only require two cascaded AT76C002 devices.

Pin Description

Name	Function
V _{CC}	Supply voltage
GND	Ground
CLOCK	Clock input
CKEN_SYNC	Synchronous clock enable input
CKEN	Asynchronous clock enable input
RESET	Master reset input
ADR	3 bit microprocessor interface input address bus
DATA	16 bit microprocessor interface bidirectional data bus
RD	Microprocessor interface read input
WR/DS	Microprocessor interface write/data strobe input
CS	Microprocessor interface chip select input
MOTO/ nINTEL	Microprocessor interface configuration selection input
SEN	Sample enable input
FXP	16 bit forward delay line input (for cascadability)
FXN	16 bit forward delay line output (for cascadability)
BXP	16 bit backward delay line output (for cascadability)
BXN	16 bit backward delay line input (for cascadability)
PRA	32 bit intermediate result input bus (for cascadability)
SF	2 bit output configuration input bus
DOUT	32 bit filter output bus
OUT_DEN	Output data valid
ENA0	Least significant 16 bit data out enable (active high)
ENA0_N	Least significant 16 bit data out enable (active low)
ENA1	Most significant 16 bit data out enable (active high)
ENA1_N	Most significant 16 bit data out enable (active low)

Arithmetic Precision

The AT76C002 includes several features to tune the dynamic of the output results. First of all, the 32 bit output of the FIR structure can be divided by 256 (8 bit down shifter), divided by 1 to 256 (0 to 8 bit down shifter), and then bits 23 to 8 of the data can be multiplied by a 10 bit gain. All features are accessible via the microprocessor bus. These features are useful in cascade mode because, in long filters, most of the coefficients are very low compared with the central ones. Consequently, in a cascade chain, for a device which implements a part of the filter with low coefficients, the coefficients can be tuned in order to use as much as possible the whole 12 bit dynamic. The result is then re-tuned before being transmitted to the next device in the cascade chain.

Microprocessor Interface

The AT76C002 contains a 16 bit microprocessor interface which can be configured, using the MOTO/nINTEL input, to have a Motorola or Intel compatible protocol. In Motorola mode, the protocol uses CS (Chip Select), DS (Data Strobe) and RDW (Read/nWrite) signals. In Intel mode, the protocol uses CS (Chip Select), DS/WR (Write) and RDWR (Read) signals.



Electrical Specifications

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Conditions
V _{DD}	DC supply voltage	-0.5	5.5	V	
V _I	DC input voltage	-0.5	V _{DD} + 0.5V	V	or see +-I _{Ik}
V _O	DC output voltage	-0.5	V _{DD} + 0.5V	V	or see +-I _{Ok}
+I _{Ik}	DC input diode current		10	mA	V _I < -0.5V V _I > V _{DD} + 0.5V
+I _{Ok}	DC output diode current		20	mA	V _O < -0.5V V _O > V _{DD} + 0.5V
I _{OLMAX}	Continuous output current		10	mA	Industrial
I _{OHMAX}	Continuous output current		10	mA	Industrial
T _{SH}	Time of outputs shorted		5	sec	
T _A	Temperature range	-40	+85	C	Industrial
T _{SG}	Storage temperature	-65	+150	C	

DC Characteristics

Symbol	Parameter	Min	Max	Unit	Conditions
I _{IH}	Input leakage, no pullup	-1.0	+1.0	μA	V _{IN} = V _{DD} = 5.5V
I _{IL}	Input leakage, no pullup	-1.0	+1.0	μA	V _{IN} = 0 V _{DD} = 5.5V
I _{OZ}	High-impedance output current bi-directional pins	-1.0	+1.0	μA	V _{DD} = 5.5V
V _{IL}	Low level input voltage		30% V _{DD}	V	CMOS inputs and bi-dir
V _{IH}	High level input voltage	70% V _{DD}		V	CMOS inputs and bi-dir
V _{OL}	Low level output voltage		0.5	V	I _{OL} = 5.0 mA
V _{OH}	High level output voltage	V _{DD} - 0.5V		V	I _{OH} = 5.0 mA
C _{IN}	Input capacitance		7	pF	

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V _{DD}	DC supply voltage	4.5	5.0	5.5	V	
V _I	DC input voltage	0	5.0	V _{DD}	V	
V _O	DC output voltage	0	5.0	V _{DD}	V	
T _A	Temperature range	-40		+85	C	Industrial
T _R	Input rise time			15	ns	10% - 90% CMOS
T _F	Input fall time			15	ns	10% - 90% CMOS



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