ANALOG SOLUTIONS™
a subsidiary of Silicon General, Inc.

ZAD2846

16-Bit High-Speed Sampling A/D Converter

T-51-10-16

Applications

- ☐ Medical Imaging Data Acquisition
- ☐ High-Speed Automatic Test
- ☐ Wide Dynamic Range Scientific Instrumentation
- ☐ Professional Audio
- ☐ Multiplexed Data Acquisition

Key Features

- ☐ 2.5 μs A/D Conversion Time
- ☐ 300 kHz Total Throughput
- ☐ Superior Linearity Throughout Signal Range
- ☐ Built-In Ultra-Linear Sample/Hold
- ☐ Sample/Hold Dielectric Absorption < 0.001%
- ☐ Aperture Uncertainty < 50 ps.
- ☐ Dynamic Gain and Offset Correction Capabilities
- ☐ Tri-State Output Latches

Solutions for Data Conversion

Offering a 3.33 microsecond total throughput time and improved linearity and drift, the ZAD2846 sets the performance standard for 16-bit sampling A/D converters. Utilizing the latest IC technology and advanced Analog Solutions' proprietary circuit designs, the ZAD2846 provides significantly enhanced performance at a cost less than many older, slower designs.

The ZAD2846 is the solution to your high-speed 16-bit conversion needs.

General Description

The ZAD2846 is a high-performance, 3.33 microsecond, 16-bit sampling ADC which includes an ultra-linear Sample/Hold and high-speed A/D converter in one compact, fully tested module. The ZAD2846 has been optimized for performance in critical CT and MRI systems, where the dynamic range, accuracy around zero and repeatability are all critical.

Utilizing an advanced Digitally Corrected Sub-Ranging (DCSR) A/D converter approach and a novel Sample/Hold circuit, the ZAD2846 assures 16-bit total performance.

The ZAD2846's excellent long-term drift and temperature stability are accomplished by using specially selected and tested resistor networks in a proprietary DCSR circuit design that reduces the converter's sensitivity to individual component drift.

Description of Converter

The ZAD2846 utilizes a unique three-pass Digitally Corrected Sub-Ranging (DCSR) technique in conjunction with our proven "monobit" D/A converter architecture to provide premium converter performance.

The unit consists of an ultra-linear Sample/Hold, a 6-bit flash to ensure long-term accuracy, and our monobit DAC for reduced sensitivity to resistor drift.

The combination of the three-pass DCSR technique and monobit design DAC provides up to four times more allowance for component variation and drift than older two-pass sub-ranging converters.

This conservative design approach assures that the unit stays within specification over its full temperature range and that long-term drift is minimized.

PERFORMANCE SPECIFICATIONS
ZAD2846 LOW-DISTORTION 16-BIT SAMPLING A/D CONVERTER

	BIPOLAR
ANALOG INPUT	
Voltage Range	±5 V
Input Impedance	100 MΩ//5 pF typical
Input Bias Current	±2 μA max (+10° to 60°C)
Initial Offset Voltage	±5mV max[3]
Stability of Offset Voltage	±100 μV/72 hrs typical

	BIPOLAR
HOLD MODE	
Droop Rate	5 μV/μs max (typically doubles every 10°C)
Dielectric Absorption	±0.001% of input signal voltage change, typical
S/H Feedthrough @ 20 kHz	−96 dB typical, −90 dB max

ACCURACY	
Resolution	16 bits
Quantization Error	±0.5 LSB
Relative Accuracy[1]	±0.003% FSR, max
FSR Factory-Calibrated to	±0.01%[3]
Absolute Accuracy	±0.003% FSR max[2]
Differential Non-Linearity	±0.5 LSB typical, ±0.75 LSB max
Reference Output	+10.000 V, ±20 mV, load = 2 mA max
Noise Bipolar	60 μV RMS max
Missing Codes	No missing codes 10° to 50°C
Harmonic Distortion[7] (±4.5 V input, 20 kHz)	−96 dB, typical −92 dB, minimum

SAMPLE MODE	
Slew Rate	12 V/μs typical
Bandwidth	1 MHz min
Acquisition Time	1.0 μs typical

DIGITAL INPUTS/OUTPUTS (see note 6)	
Logic Levels	LSTTL/CMOS compatible
Data Outputs	16 bits data; Tri-state latch, 4 LS loads
Trigger Input[5]	Negative edge; 0.2 μs pulse width min., 2 μs max.
Trigger Load	2 LSTTL load[6]
Tri-State Control	Logic 1 on HI BYTE EN or LO BYTE EN generates HI impedance
End of Conversion (EOC)	Data valid on EOC high to low transition

STABILITY	
Differential Non-Linearity Temperature Coefficient	±0.5 ppm/°C typical ±1 ppm/°C max
Offset Temperature Coefficient	±20 μV/°C typical, ±80 μV/°C max
Offset Versus Supply	100 μV/1% change in supply, max
Gain Temperature Coefficient	±2 ppm/°C typical ±7 ppm/°C max
Warm-up Time	15 minutes to specified accuracy

POWER REQUIREMENTS	
+15 V ±0.25 V	100 mA typical
−15 V ±0.25 V	100 mA typical
+ 5 V ±0.25 V	100 mA typical

ENVIRONMENTAL & MECHANICAL	
Operating Temperature Range	+10°C to +60°C
Storage Temperature Range	−10°C to +70°C
Relative Humidity	0 to 85%, non-condensing up to 40°C
Shielding	RFI 6 sides, EMI 5 sides

THROUGHPUT	
Throughput Time (ADC and S/H)	3.33 μs max (300 kHz throughput)
A/D Conversion Time	2.2 μsec, typical

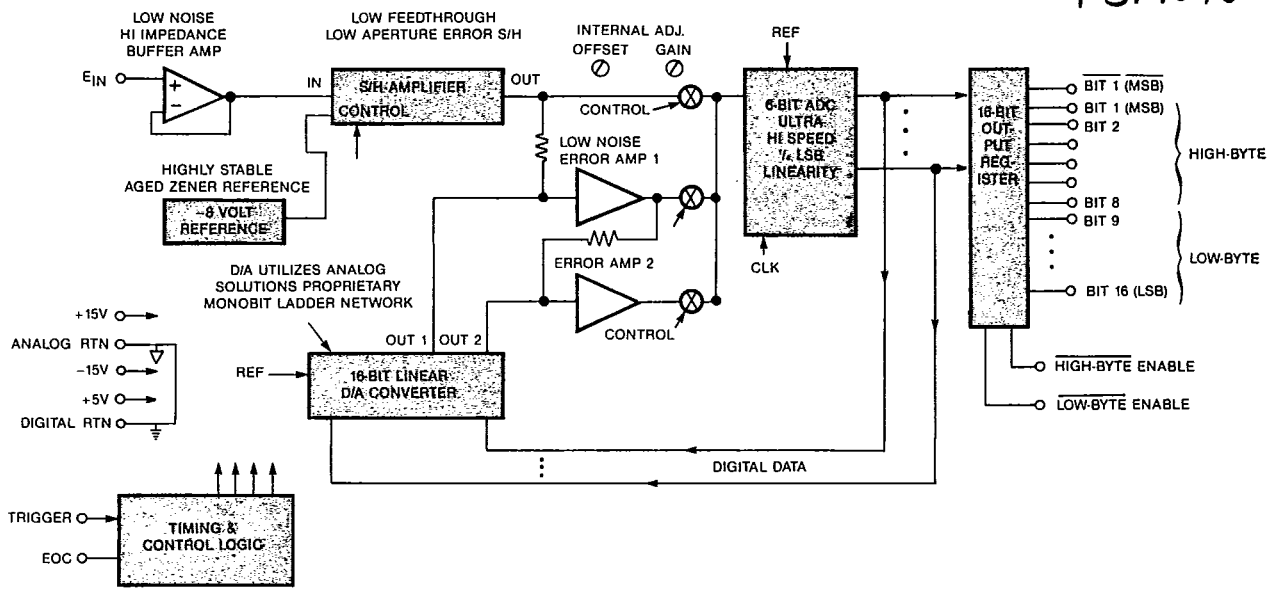
MATING CONNECTOR	
	J1: AMP 10383-7 or equivalent (analog, 16 pin)
	J2: AMP 1-103183-2 or equivalent (digital, 28 pin)

SAMPLE-TO-HOLD SWITCHING	
Aperture Delay	18 ns typical
Aperture Uncertainty	±50 ps typical ±100 ps max

PACKAGE SIZE	
	3.8 in. (96.5mm) × 4.5 in. (114.3mm) × 0.562 in. (14.3mm) max. pkg. height

(Specifications apply @25°C unless otherwise noted)

NOTE:
1. Worst case summation of S/H and A/D non-linearity errors. Best fit straight line.
2. After OFFSET/GAIN adjustment.
3. Internal (or external customer installed) pots allow field calibration.
4. Shaded areas denotes enhanced performance.
5. Internal 10 kΩ pull-up and HC132 gate.
6. Unit contains CMOS devices and should be handled with standard CMOS safety precautions.
7. At 300 kHz sampling rate.



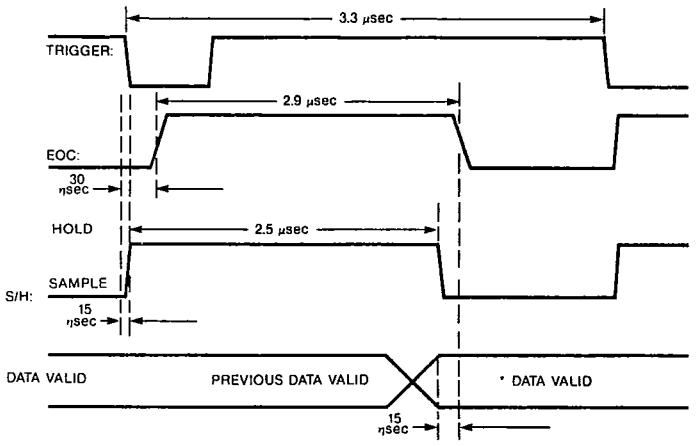
ZAD2846 Three-Pass Digitally Corrected Sub-Ranging (DCSR) Architecture

Sample/Hold Characteristics:

The Sample/Hold is one of the most critical and difficult portions of any data acquisition system.

Through careful design, utilizing unique circuitry, the Sample/Hold section of the ZAD2846 provides true 16-bit linearity, dielectric absorption of 0.001% (< 1 LSB) necessary for accurately acquiring wide dynamic range inputs, and 0.8 microseconds total acquisition and settling time.

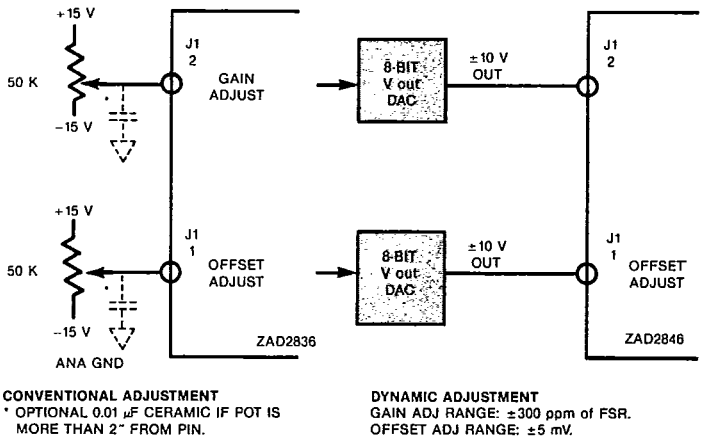
The ZAD2846's Sample/Hold is truly leading the state-of-the-art.



Timing Diagram

Dynamic Adjustment of Gain and Offset:

In addition to internal gain and offset adjustment, provision has been made for the addition of external adjustments. By utilizing these pins and external voltage output D/A's, the gain and offset of the A/D can be dynamically adjusted by the host computer or microcomputer. The available adjustment range for the ZAD2846 has been increased beyond that normally required to enable this dynamic adjustment to handle typical system gain and offset errors.



External Offset and Gain Adjustment

This provides the system designer with the capability to dynamically correct system errors, which results in increased accuracy, system stability and reduced long-term drift.

PC Board Layout

The analog input lead lengths should be as short as possible, preferably surrounded on both sides by an analog ground plane. The module has been carefully laid out internally to separate the analog input from the digital output. This practice should be extended to the PC board as much as possible. All digital control signals should also be kept away from the analog input.

Separate ground planes for analog and digital circuits associated with the ZAD2846 are extremely important. Of equal importance is the use of completely

separate analog and digital ground returns to their respective power supplies. No interconnection of these two returns should occur anywhere in the system except for that which is located within the ZAD2846. In addition, the use of the ANALOG RETURN PIN as an analog ground mecca is recommended. All of these precautions are suggested in order to minimize the effects of ground loops and to eliminate the possibility of digital noise coupling into the analog circuitry.

Power Supplies

In order to take advantage of the full 16-bit accuracy of the ZAD2846, it is recommended that well-regulated linear power supplies be used for the ±15V required by the ZAD2846.

Output Coding

Offset Binary	MSB LSB
+4.99985 V	11.....11
+0.00000 V	10.....00
−5.00000 V	00.....00

Note: For 2's complement coding use the $\overline{\text{MSB}}$ in place of the MSB output.

Additional Products from Analog Solutions

Precision A/D and D/A Converters
Precision 16-bit and 18-bit D/A Converters
High-Performance Sample/Hold Amplifiers
Logarithmic, Isolation and Special-Purpose Amplifiers
High-Speed Telecommunications A/D and D/A Systems
Precision Load Cell and Strain-Gage Sub-Systems
High Speed Industrial Control Interfaces

Custom Products

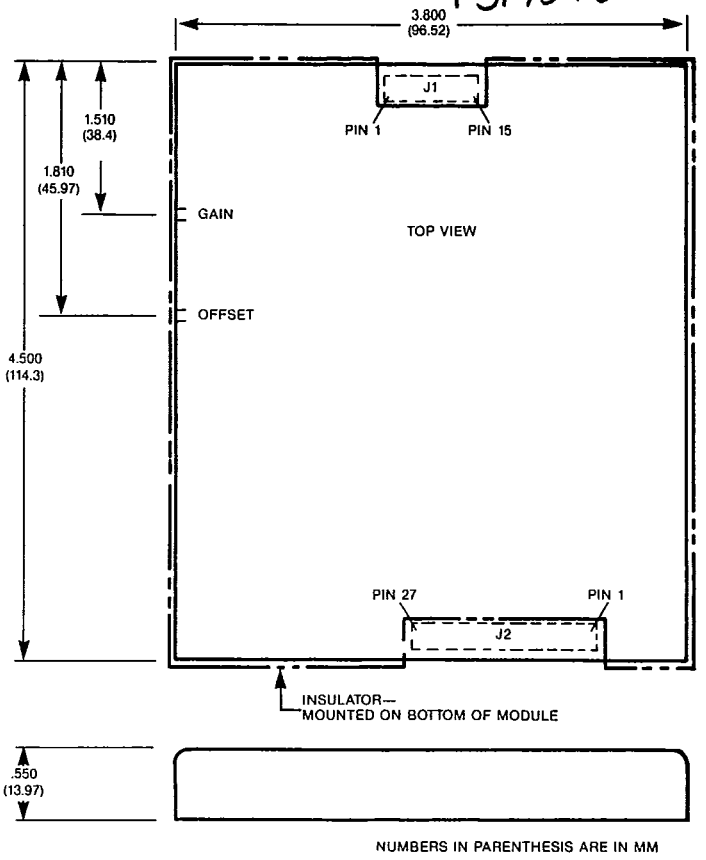
We invite customers to take full advantage of our custom design capability to provide the optimum product solution. Please contact our sales department for further information.

Ordering Guide

To Order Specify: ZAD2846

16-Bit High-Speed Sampling A/D Converter

To place your order, contact Analog Solutions



NUMBERS IN PARENTHESIS ARE IN MM

Contact the factory for mechanical details.

Physical Outline

J1 Pin Assignments

1.	OFFSET ADJ	9.	N/C
2.	GAIN ADJ.	10.	REF OUT
3.	−15 V	11.	S/H OUT
4.	−15V	12.	N/C
5.	ANALOG RTN	13.	SIG. RTN
6.	ANALOG RTN	14.	SIG. RTN
7.	+15 V	15.	SIG. IN
8.	+15 V	16.	SIG. RTN

J2 Pin Assignments

1.	TRIGGER	19.	$\overline{\text{LOW BYTE}}$ ENABLE*
2.	EOC	20.	$\overline{\text{HIGH BYTE}}$ ENABLE*
3.	N/C	21.	BIT 7
4.	N/C	22.	BIT 8
5.	+5 V	23.	BIT 5
6.	+5 V	24.	BIT 6
7.	DIGITAL RTN	25.	BIT 3
8.	DIGITAL RTN	26.	BIT 4
9.	$\overline{\text{BIT 1}}$	27.	BIT 1 MSB
10.	DIGITAL RTN	28.	BIT 2
11.	BIT 15		
12.	BIT 16 LSB		
13.	BIT 13		
14.	BIT 14		
15.	BIT 11		
16.	BIT 12		
17.	BIT 9		
18.	BIT 10		

N/C: Do Not Connect.

SIG RTN, Analog RTN and Digital RTN Internally Connected

* Logic O = Enabled

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Solutions for Data Conversion and Power Management