

MOS DIGITAL INTEGRATED CIRCUIT

μ PD6300C

LATCH and DRIVER for FIP

CMOS LSI

DESCRIPTION

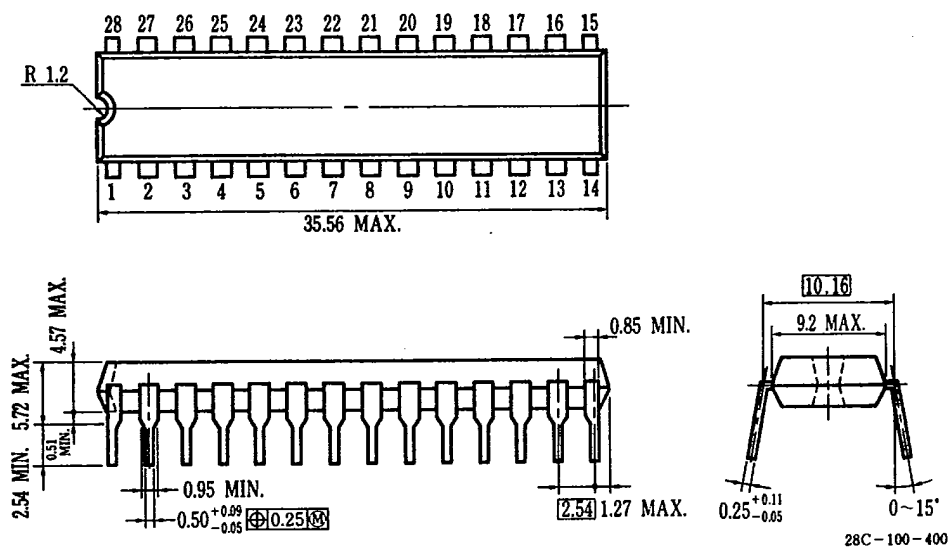
The μ PD6300C is a latch and driver CMOS IC for FIP (Fluorescent Indicator Panel). For multiplex wiring, the μ PD6300C is supplied with the serial interface circuit, 20 bit shift register, 20 bit data latch and 20 bit drivers. The serial data transfer from the data source to the μ PD6300C is accomplished with 3 or 4 signals.

FEATURES

- Serial Input 20 bit Shift Register Incorporated.
- 20 bit Output Data Latch Incorporated.
- 20 bit Output Drivers for FIP.
- Output Characteristics $V_{out} = 40$ V.
 $I_{out} = 5$ mA.
- Serial Interface Format: Compatible with NEC microcomputer.
- Brightness Control Enable: External Duty Control.
- Wide Operating Temperature Range $T_{opt} = -40$ to $+85$ °C.
- 28 PIN Plastic Molded Slim DIP (Dual In line Package).

PACKAGE DIMENSIONS (Unit: mm)

28PIN PLASTIC DIP (400mil)



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage at V _{DD} terminal	V _{DD}	-0.3 to +7.0 *1	V
Input Voltage	V _{IN}	-0.3 to V _{DD} *1	V
Output Voltage (1~7, 15~27 Pins)	V _{O0} to V _{O19}	-35 *1, *2	V
Output Current (1~7, 15~27 Pins)	I _{O0} to I _{O19}	-5	mA
Operating Temperature Range	T _{opt}	-40 to +85	°C
Storage Temperature Range	T _{stg}	-55 to +125	°C

Notes: *1; These Voltage are referenced to the V_{SS}.

*2; V_{DD} = 5 V

RECOMMENDED OPERATING CONDITIONS

	CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
	Operating Temperature Range	T _{opt}	-40		+85	°C
	Operating Supply Voltage	V _{DD}	4.5	5.0	5.5	V
*3	Output Voltage (1~7, 15~27 Pins)	V _{O0} to V _{O19}		-22	-35	V
	Output Current (1~7, 15~27 Pins)	I _{O0} to I _{O19}		-2.0	-5.0	mA
	Input Voltage High	V _{IH}	0.7 V _{DD}		V _{DD}	V
	Input Voltage Low	V _{IL}	V _{SS}		0.3 V _{DD}	V
	SCK Frequency	f _{SCK}			500	kHz
*4	SCK Cycle Time	t _{KCY}	2.0			μs
*4	SCK High Level Pulse Width	t _{KH}	0.9			μs
*4	SCK Low Level Pulse Width	t _{KL}	0.9			μs
*4	SI Setup Time to SCK↓	t _{SIK}	0.4			μs
*4	SI Hold Time	t _{KSI}	0.4			μs
*5	CS↓→SCK↓ Valid Time	t _{CSL}	0			μs
*5	CS↓→SCK↓ Valid Time	t _{CSH}	0.9			μs
*5	SCK→LH↓ Valid Time	t _{SKL}	0			μs
*5	LH Low Level Pulse Width	t _{LL}	1.8			μs
*5	LH↑→CS↑ Valid Time	t _{LHC}	0.9			μs
*6	LH Delay Time	t _{LHD}			1.9	μs

Notes: *3; These Voltage are referenced to the V_{DD}.

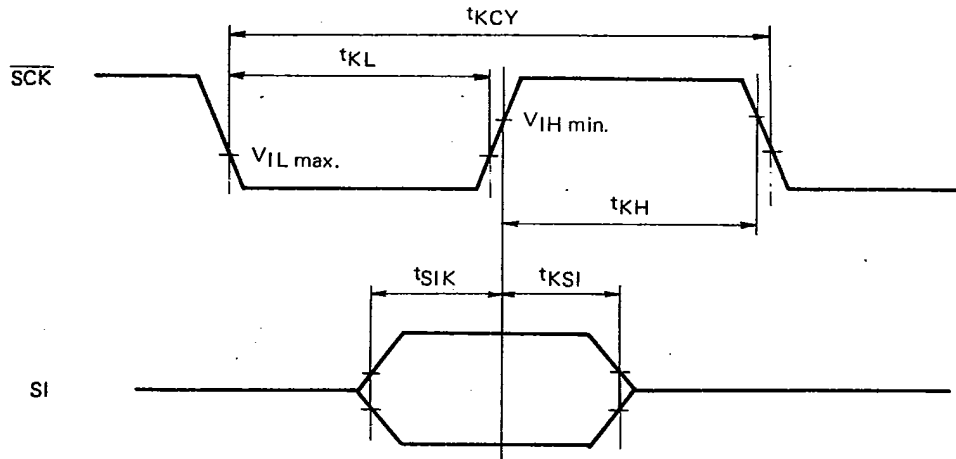
*4; See Fig. 1

*5; See Fig. 2

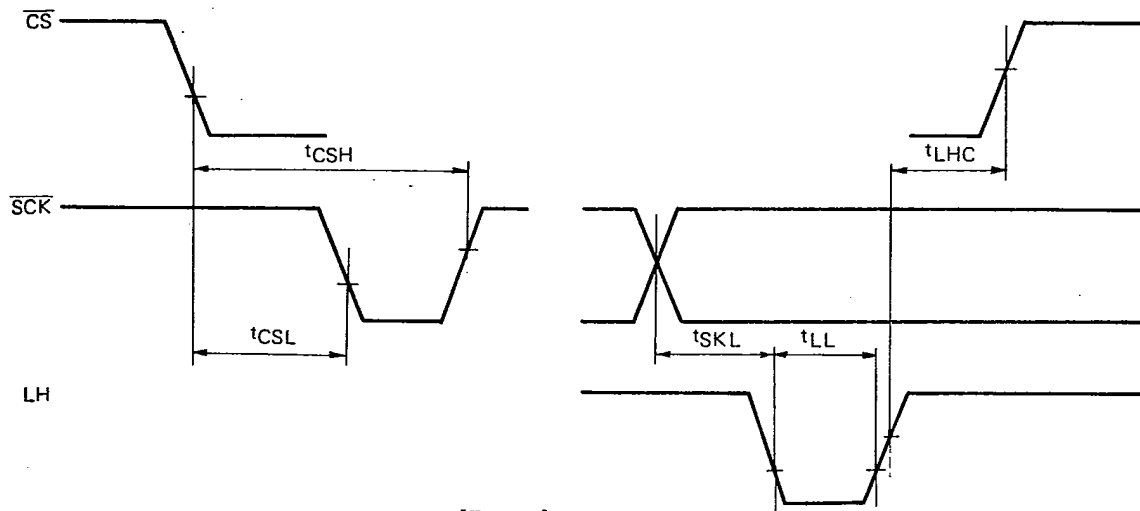
*6; See Fig. 3

ELECTRICAL CHARACTERISTICS (Recommended Operating Conditions)

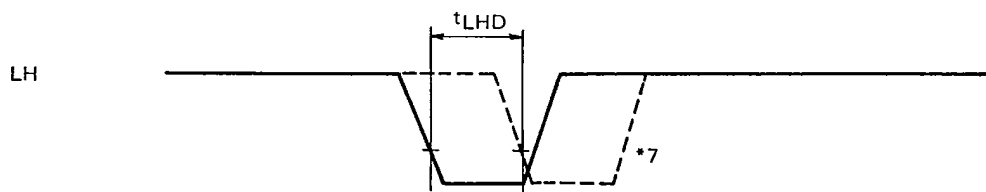
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Leakage Current	I _{IL}			±10	μA	V _{IN} =V _{SS} or V _{DD}
SO Output Voltage High	V _{SOH}	V _{DD} -1			V	I _{SOH} =-1 mA
SO Output Voltage Low	V _{SOL}			0.4	V	I _{SOL} =0.8 mA
Output Voltage High (1~7, 15~27 Pins)	V _O	V _{DD} -15			V	I _O =-5 mA O ₀ to O ₁₉ Output
Output Leakage Current (1~7, 15~27 Pins)	I _{OLL1}			1.0	μA	V _O =-10 V
	I _{OLL2}			10.0	μA	V _O =-20 V
Supply Current at V _{DD} Terminal	I _{DD}			1	mA	V _{DD} =5.5 V All Input = [High] All Output = Open
$\overline{\text{SCK}} \rightarrow \text{SO}$ Valid Time	t _{KSO}			0.5	μs	See Fig. 4
Input Capacitance	C _{IN}			15	pF	f=1 MHz



[Fig. 1]

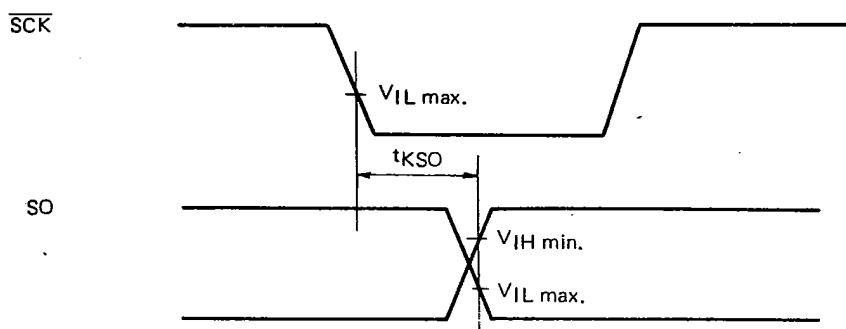


[Fig. 2]



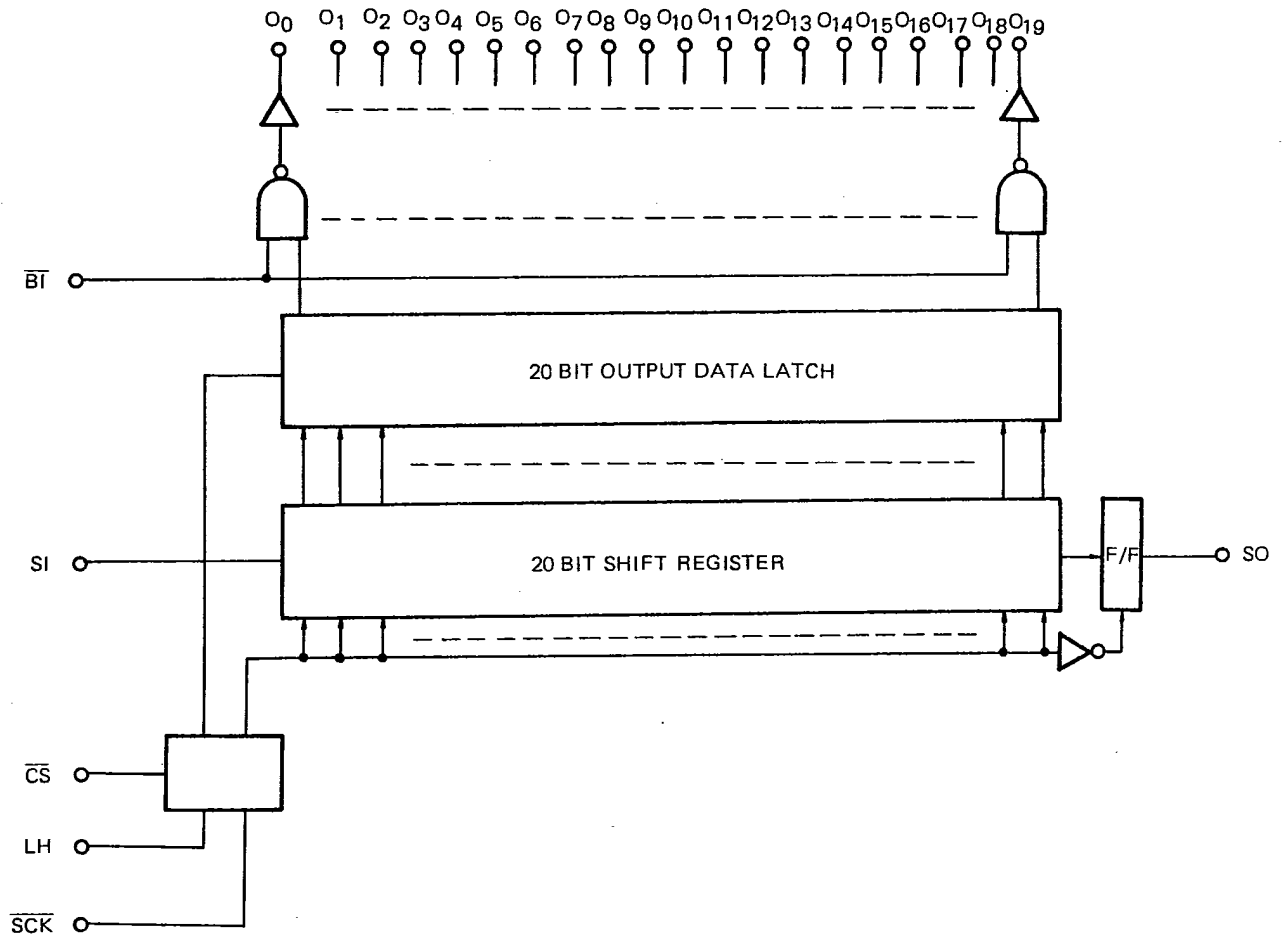
Note: *7; Internal Delay

[Fig. 3]

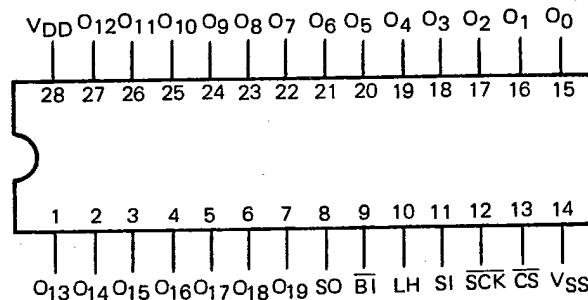


[Fig. 4]

BLOCK DIAGRAM



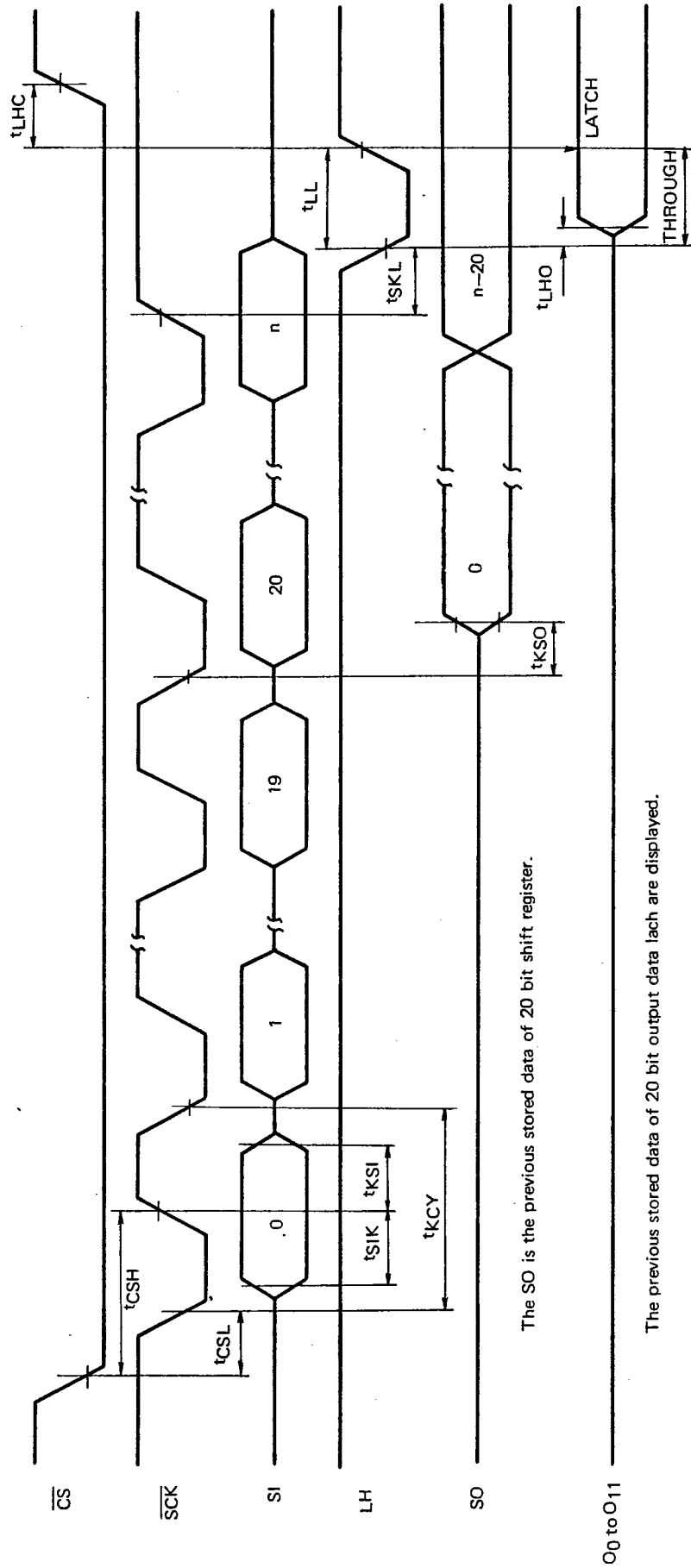
PIN CONNECTION (Top View)



FUNCTION

- $O_0 \sim O_{19}$: Output, P ch MOS Open Drain
These 20 Outputs are the Outputs of 20 bit output data latch and can drive FIP directly.
- \overline{BI} : Blanking Input
When "L" level signal is supplied to the BI, O_0 to O_{19} are disable.
"H" : O_0 to O_{19} are active.
- LH : Latch and Hold Input
When "L" level signal is supplied to the LH,
The data of 20 bit shift register are normally transfered the 20 bit output data latch.
At the time of the rising edge of LH; the data of 20 bit output data latch are hold.
"H" ; The data of 20 bit output data latch are protected.
- SI : Serial Data Input
- \overline{SCK} : Serial Clock Input
The SI data are read and stored in the 20 bit shift register at the rising edge of \overline{SCK} .
- SO : Serial Data Output. CMOS push-pull
The SO is a signal of serial output data from 20 bit sift register.
- \overline{CS} : Chip Select Input
When the CS is "L" level, the LH and \overline{SCK} are active.

TIMING CHART

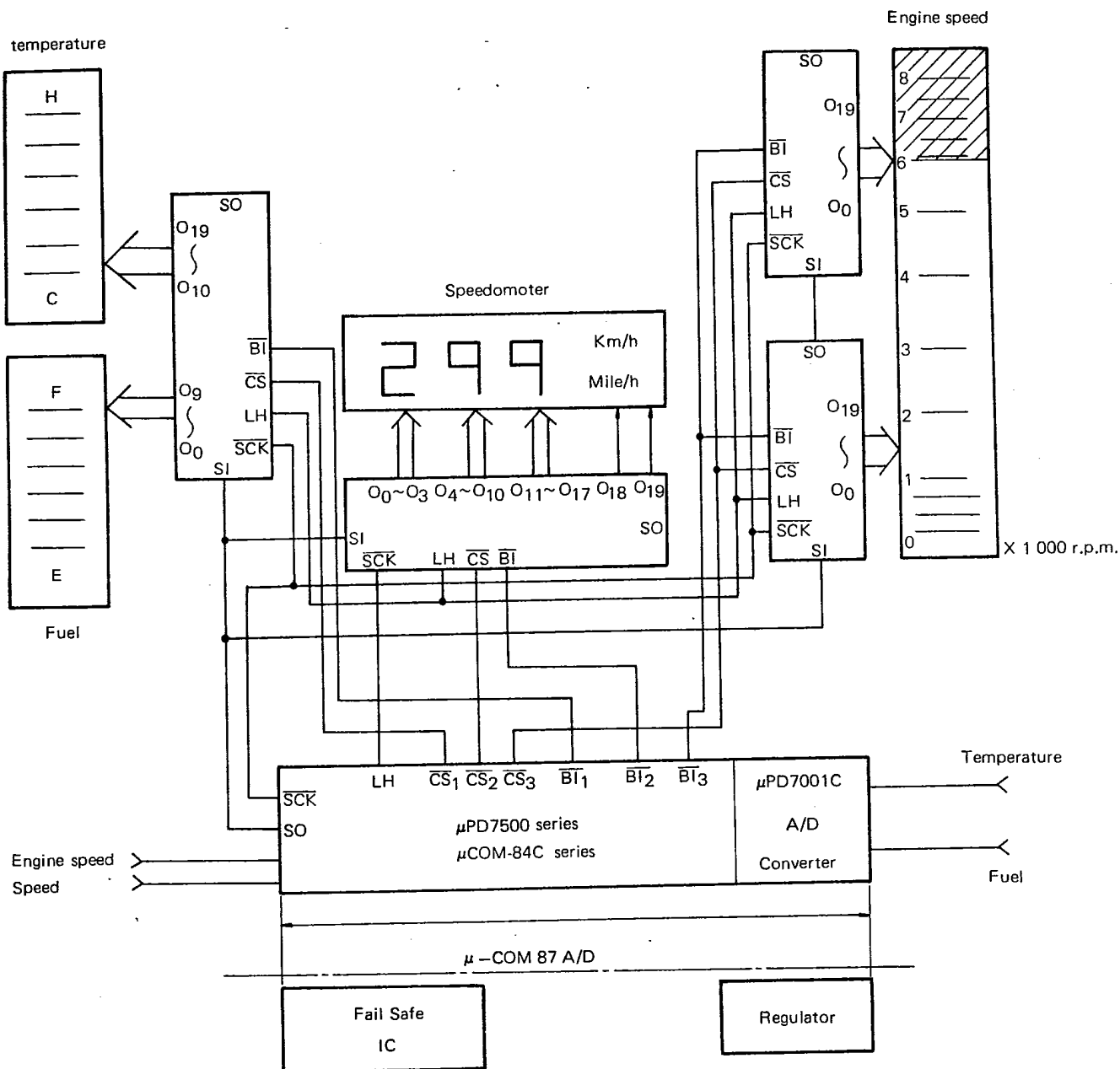


The SO is the previous stored data of 20 bit shift register.

The previous stored data of 20 bit output data latch are displayed.

APPLICATION CIRCUIT

AUTOMOTIVE DASHBOARD SYSTEM



EXAMPLE OF SOFTWARE

Using of serial I/O of μ -COM75 series

Subroutine of 24 bit data transfer

SI OUT : ANP 6, 0BH

: LH LI 05H

LOOP : LAM HL

TAMSIO

SIO

SKI 2

JCP \$-2

DLS

JCP LOOP

ANP 6, 7

ORP 6, 8

ORP 6, 4

RT

RAM (ADD)				
	3	2	1	0
00H	O3	O2	O1	O0
01H	O7	O6	O5	O4
02H	O11	O10	O9	O8
03H	O15	O14	O13	O12
04H	O19	O18	O17	O16
05H	O23	O22	O21	O20

P62 - \overline{CS}

P63 - LH

