

### 4M-BIT CMOS FAST SRAM 256K-WORD BY 16-BIT

#### Description

The μPD434016A is a high speed, low power, 4,194,304 bits (262,144 words by 16 bits) CMOS static RAM.

Operating supply voltage is 5.0 V ± 0.5 V.

The μPD434016A is packaged in 44-pin plastic SOJ and 44-pin plastic TSOP (II).

#### Features

- 262,144 words by 16 bits organization
- Fast access time : 12, 15, 17, 20 ns (MAX.)
- Byte data control : /LB (I/O1 - I/O8), /UB (I/O9 - I/O16)
- Output Enable input for easy application
- Single +5.0 V power supply

#### Ordering Information

Part number	Package	Access time (MAX.)	Supply current (MAX.)	
			At operating	At standby
μPD434016ALE-12	44-pin plastic SOJ (400 mil)	12 ns	230 mA	10 mA
μPD434016ALE-15		15 ns	220 mA	
μPD434016ALE-17		17 ns	210 mA	
μPD434016ALE-20		20 ns	200 mA	
μPD434016AG5-12-7JF	44-pin plastic TSOP (II) (400 mil) (Normal bent)	12 ns	230 mA	
μPD434016AG5-15-7JF		15 ns	220 mA	
μPD434016AG5-17-7JF		17 ns	210 mA	
μPD434016AG5-20-7JF		20 ns	200 mA	

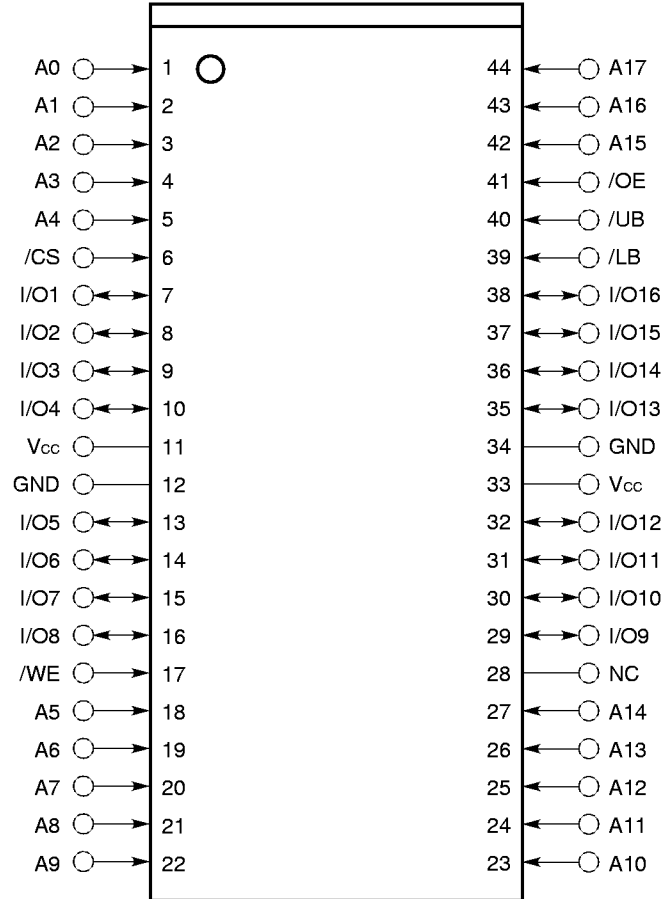
The information in this document is subject to change without notice.

Pin Configurations (Marking Side)

/xxx indicates active low signal.

44-pin plastic SOJ (400 mil)

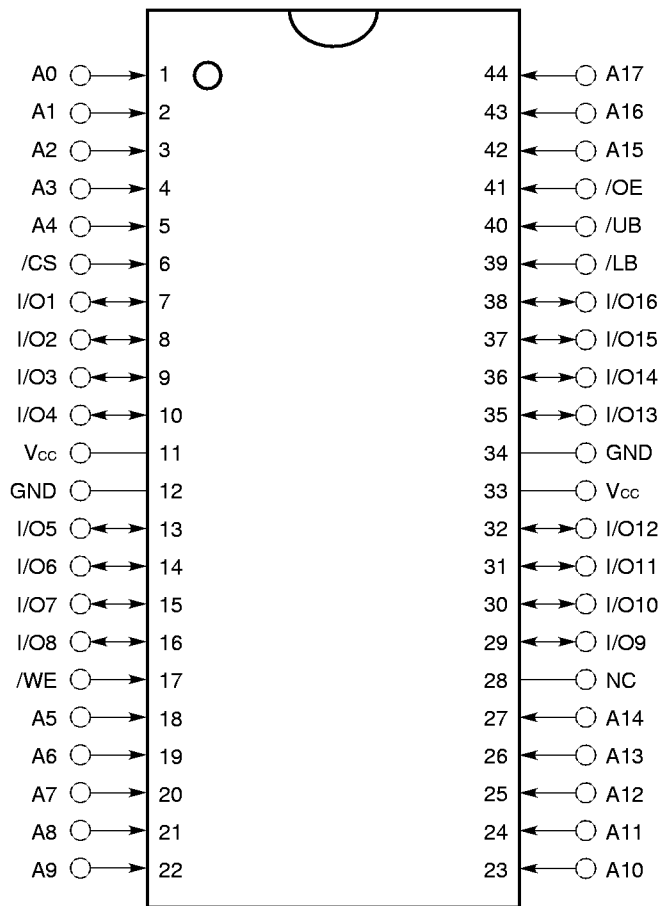
[ μPD434016ALE ]



- A0 - A17 : Address Inputs
- I/O1 - I/O16 : Data Inputs / Outputs
- /CS : Chip Select
- /WE : Write Enable
- /OE : Output Enable
- /LB, /UB : Byte data select
- Vcc : Power supply
- GND : Ground
- NC : No connection

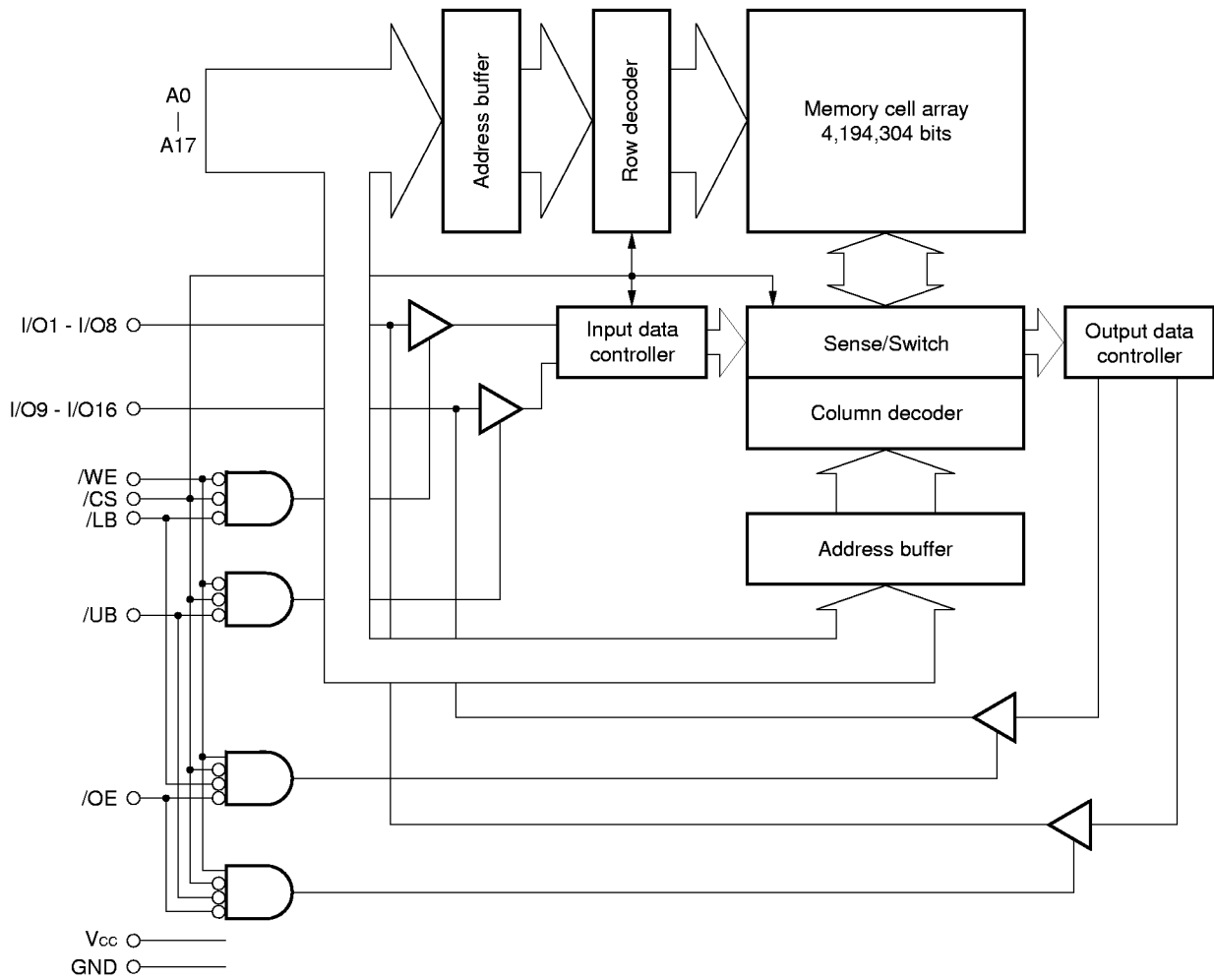
44-pin plastic TSOP (II) (400 mil) (Normal Bent)

[ μPD434016AG5-7JF ]



- A0 - A17 : Address Inputs
- I/O1 - I/O16 : Data Inputs / Outputs
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- GND : Ground
- NC : No connection

Block Diagram



Truth Table

/CS	/OE	/WE	/LB	/UB	Mode	I/O		Supply current
						I/O1 - I/O8	I/O9 - I/O16	
H	x	x	x	x	Not selected	High impedance	High impedance	I <sub>SB</sub>
L	L	H	L	L	Read	D <sub>OUT</sub>	D <sub>OUT</sub>	I <sub>CC</sub>
			L	H		D <sub>OUT</sub>	High impedance	
			H	L		High impedance	D <sub>OUT</sub>	
L	x	L	L	L	Write	D <sub>IN</sub>	D <sub>IN</sub>	
			L	H		D <sub>IN</sub>	High impedance	
			H	L		High impedance	D <sub>IN</sub>	
L	H	H	x	x	Output disable	High impedance	High impedance	
L	x	x	H	H		High impedance	High impedance	

Remark x : Don't care

**Electrical Specifications**

**Absolute Maximum Ratings**

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V <sub>CC</sub>		-0.5 <sup>Note</sup> to +7.0	V
Input / Output voltage	V <sub>I</sub>		-0.5 <sup>Note</sup> to V <sub>CC</sub> +0.5	V
Operating ambient temperature	T <sub>A</sub>		0 to +70	°C
Storage temperature	T <sub>stg</sub>		-55 to +125	°C

**Note** -2.0 V (MIN.) (pulse width : 2 ns)

**Caution** Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V <sub>CC</sub>		4.5	5.0	5.5	V
High level input voltage	V <sub>IH</sub>		2.2		V <sub>CC</sub> +0.5	V
Low level input voltage	V <sub>IL</sub>		-0.5 <sup>Note</sup>		+0.8	V
Operating ambient temperature	T <sub>A</sub>		0		70	°C

**Note** -2.0 V (MIN.) (pulse width : 2 ns)

**DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)**

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input leakage current	$I_{LI}$	$V_{IN} = 0\text{ V to }V_{CC}$	-2		+2	μA
Output leakage current	$I_{LO}$	$V_{I/O} = 0\text{ V to }V_{CC}$ , /CS = $V_{IH}$ or /OE = $V_{IH}$ or /WE = $V_{IL}$ or /LB = $V_{IH}$ or /UB = $V_{IH}$	-2		+2	μA
Operating supply current	$I_{CC}$	/CS = $V_{IL}$ , $I_{I/O} = 0\text{ mA}$ , Minimum cycle time	Cycle time : 12 ns		230	mA
			Cycle time : 15 ns		220	
			Cycle time : 17 ns		210	
			Cycle time : 20 ns		200	
Standby supply current	$I_{SB}$	/CS = $V_{IH}$ , $V_{IN} = V_{IH}$ or $V_{IL}$			50	mA
	$I_{SB1}$	$V_{CC} - 0.2\text{ V} \leq /CS$ , $V_{IN} \leq 0.2\text{ V}$ or $V_{CC} - 0.2\text{ V} \leq V_{IN}$			10	
High level output voltage	$V_{OH}$	$I_{OH} = -4.0\text{ mA}$	2.4			V
Low level output voltage	$V_{OL}$	$I_{OL} = +8.0\text{ mA}$			0.4	V

**Remark**  $V_{IN}$  : Input voltage

**Capacitance ( $T_A = 25\text{ °C}$ ,  $f = 1\text{ MHz}$ )**

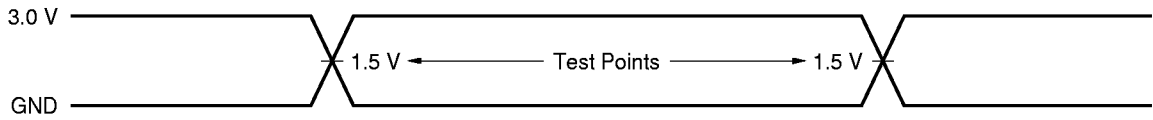
Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	$C_{IN}$	$V_{IN} = 0\text{ V}$			6	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O} = 0\text{ V}$			10	pF

- Remarks**
- $V_{IN}$  : Input voltage
  - These parameters are periodically sampled and not 100% tested.

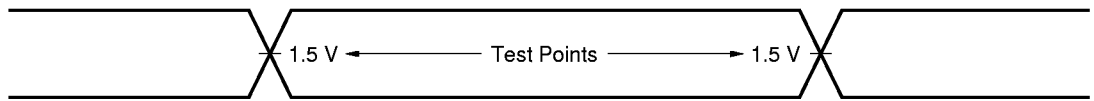
AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

AC Test Conditions

Input Waveform (Rise and Fall Time ≤ 3 ns)



Output Waveform

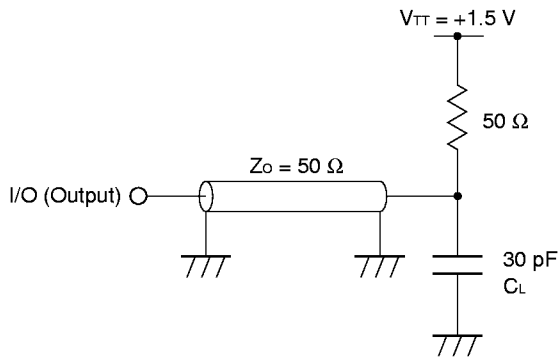


Output Load

AC characteristics directed with the note should be measured with the output load shown in **Figure 1** or **Figure 2**.

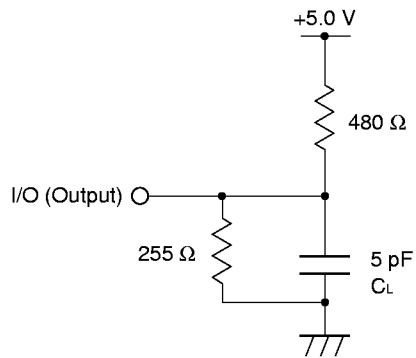
**Figure 1**

(for tAA, tACS, toE, tABD, toH)



**Figure 2**

(for tCLZ, toLZ, tBLZ, tCHZ, toHZ, tBHZ, tWHZ, toW)



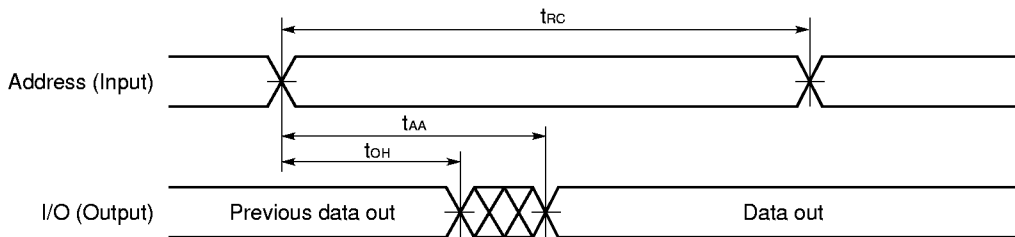
**Remark** CL includes capacitances of the probe and jig, and stray capacitances.

Read Cycle

Parameter	Symbol	-12		-15		-17		-20		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t <sub>RC</sub>	12		15		17		20		ns	
Address access time	t <sub>AA</sub>		12		15		17		20	ns	1
/CS access time	t <sub>ACS</sub>		12		15		17		20	ns	
/OE access time	t <sub>OE</sub>		6		7		8		10	ns	
/LB, /UB access time	t <sub>ABD</sub>		6		7		8		10	ns	
Output hold from address change	t <sub>OH</sub>	3		3		3		3		ns	
/CS to output in low impedance	t <sub>CLZ</sub>	3		3		3		3		ns	2, 3
/OE to output in low impedance	t <sub>OLZ</sub>	0		0		0		0		ns	
/LB, /UB to output in low impedance	t <sub>BLZ</sub>	0		0		0		0		ns	
/CS to output in high impedance	t <sub>CHZ</sub>		6		7		8		8	ns	
/OE to output hold in high impedance	t <sub>OHZ</sub>		6		7		8		8	ns	
/LB, /UB to output hold in high impedance	t <sub>BHZ</sub>		6		7		8		8	ns	

- Notes**
1. See the output load shown in **Figure 1**.
  2. Transition is measured at ± 200 mV from steady-state voltage with the output load shown in **Figure 2**.
  3. These parameters are periodically sampled and not 100% tested.

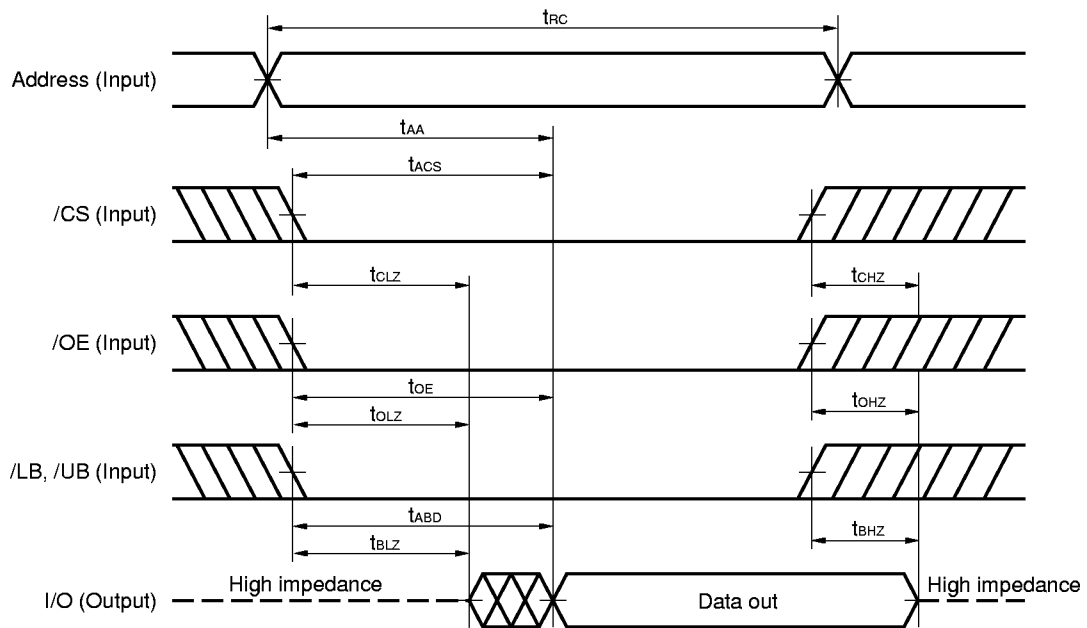
Read Cycle Timing Chart 1 (Address Access)



- Remarks**
1. In read cycle, /WE should be fixed to high level.
  2. /CS = /OE = /LB (or /UB) = V<sub>IL</sub>



Read Cycle Timing Chart 2 (/CS Access)



**Caution** Address valid prior to or coincident with /CS low level input.

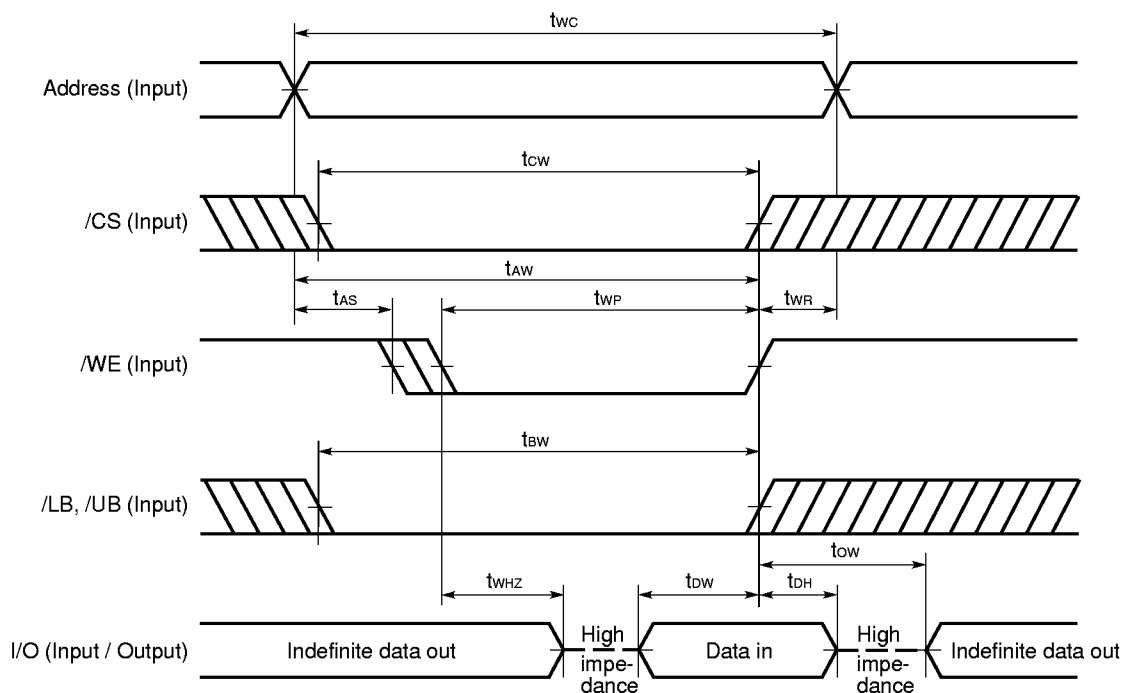
**Remark** In read cycle, /WE should be fixed to high level.

Write Cycle

Parameter	Symbol	-12		-15		-17		-20		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	$t_{wc}$	12		15		17		20		ns	
/CS to end of write	$t_{cw}$	8		10		11		12		ns	
Address valid to end of write	$t_{aw}$	8		10		11		12		ns	
Write pulse width	$t_{wp}$	8		10		11		12		ns	
/LB, /UB to end of write	$t_{bw}$	8		10		11		12		ns	
Data valid to end of write	$t_{dw}$	6		7		8		9		ns	
Data hold time	$t_{dh}$	0		0		0		0		ns	
Address setup time	$t_{as}$	0		0		0		0		ns	
★ Write recovery time	$t_{wr}$	1		1		1		1		ns	
/WE to output in high impedance	$t_{whz}$		6		7		8		8	ns	1, 2
Output active from end of write	$t_{ow}$	3		3		3		3		ns	

- Notes 1.** Transition is measured at ± 200 mV from steady-state voltage with the output load shown in **Figure 2**.  
**2.** These parameters are periodically sampled and not 100% tested.

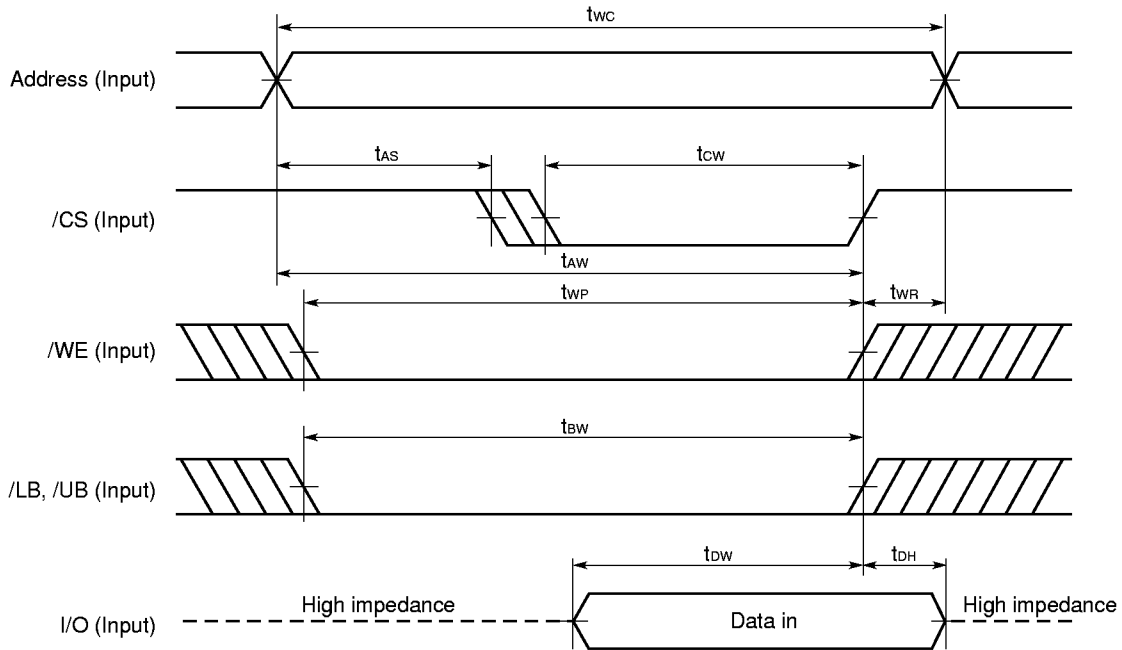
Write Cycle Timing Chart 1 (/WE Controlled)



**Caution** /CS or /WE should be fixed to high level during address transition.

- Remarks 1.** Write operation is done during the overlap time of a low level /CS, a low level /WE and a low level /LB (or low level /UB).  
**2.** During  $t_{whz}$ , I/O pins are in the output state, therefore the input signals of opposite phase to the output must not be applied.  
**3.** When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

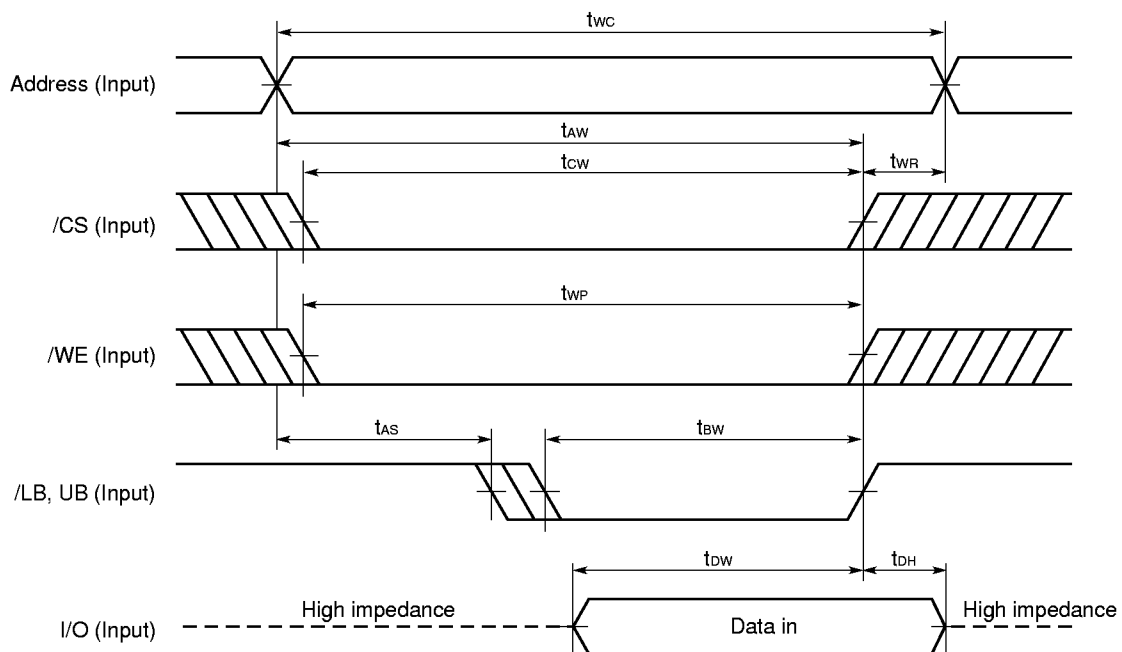
Write Cycle Timing Chart 2 (/CS Controlled)



**Caution** /CS or /WE should be fixed to high level during address transition.

**Remark** Write operation is done during the overlap time of a low level /CS, a low level /WE and a low level /LB (or low level /UB).

Write Cycle Timing Chart 3 (/LB, /UB Controlled)

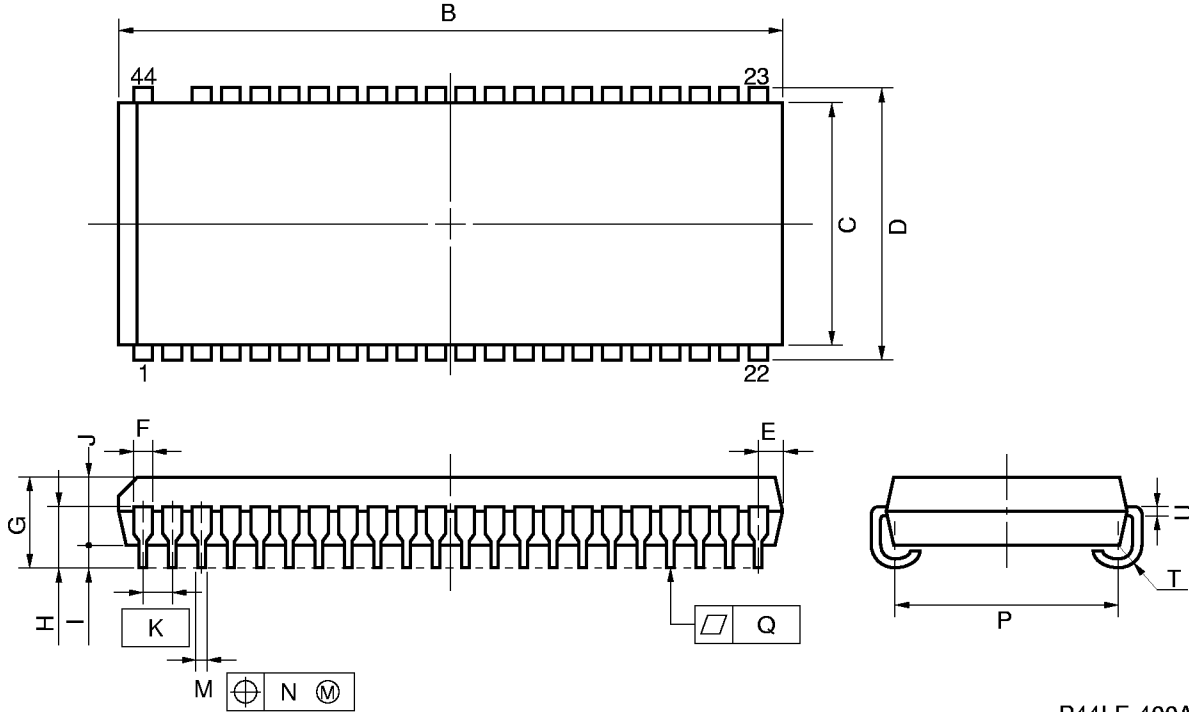


**Caution** /CS or /WE should be fixed to high level during address transition.

**Remark** Write operation is done during the overlap time of a low level /CS, a low level /WE and a low level /LB (or low level /UB).

Package Drawings

44 PIN PLASTIC SOJ (400 mil)



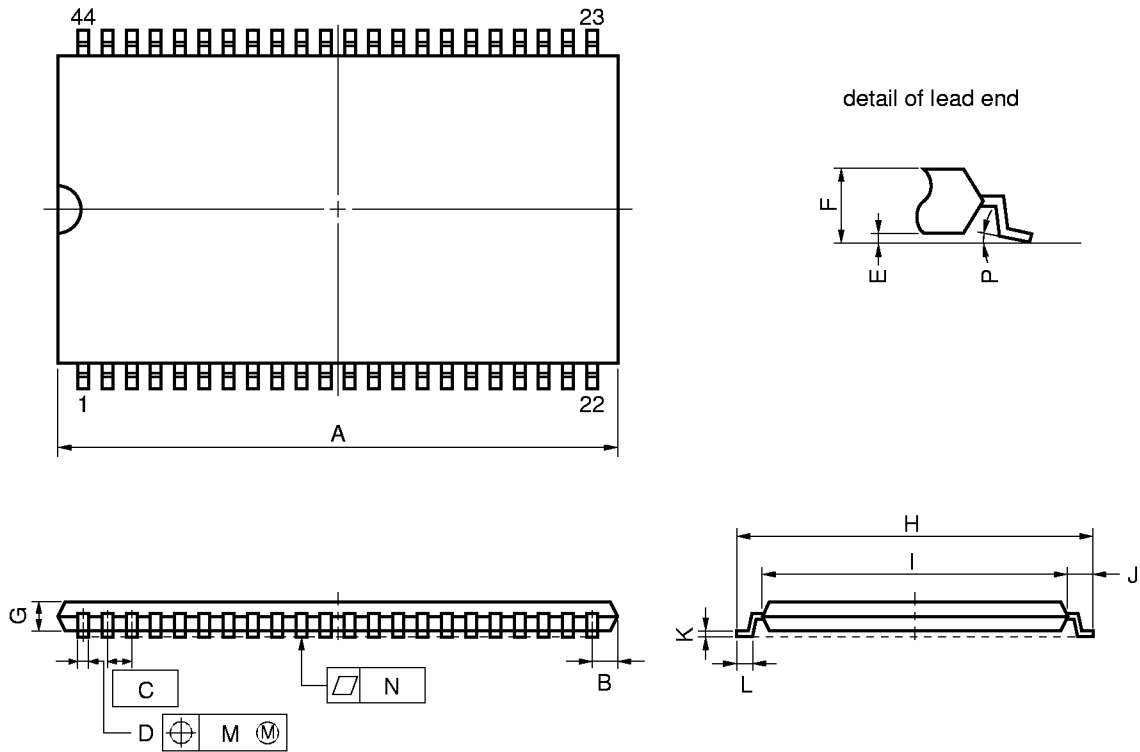
P44LE-400A

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	28.73 <sup>+0.2</sup> <sub>-0.35</sub>	1.131 <sup>+0.008</sup> <sub>-0.014</sub>
C	10.16	0.400
D	11.18±0.20	0.440±0.008
E	1.03±0.15	0.041 <sup>+0.006</sup> <sub>-0.007</sub>
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.3±0.2	0.091 <sup>+0.008</sup> <sub>-0.009</sub>
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 <sup>+0.004</sup> <sub>-0.005</sub>
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	0.20 <sup>+0.10</sup> <sub>-0.05</sub>	0.008 <sup>+0.004</sup> <sub>-0.002</sub>

44 PIN PLASTIC TSOP(II) (400 mil)



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.63 MAX.	0.734 MAX.
B	0.93 MAX.	0.037 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.32 <sup>+0.08</sup> <sub>-0.07</sub>	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 <sup>+0.009</sup> <sub>-0.008</sub>
K	0.145 <sup>+0.025</sup> <sub>-0.015</sub>	0.006±0.001
L	0.5±0.1	0.020 <sup>+0.004</sup> <sub>-0.005</sub>
M	0.13	0.005
N	0.10	0.004
P	3° <sup>+7°</sup> <sub>-3°</sub>	3° <sup>+7°</sup> <sub>-3°</sub>

S44G5-80-7JF5

**Recommended Soldering Conditions**

Please consult with our sales offices for soldering conditions of the  $\mu$ PD434016A.

**Type of Surface Mount Device**

$\mu$ PD434016ALE : 44-pin plastic SOJ (400 mil)

$\mu$ PD434016AG5-7JF : 44-pin plastic TSOP (II) (400 mil) (Normal Bent)