Video enhancement and D/A processor (VEDA)

SAA9065

1. FEATURES

- CMOS circuit to enhance video data and to convert luminance and colour-difference signals from digital-to-analog
- 16-bit parallel input for 4:1:1 and 4:2:2 YUV data
- Data clock input LLC (line-locked clock) for a data rate up to 30 MHz
- 8-bit luminance and 8-bit multiplexed colour-difference formats (optional 7-bit formats)
- MC input to support various clock and pixel rates
- Formatter for YUV input data; 4:2:2 format, 4:1:1 format and filter characteristics selectable
- HREF input to determine the active line (number of pixels)
- Controllable peaking of luminance signal
- Coring stage with controllable threshold to eliminate noise in luminance signal
- Interpolation filter suitable for both formats to increase the data rate in chrominance path
- Polarity of colour-difference signals selectable
- Separate digital-to-analog converters (9-bit resolution for Y; 8-bit for colour-difference signals)
- 1 V (p-p)/ 75 Ω outputs realized by two resistors
- No external adjustments
- All functions controlled via I^2C-bus

2. QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	supply voltage digital part	4.5	5	5.5	V
V_{DDA}	supply voltage analog part	4.75	5	5.25	V
I_{DD}	total supply current	-	tbf	-	mA
V_{IL}	input voltage LOW on YUV-bus	−0.5	-	0.8	V
V_{IH}	input voltage HIGH on YUV-bus	2	-	V_{DDD}+0.5	V
f_{LLC}	input data rate	-	-	30	MHz
$V_{o\ Y,CD}$	output signal Y, ±(R–Y) and ±(B–Y) (peak-to-peak value)	-	2	-	V
$R_{L\ Y,CD}$	output load resistance	125	-	-	Ω
ILE	DC integral linearity error in output signal (8-bit data)	-	-	1	LSB
DLE	DC differential error in output signal (8-bit data)	-	-	0.5	LSB
T_{amb}	operating ambient temperature range	0	-	70	°C

3. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA9065	44	PLCC	plastic	SOT187

4. BLOCK DIAGRAM

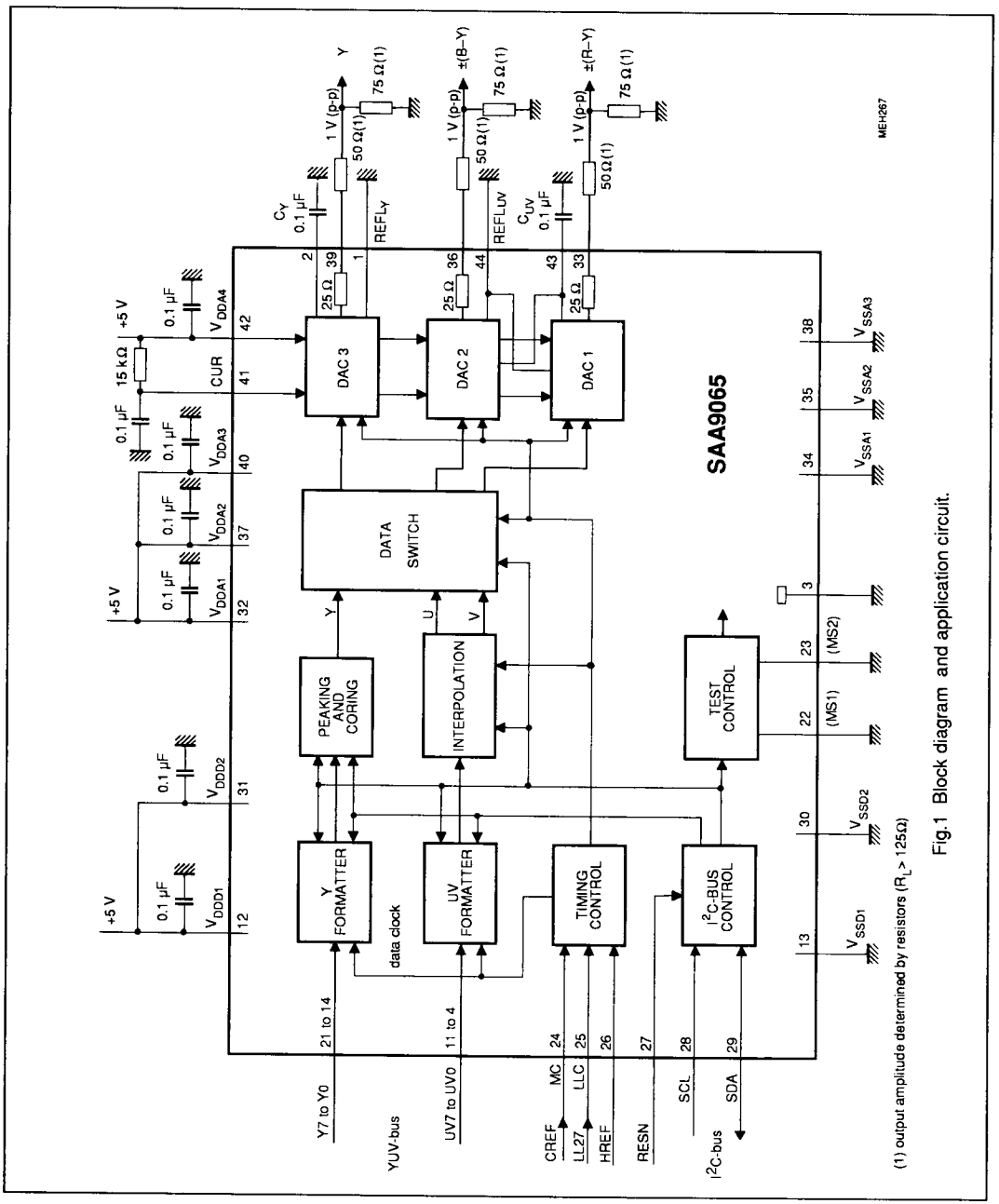


Fig.1 Block diagram and application circuit.

5. PINNING

SYMBOL	PIN	DESCRIPTION
$REFL_Y$	1	low reference of luminance DAC (connected to V_{SSA1})
C_Y	2	capacitor for luminance DAC (high reference)
SUB	3	substrate (connected to V_{SSA1})
UV0	4	UV signal input bits UV7 to UV0 (digital colour-difference signal)
UV1	5	
UV2	6	
UV3	7	
UV4	8	
UV5	9	
UV6	10	
UV7	11	
V_{DDD1}	12	+5 V digital supply voltage 1
V_{SSD1}	13	digital ground 1 (0 V)
Y0	14	Y signal input bits Y7 to Y0 (digital luminance signal)
Y1	15	
Y2	16	
Y3	17	
Y4	18	
Y5	19	
Y6	20	
Y7	21	
MS2	22	mode select 2 input for testing chip
MS1	23	mode select 1 input for testing chip
MC	24	data clock CREF (13.5 MHz e. g.); at MC = HIGH the LLC divider-by-two is inactive
LLC	25	line-locked clock signal (LL27 = 27 MHz)
HREF	26	data clock for YUV data inputs (for active line 768Y or 640Y long)
RESN	27	reset input (active LOW)
SCL	28	I^2C-bus clock line
SDA	29	I^2C-bus data line
V_{SSD2}	30	digital ground 2 (0 V)
V_{DDD2}	31	+5 V digital supply voltage 2
V_{DDA1}	32	+5 V analog supply voltage for buffer of DAC 1
(R–Y)	33	±(R–Y) output signal (analog signal)
V_{SSA1}	34	analog ground 1 (0 V)

SYMBOL	PIN	DESCRIPTION
V_{SSA2}	35	analog ground 2 (0 V)
(B–Y)	36	±(B–Y) output signal (analog colour-difference signal)
V_{DDA2}	37	+5 V analog supply voltage for buffer of DAC 2
V_{SSA3}	38	analog ground 3 (0 V)
Y	39	Y output signal (analog luminance signal)
V_{DDA3}	40	+5 V analog supply voltage for buffer of DAC 3
CUR	41	current input for analog output buffers
V_{DDA4}	42	supply and reference voltage for the three DACs
C_{UV}	43	capacitor for chrominance DACs (high reference)
$REFL_{UV}$	44	low reference of chrominance DACs (connected to V_{SSA1})

PIN CONFIGURATION

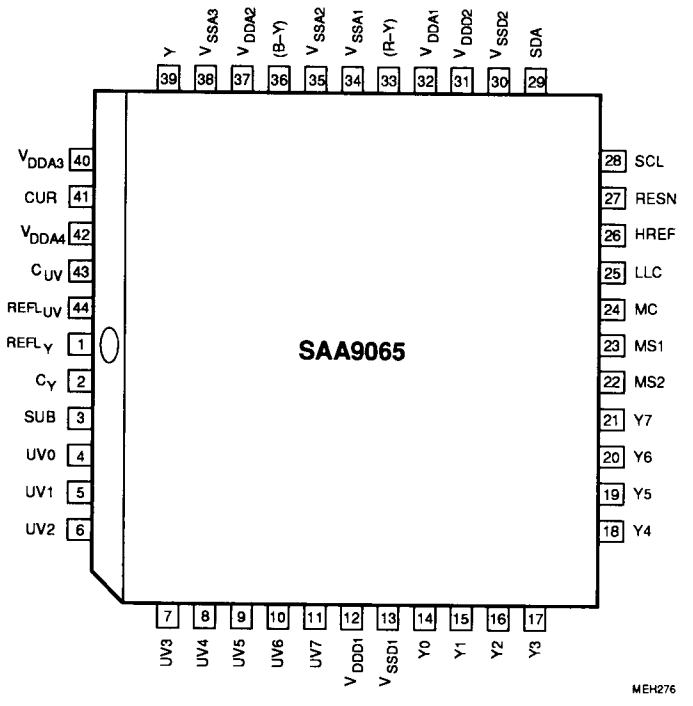


Fig.2 Pin configuration.

6. FUNCTIONAL DESCRIPTION

The CMOS circuit SAA9065 processes digital YUV-bus data up to a data rate of 30 MHz. The data inputs Y7 to Y0 and UV7 to UV0 (Fig.1) are provided with 8-bit data. The data of digital colour-difference signals U and V are in a multiplexed state (serial in 4:2:2 or 4:1:1 format; Tables 2 and 3).

Data is read with the rising edge of LLC (line-locked clock) to achieve a data rate of LLC at MC = HIGH only. If MC is supplied with the frequency CREF (LLC/2 for example), data is read only at every second rising edge (Fig.3).The 7-bit YUV input data are also supported by means of the R78-bit (R78 = 0). Additionally, the luminance data format is converted for internal use into a two´s complement format by inverting MSB. The Y input byte (bits Y7 to Y0) represent luminance information; the UV input byte (bits UV7 to UV0) one of the two digital colour-difference signals in 4:2:2 format (Table 2).

The HREF input signal (HREF = HIGH) determines the start and the end of an active line (Fig.3) the number of pixels respectively . The analog output Y is blanked at HREF = LOW, the (B–Y) and (R–Y) outputs are in a colourless state. The blanking level can be set by the BLV-bit.
The SAA9065 is controllable via the I²C-bus.

Y and UV formatters

The input data formats are formatted into the internally used processing formats (separate for 4:2:2 and 4:1:1 formats). The IFF, IFC and IFL bits control the input data format and determine the right interpolation filter (Figures 10 to 13).

Peaking and coring

Peaking is applied to the Y signal to compensate several bandwidth reductions of the external pre-processing. Y signals can be improved to obtain a better sharpness.
There are the two switchable bandpass filters BF1 and BF 2 controlled via the I²C-bus by the bits BP1, BP0 and BFB. Thus, a frequency response is achieved in combination with the peaking factor K (Figures 5 to 9; K is determined by the bits BFB, WG1 and WG0).

The coring stage with controllable threshold (4 states controlled by CO1 and CO0 bits) reduces noise disturbances (generated by the bandpass gain) by suppressing the amplitude of small high-frequent signal components. The remaining high-frequent peaking component is available for a weighted addition after coring.

Table 1 LLC and MC configuration modes in DMSD applications

PIN	INPUT SIGNAL	COMMENT
LLC MC	LLC (LL27) CREF	The data rate on YUV-bus is half the clock rate on pin LLC, e. g. in SAA7151B, SAA7191 and SAA7191B single scan operation.
LLC MC	LLC (LL27) MC = HIGH	The data rate on YUV-bus must be identical to the clock rate on pin LLC, e. g. in double scan applications.
LLC MC	LLC2/LL3 MC = HIGH	The data rate on YUV-bus must be identical to the clock rate on pin LLC, e. g. SAA9051 single scan operation.
Note: YUV data are only latched with the rising edge of LLC at MC = HIGH.		

Table 2 Data format 4 : 2 : 2. (Fig.3)

INPUT	PIXEL BYTE SEQUENCE					
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	U0	V0	U0	V0	U0	V0
UV1	U1	V1	U1	V1	U1	V1
UV2	U2	V2	U2	V2	U2	V2
UV3	U3	V3	U3	V3	U3	V3
UV4	U4	V4	U4	V4	U4	V4
UV5	U5	V5	U5	V5	U5	V5
UV6	U6	V6	U6	V6	U6	V6
UV7(MSB)	U7	V7	U7	V7	U7	V7
Y frame	0	1	2	3	4	5
UV frame	0		2		4	

Interpolation

The chrominance interpolation filter consists of various filter stages, multiplexers and de-multiplexers to increase the data rate of the colour-difference signals by a factor of 2 or 4. The switching of the filters by the bits IFF, IFC and IFL is described previously. Additional signal samples with significant amplitudes between two consecutive signal samples of the low data rate are generated. The time-multiplexed U and V samples are stored in parallel for converting.

Data switch

The digital signals are adapted to the conversation range. U and V data have 8-bit formats again; Y can have 9 bits dependent on peaking. Blanking and switching to colourless level is applied here. Bits can be inverted by INV-bit to change the polarity of colour-difference output signals.

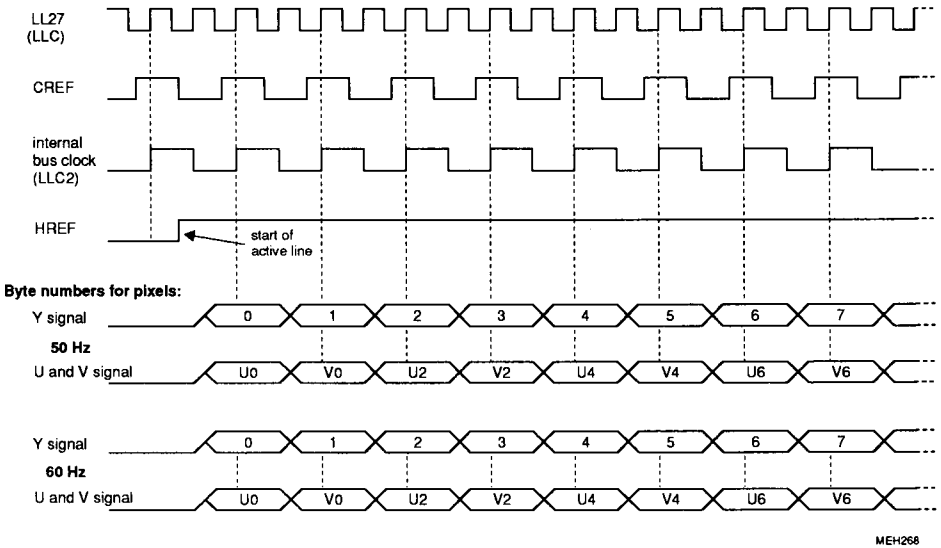
Digital-to-analog converters

Conversion is separate for Y, U and V. The converters use resistor chains with low-impedance output buffers. The minimum output voltage is 200 mV to reduce integral non-linearity errors. The analog signal, without load on output pin, is between 0.2 and 2.2 V floating. An application for 1 V/ 75 Ω on outputs is shown in Fig.1.

Each digital-to-analog converter has its own supply and ground pins suitable for decoupling. The reference voltage, supplying the resistor chain of all three DACs, is the supply voltage V_{DDA4}. The current into pin 41 is 0.3 mA ; a larger current improves the bandwidth but increases the integral non-linearity.

Table 3 Data format 4 : 1 : 1

INPUT	PIXEL BYTE SEQUENCE							
Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
UV0	0	0	0	0	0	0	0	0
UV1	0	0	0	0	0	0	0	0
UV2	0	0	0	0	0	0	0	0
UV3	0	0	0	0	0	0	0	0
UV4	V6	V4	V2	V0	V6	V4	V2	V0
UV5	V7	V5	V3	V1	V7	V5	V3	V1
UV6	U6	U4	U2	U0	U6	U4	U2	U0
UV7	U7	U5	U3	U1	U7	U5	U3	U1
Y frame	0	1	2	3	4	5	6	7
UV frame	0				4			



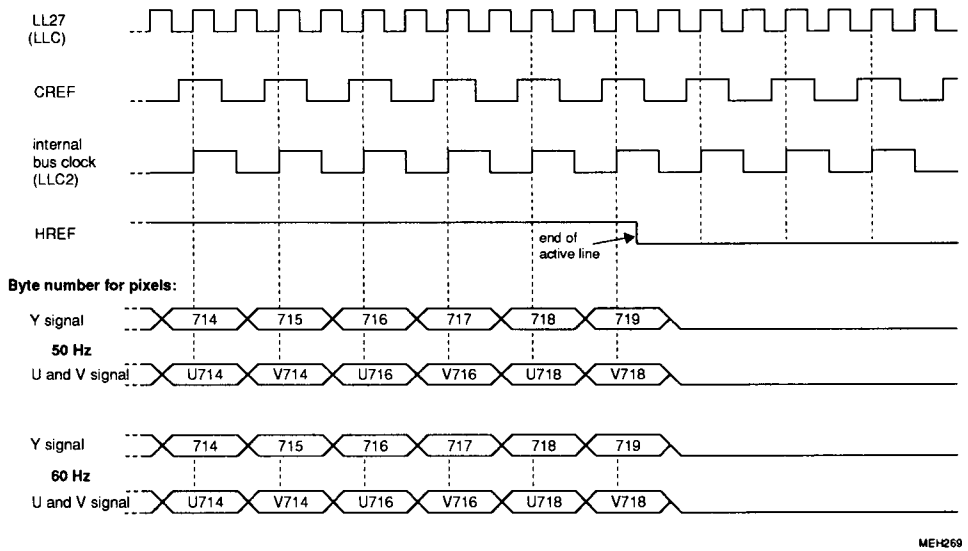


Fig.3 Line control by HREF for 4 : 2 : 2 format, CREF = 13.5 MHz; HREF = 720 pixel; 50 Hz and 60 Hz field.

7. LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD1}	supply voltage range (pin 12)	−0.3	7	V
V_{DDD2}	supply voltage range (pin 31)	−0.3	7	V
V_{DDA1}	supply voltage range (pin 32)	−0.3	7	V
V_{DDA2}	supply voltage range (pin 37)	−0.3	7	V
V_{DDA3}	supply voltage range (pin 40)	−0.3	7	V
V_{DDA4}	supply voltage range (pin 42)	−0.3	7	V
$V_{diff\ GND}$	difference voltage $V_{SSD} - V_{SSA}$	-	±100	mV
V_n	voltage on all input pins 4 to 11, 14 to 27 and 41	−0.3	V_{DDD}	V
V_n	voltage on analog output pins 33, 36 and 39	−0.3	V_{DDD}	V
P_{tot}	total power dissipation	0	tbf	mW
T_{stg}	storage temperature range	−55	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	±2000	-	V

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

8. THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction-to-ambient in free air	46 K/W

9. CHARACTERISTICS

V_{DDD} = 4.5 to 5.5 V; V_{DDA} = 4.75 to 5.25 V; LLC = LL27; MC = CREF = 13.5 MHz; T_{amb} = 0 to 70 °C; measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD1}	supply voltage range (pin 12)	for digital part	4.5	5	5.5	V
V_{DDD2}	supply voltage range (pin 31)	for digital part	4.5	5	5.5	V
V_{DDA1}	supply voltage range (pin 32)	for buffer of DAC 1	4.75	5	5.25	V
V_{DDA2}	supply voltage range (pin 37)	for buffer of DAC 2	4.75	5	5.25	V
V_{DDA3}	supply voltage range (pin 40)	for buffer of DAC 3	4.75	5	5.25	V
V_{DDA4}	supply voltage range (pin 42)	DAC reference voltage	4.75	5	5.25	V
I_{DDD}	supply current (I_{DDD1} + I_{DDD2})	for digital part	-	tbf	tbf	mA
I_{DDA}	supply current (I_{DDA1} to I_{DDA4})	for DACs and buffers	-	tbf	tbf	mA
YUV-bus inputs (pins 4 to 11 and 14 to 21)		Figures 3 and 4				
V_{IL}	input voltage LOW		−0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}+0.5	V
C_I	input capacitance	V_I = HIGH	-	-	10	pF
I_{LI}	input leakage current		-	-	4.5	µA
Inputs MS1, MS2, MC, LLC, HREF and RESN (pins 22 to 27)						
V_{IL}	input voltage LOW		−0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}+0.5	V
C_I	input capacitance	V_I = HIGH	-	-	10	pF
I_{LI}	input leakage current		-	-	4.5	µA
V_{24}	MC input voltage for LL27	27 MHz data rate	2.0	-	V_{DDD}+0.5	V
	CREF signal on MC input	CREF data rate; note 1	-	-	-	V
I²C-bus SCL and SDA (pins 28 and 29)						
V_{IL}	input voltage LOW		−0.5	-	1.5	V
V_{IH}	input voltage HIGH		3.0	-	V_{DDD}+0.5	V
I_I	input current	V_I = LOW or HIGH	-	-	±10	µA
V_{OL}	SDA output voltage LOW (pin 29)	I_{29} = 3 mA	-	-	0.4	V
I_{29}	output current	during acknowledge	3	-	-	mA
Digital-to-analog converters (pins 1, 2, 41, 42, 43 and 44)						
V_{DAC}	input reference voltage for internal resistor chains (pin 42)		4.75	5	5.25	V
I_{CUR}	input current (pin 41)	R_{41-42} = 15 kΩ	-	300	-	µA
$V_{1,44}$	reference voltage LOW	pin connected to V_{SSA1}	-	0	-	V
C_L	external blocking capacitor to V_{SSA1} for reference voltage HIGH (pins 2 and 43)		-	0.1	-	µF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{LLC}	data conversation rate (clock)	Fig.3	-	-	30	MHz
Res	resolution	luminance DAC	-	9	-	bit
		chrominance DACs	-	8	-	bit
ILE	DC integral linearity error	8-bit data	-	-	1.0	LSB
DLE	DC differential error	8-bit data	-	-	0.5	LSB
Y, ±(R–Y) and ±(B–Y) analog outputs (pins 39, 33 and 36)						
V_o	output signal voltage (peak-to-peak value)	without load	-	2	-	V
$V_{33,36,39}$	output voltage range	without load; note 2	0.2	-	2.2	V
V_{39}	output blanking level	Y output; note 3	-	16	-	LSB
$V_{33,36}$	output no-colour level	±(R–Y), ±(B–Y); note 4	-	128	-	LSB
$R_{33,36,39}$	internal serial output resistance		-	25	-	Ω
$R_{L\ 33,36,39}$	output load resistance	external load	125	-	-	Ω
B	output signal bandwidth	-3 dB	20	-	-	MHz
t_d	signal delay from input to Y output		-	tbf	-	ns
LLC timing (pins 25)		LLC; Fig.3				
t_{LLC}	cycle time		33	37	41	ns
$t_{p\,H}$	pulse width		40	50	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns
YUV-bus timing (pins 4 to 11 and 14 to 21)		Fig.5				
t_{SU}	input data set-up time		11	-	-	ns
t_{HD}	input data hold time		3	-	-	ns
MC timing (pin24)		Fig.5				
t_{SU}	input data set-up time		11	-	-	ns
t_{HD}	input data hold time		3	-	-	ns
RESN timing (pin 27)						
t_{SU}	set-up time after power-on or failure	active LOW; note 5	4 x t_{LLC}	-	-	ns

Notes to the characteristics

1. YUV-bus data is read at MC = HIGH (pin 24) clocked with LLC (Fig.5) . Data is read only with every second rising edge of LLC when CREF = LLC/2 on MC-pin 24.
2. 0.2 to 2.2 V ouput voltage range at 8-bit DAC input data. The data word can increase to 9-bit dependent on peaking factor.
3. The luminance signal is set to the digital black level: 16 LSB for BLV-bit = 0; 0 LSB for BLV-bit = 1.
4. The chrominance amplitudes are set to the digital colourless level of 128 LSB.
5. The circuit is prepared for a new data initialization.

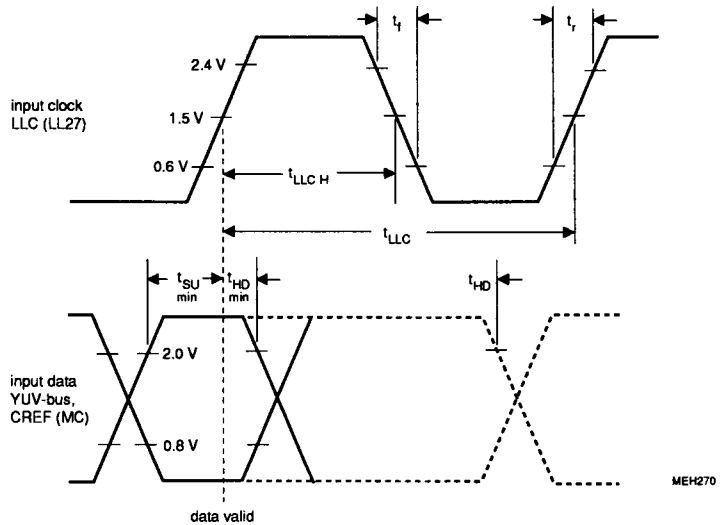


Fig.4 YUV-bus data and CREF timing.

PROCESSING DELAY	LLC CYCLES	REMARKS
YUV digital input to YUV analog output	44 88	at MC = "1" at MC = LLC/2

10. I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A		DATAn	A	P

S = start condition
SLAVE ADDRESS = **1011 111X**
A = acknowledge, generated by the slave
SUBADDRESS* = subadress byte (Table 4)
DATA = data byte (Table 4)
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read (the circuit is slave transmitter)

* If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 4 I²C-bus transmission

FUNCTION	SUBADDRESS	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Peaking and coring	01	0	CO1	CO0	BP1	BP0	BFB	WG1	WG0
Input formats; interpolation	02	IFF	IFC	IFL	0	0	0	0	0
Input/output setting	03	0	0	0	0	DRP	BLV	R78	INV

Bit functions in data bytes:

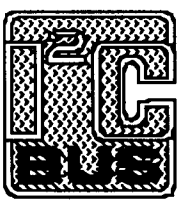
CO1 to CO0 — Control of coring threshold:

CO1	CO0	
0	0	coring off
0	1	small noise reduction
1	0	medium noise reduction
1	1	high noise reduction

BP1, BP0 and BFB — Bandpass filter selection:

BP1	BP0	BFB	
0	0	0	characteristic Fig.5
0	1	0	characteristic Fig.6
1	0	0	characteristic Fig.7
1	1	0	characteristic Fig.8
0	0	1	BF1 filter bypassed Fig.9
X	X	1	not recommended

BFB, WG1 and WG0	Peaking factor K:	BFB	WG1	WG0	
		0	0	0	K = 1/8; minimum peaking
		0	0	1	K = 1/4
		0	1	0	K = 1/2
		0	1	1	K = 1; maximum peaking
		1	0	0	K = 0; peaking off
		1	0	1	K = 1/4; minimum peaking
		1	1	0	K = 1/2
		1	1	1	K = 1; maximum peaking
IFF, IFC, IFL	Input format and filter control at 13.5 MHz data rate:	IFF	IFC	IFL	
		0	0	0	4 : 1 : 1 format; –3 dB attenuation at 1.6 MHz video frequency; Fig.10
		0	0	1	4 : 1 : 1 format; –3 dB attenuation at 600 kHz video frequency; Fig.11
		0	1	0	4 : 1 : 1 format; –3 dB attenuation at 1.2 MHz video frequency; Fig.12
		1	0	0	4 : 2 : 2 format; –3 dB attenuation at 1.6 MHz video frequency; Fig.10
		1	0	1	4 : 2 : 2 format; –3 dB attenuation at 600 kHz video frequency; Fig.11
		1	1	X	4 : 2 : 2 format; –3 dB attenuation at 2.5 MHz video frequency; Fig.13
DRP	UV input data code:	0 = two's complement; 1 = offset binary			
BLV	Blanking level on Y output:	0 = 16 LSB; 1 = 0 LSB			
R78	YUV input data solution:	0 = 7-bit data; 1 = 8-bit data			
INV	Polarity of colour-difference output signals:	0 = normal polarity equal to input signal 1 = inverted polarity			



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

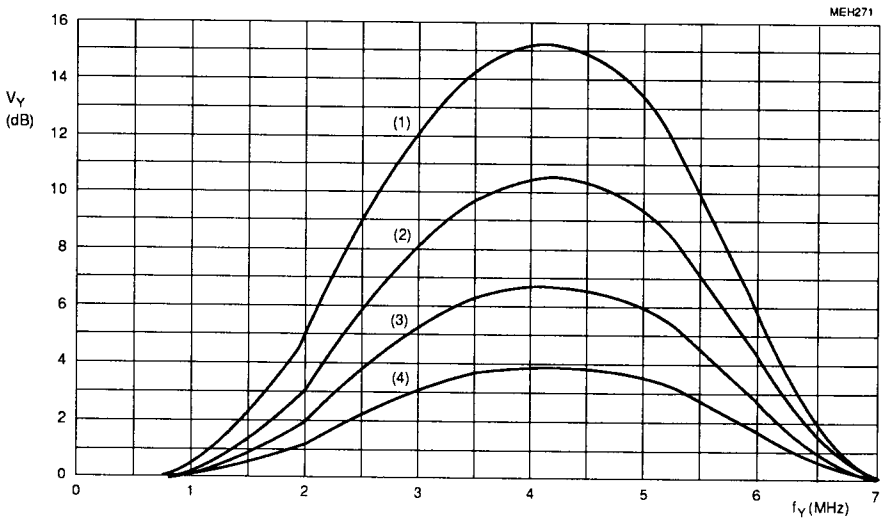


Fig.5 Peaking frequency response with I²C-bus control bits BP1 = 0; BP0 = 0 and BFB = 0: (1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

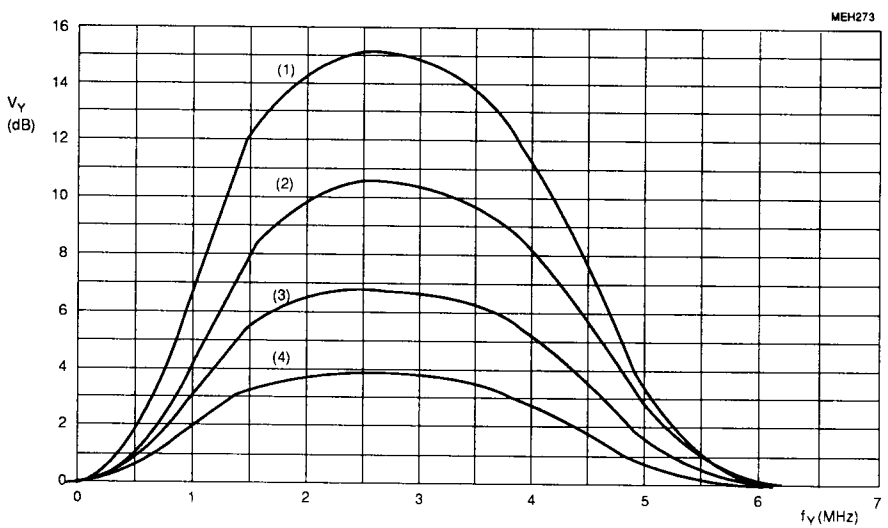


Fig.6 Peaking frequency response with I²C-bus control bits BP1 = 0; BP0 = 1 and BFB = 0: (1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

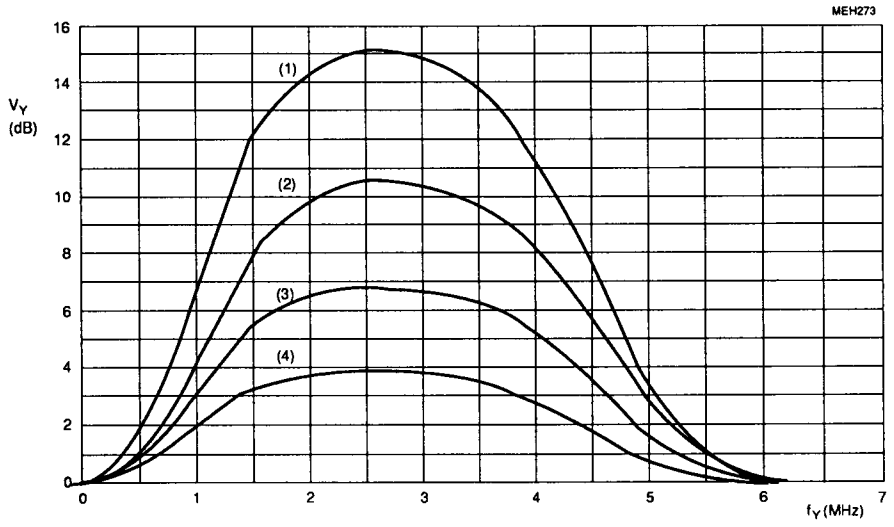


Fig.7 Peaking frequency response with I²C-bus control bits BP1 = 1; BP0 = 0 and BFB = 0: (1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

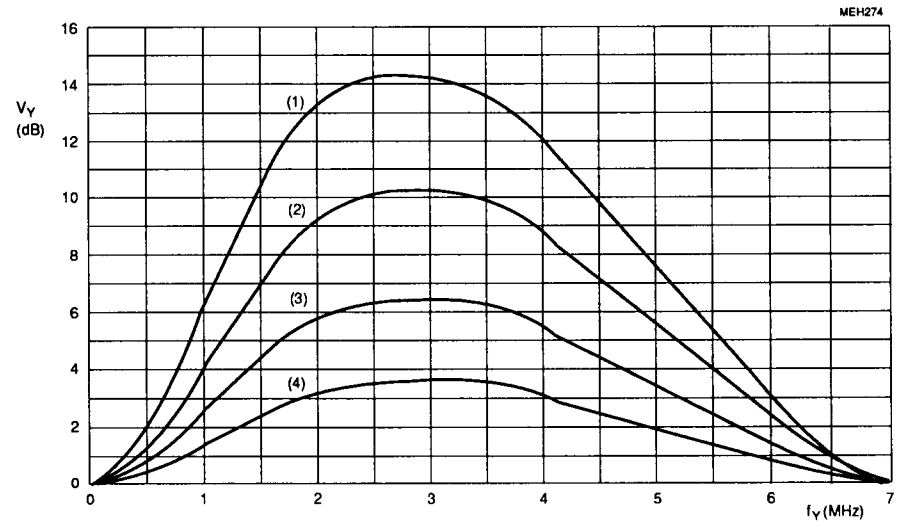


Fig.8 Peaking frequency response with I²C-bus control bits BP1 = 1; BP0 = 1 and BFB = 0: (1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

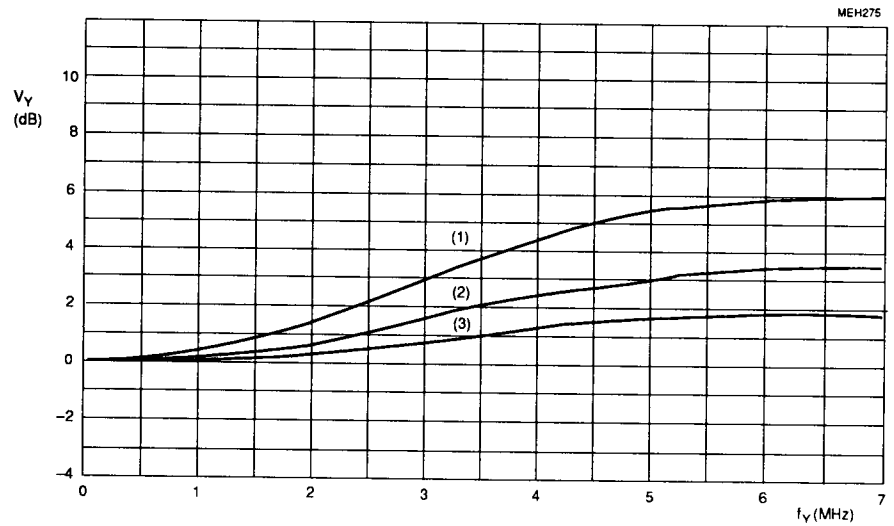


Fig.9 Peaking frequency response with I²C-bus control bits BP1 = 0; BP0 = 0 and BFB = 1; bandpass filter BF1 bypassed and peaking off; (1) K = 1; (2) K = 1/2; (3) K = 1/4.

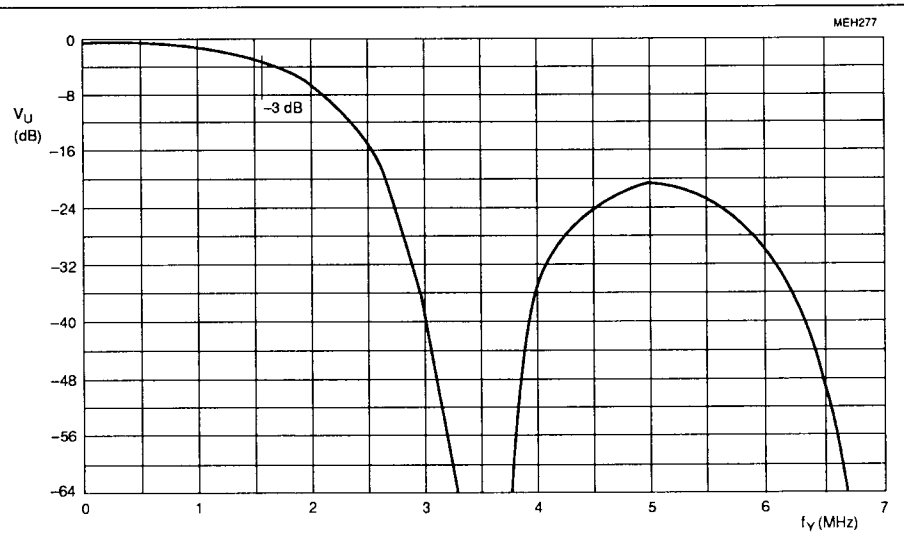


Fig.10 Interpolation filter with I²C-bus control bits IFF = 0; IFC = 0 and IFL = 0 in 4:1:1 format, and control bits IFF = 1; IFC = 0 and IFL = 0 in 4:2:2 format; 13.5 MHz data rate.

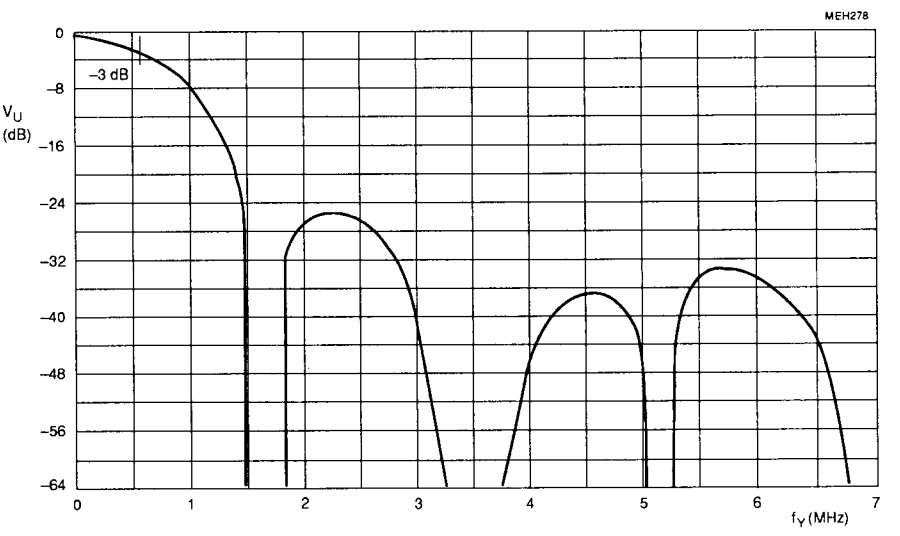


Fig.11 Interpolation filter with I²C-bus control bits IFF = 0; IFC = 0 and IFL = 1 in 4:1:1 format, and control bits IFF = 1; IFC = 0 and IFL = 1 in 4:2:2 format; 13.5 MHz data rate.

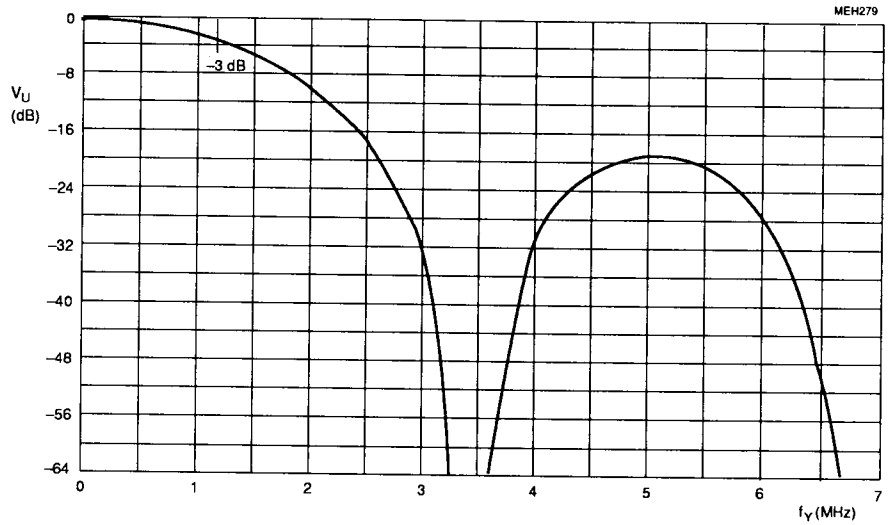


Fig.12 Interpolation filter with I²C-bus control bits IFF = 0; IFC = 1 and IFL = 0 in 4:1:1 format; 13.5 MHz data rate.

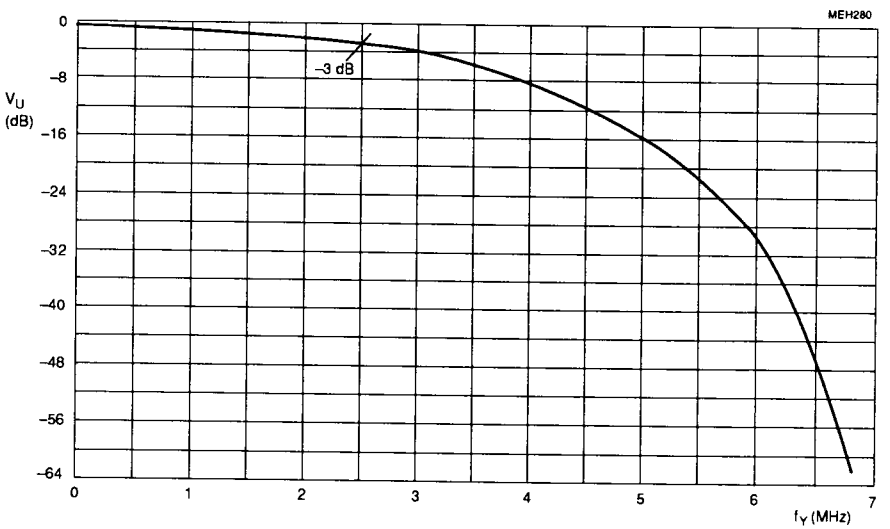


Fig.13 Interpolation filter with I²C-bus control bits IFF = 1; IFC = 1 and IFL = X in 4:2:2 format; 13.5 MHz data rate.