HD44103

(Dot Matrix Liquid Crystal Graphic Display Common Driver)

Description

The HD44103CH is a common signal driver for dot matrix liquid crystal graphic display systems. It generates the timing signals required for display with its internal oscillator and supplies them to the column driver (HD44102CH) to control display, also automatically scanning the common signals of the liquid crystal according to the display duty. It can select 5 types of display duty ratio: 1/8, 1/12, 1/16, 1/24, and 1/32. 20 driver output lines are provided, and the impedance is low (500 Ω max.) to enable a large screen to be driven.

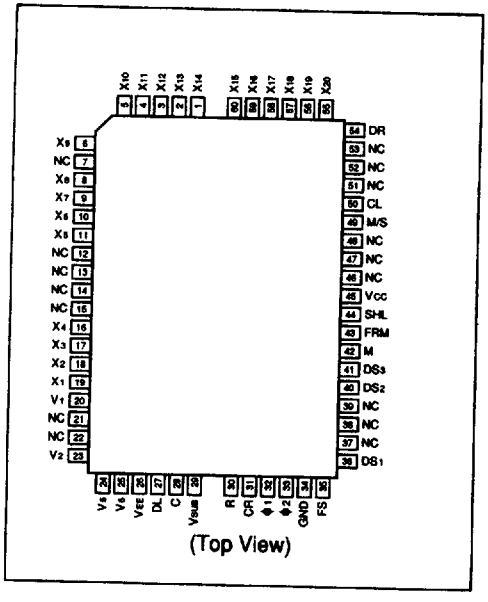
Features

- Dot matrix liquid crystal graphic display common driver incorporating the timing generation circuit
- Internal oscillator (Oscillation frequency can be selected by attaching an oscillation resistor and an oscillation capacity)
- Generates display timing signals
- 20-bit bidirectional shift register for generating common signals
- 20 liquid crystal driver circuits with low output impedance
- Selectable display duty ratio: 1/8, 1/12, 1/16, 1/24, 1/32
- Low power dissipation
- Power supplies: V_{CC}: 5 V ±10%,
  V_{EE}: 0 to –5.5 V
- CMOS process

Ordering Information

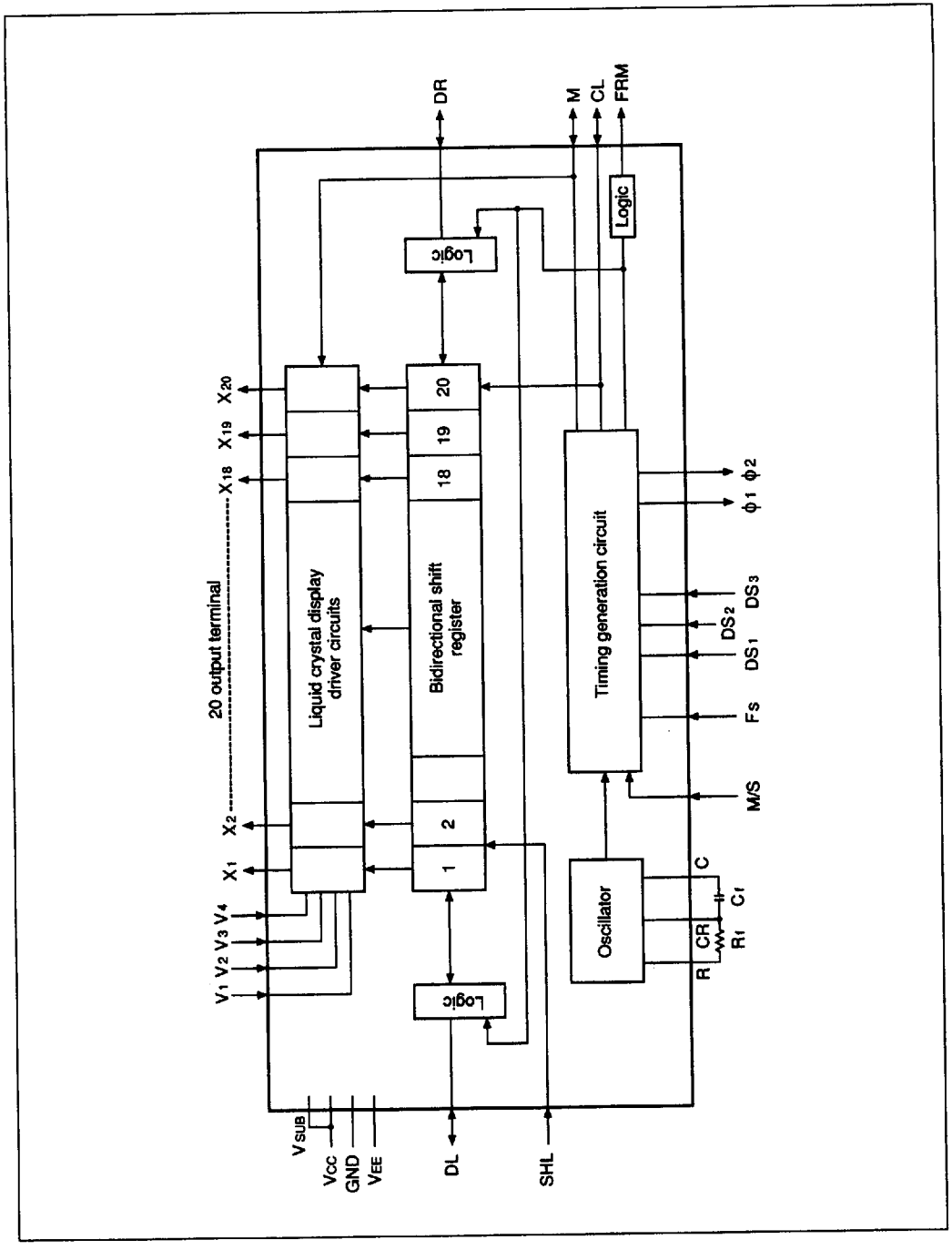
Type No.	Package
HD44103CH	60-pin plastic QFP(FP-60)

Pin Arrangement



(Top View)

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Rated Value	Unit	Note
Supply voltage (1)	V_{CC}	−0.3 to +7.0	V	1
Supply voltage (2)	V_{EE}	V_{CC} −13.5 to V_{CC} + 0.3	V	4
Terminal voltage (1)	V_{T1}	−0.3 to V_{CC} + 0.3	V	1, 2
Terminal voltage (2)	V_{T2}	V_{EE} −0.3 to V_{CC} + 0.3	V	3
Operating temperature	T_{opr}	−20 to +75	°C	
Storage temperature	T_{stg}	−55 to +125	°C	

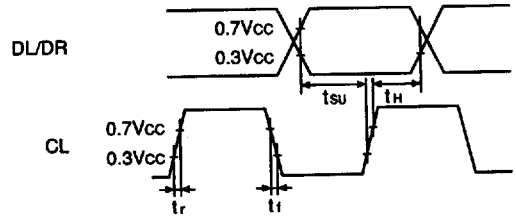
Notes: 1. Referenced to GND = 0.
2. Applied to input terminals (except V1, V2, V5, and V6) and I/O common terminals.
3. Applied to terminals V1, V2, V5, and V6.
4. Connect a protection resistor of 220 Ω ± 5% to V_{EE} power supply in series.

Electrical Characteristics

(V_{CC} = +5 V ±10%, GND = 0 V, V_{EE} = 0 to −5.5 V, Ta = −20 to +75 °C) (Note 5)

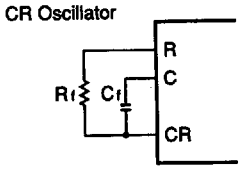
Item	Symbol	Min	Typ	Max	Unit	Test condition	Note
Input high voltage	V_{IH}	0.7 × V_{CC}	–	V_{CC}	V		6
Input low voltage	V_{IL}	0	–	0.3 × V_{CC}	V		6
Output high voltage	V_{OH}	V_{CC} − 0.4	–	–	V	I_{OH} = −400 µA	7
Output low voltage	V_{OL}	–	–	0.4	V	I_{OL} = +400 µA	7
Vi-Xj on resistance	R_{ON}	–	–	500	Ω	V_{EE} = −5 ± 10%, Load current ±150 µA	
Input leakage current (1)	I_{IL1}	−1	–	1	µA	V_{IN} = V_{CC} to GND	8
Input leakage current (2)	I_{IL2}	−2	–	2	µA	V_{IN} = V_{CC} to V_{EE}	9
Shift frequency	f_{SFT}	–	–	50	kHz	In slave mode	10
Oscillation frequency	f_{OSC}	300	430	560	kHz	R_f = 68 kΩ ± 2%, C_f = 10 pF ± 5%	11
External clock operating frequency	f_{cp}	50	–	560	kHz		
External clock duty	Duty	45	50	55	%		12
External clock rise time	t_{rcp}	–	–	50	ns		12
External clock fall time	t_{fcp}	–	–	50	ns		12
Dissipation power (master)	P_{w1}	–	–	4.4	mW	CR oscillation = 430 kHz	13
Dissipation power (slave)	P_{w2}	–	–	1.1	mW	Frame frequency = 70 Hz	14

Notes: 5. Specified within this range unless otherwise noted.
6. Applied to CR, FS, DS1 to DS3, M, SHL, M/S, CL, DR, and DL.
7. Applied to DL, DR, M, FRM, CL, ϕ1 and ϕ2.
8. Applied to input terminals CR, FS, DS1 to DS3, SHL and M/S, and I/O common terminals DL, DR, M, and CL at high impedance.
9. Applied to V1, V2, V5, and V6.
10. Shift operation timing

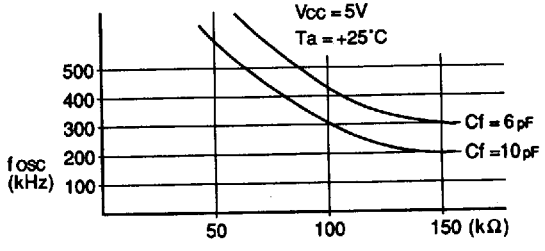


	Min	Typ	Max	Unit
t_{su}	5	–	–	µs
t_H	5	–	–	µs
t_r	–	–	100	ns
t_f	–	–	100	ns

11. Relationship between oscillation frequency and R_f/C_f



The values of R_f and C_f are typical values. The oscillation frequency varies with the mounting condition. Adjust oscillation frequency to the required value.



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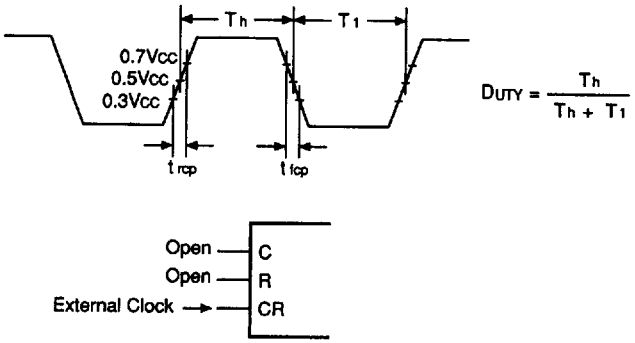
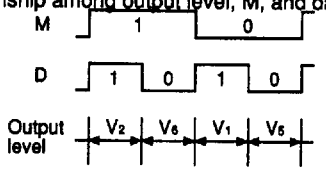
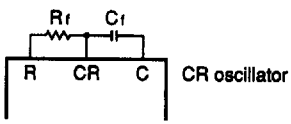
12.



13. Measured by V_{cc} terminal at output non-load of R_f = 68 kΩ ± 2% and C_f = 10pF ± 5%, 1/32 duty factor in the master mode. Input terminals must be fixed at V_{cc} or GND while measuring.
14. Measured by V_{cc} terminal at output non-load, 1/32 duty factor, frame frequency of 70 Hz in the slave mode. Input terminals must be fixed at V_{cc} or GND while measuring.

Pin Description

Pin Name	Pin Number	I/O	Function
X1–X20	20	O	Liquid crystal display driver output. Relationship among output level, M, and data (D) in shift register: 
CR, R, C	3		Oscillator 
M	1	I/O	Signal for converting liquid crystal display driver signal into AC. Master: Output terminal Slave: Input terminal

Pin Name	Pin Number	I/O	Function
CL	1	I/O	Shift register shift clock. Master: Output terminal Slave: Input terminal
FRM	1	O	Frame signal, Display synchronous signal.
DS1–DS3	3	I	Display duty ratio select. **Display Duty Ratio** — **1/24**: DS1 L, DS2 L, DS3 L; **1/12**: DS1 H, DS2 L, DS3 L; **X**: DS1 L, DS2 H, DS3 L; **1/32**: DS1 H, DS2 H, DS3 L; **1/16**: DS1 H, DS2 L, DS3 H; **1/8**: DS1 H, DS2 H, DS3 H
FS	1	I	Frequency select. The relationship between the frame frequency f_{FRM} and the oscillation frequency f_{OSC} is as follows: FS = High: $f_{OSC} = 6144 \times f_{FRM}$ (1) FS = Low: $f_{OSC} = 3072 \times f_{FRM}$ (2) Example (1) When FS = high, adjust Rf and Cf so that the oscillation frequency is approx. 430 kHz if the frame frequency is 70 Hz. Example (2) When FS = low, adjust Rf and Cf so that the oscillation is approx. 215 kHz, in order to obtain the same display waveforms as example 1. When compared with example 1, the power dissipation is reduced because of operation at lower frequency. However, the operating clocks $\phi 1$ and $\phi 2$ supplied to the column driver have lower frequencies. Therefore, the access time of the column driver HD44102CH becomes longer.
DL, DR	2	I/O	Data I/O terminals of bidirectional shift register.
SHL	1	I	Shift direction select of bidirectional shift register. **SHL** — **Shift Direction**: H: DL → DR; L: DL ← DR

Pin Name	Pin Number	I/O	Function
M/S	1	I	Master/slave select. M/S = High: Master mode The oscillator and timing generation circuit supply display timing signals to the display system. Each of I/O common terminals, DL, DR, M, and CL is placed in the output state. M/S = Low: Slave mode The timing generation circuit stops operating. The oscillator is not required. Connect terminal CR to V_{CC}. Open terminals C and R. One (determined by SHL) of DL and DR, and terminals M and CI are placed in the input state. Connect M, CL and one of DL and DR of the master to the respective terminals. Connect FD, DS1, DS2, and DS3 to V_{CC}. When display duty ratio is 1/8, 1/12, or 1/16, one HD44103CH is required. Use it in the master mode. When display duty ratio is 1/24 or 1/32, two HD44103CHs are required. Use the one in the master mode to drive common signals 1 to 20, and the other in the slave mode to drive common signals 21 to 24 (32).
ϕ1, ϕ2	2	O	Operating clock output terminals for HD44102CH. The frequencies of ϕ1 and ϕ2 become half of oscillation frequency.
V1, V2, V5, V6	4		Liquid crystal display driver level power supply. V1 and V2: Selected level V5 and V6: Non-selected level
V_{CC} GND V_{EE}	3		Power supply. V_{CC}–GND:Power supply for internal logic V_{CC}–V_{EE}: Power supply for driver circuit logic

Block Functions

Oscillator

The oscillator is a CR oscillator attached to an oscillation resistor Rf ans osckllation capacity Cf. The oscillation frequency varies with the values of Rf and Cf and the mounting conditions. Refer to Electrical Characteristics (Note 10) to make proper adjustment.

Timing Genaration Circuit

The timing generation circuit divides the signals from the oscillator and generates display timing signals (M, CL, and FRM) and operating clock (ϕ1 and ϕ2) for HD44102CH according to the display duty ratio set by DS1 to DS3. In the slave mode, this block stops operating. It is meaningless to set FS, DS1 to DS3. However, connect them to V_{CC} to prevent floating current.

Bidirectional Shift Register

20-bit bidirectional shift register. The shift direction is determined by SHL. The data input from DL or DR performs a shift operation at the rise of shift clock CL.

Liquid Crystal Display Driver Circuit

Each of 20 driver circuits is a multiplex circuit composed of four CMOS switches. The combination of the data from the shift register with M signal allows one of the four liquid crystal display driver levels V1, V2, V5, and V6 to be transferred to the output terminals.

Applications

Refer to the applications of the HD44102CH.