EM78P257

8-BIT MICRO-CONTROLLER

Version 1.4

Specification Revision History		
Version	***Content***	
1.0	*Initial version*	*05/06/2002*
1.1	*To add AKM/BKM Package type, RC Drift Rate, DC and AC Electrical Characteristic*	*03/18/2003*
1.2	*To remove BKM Package type, Change Power on reset content*	*06/27/2003*
1.3	*To add AC, DC curve*	*05/23/2004*
1.4	*To remove prescalers from TCCA, TCCB and TCCC*	*07/27/2004*

Application Note

AN-001 EM78P257 Firmware programming for Mouse, Comparator, IR and Change Interrupt, Internal C, External R Oscillation Mode Application Note

AN-002 EM78P257 applied by Comparator, IR ourput and Mouse separately

1. GENERAL DESCRIPTION

EM78P257A/B is an 8-bit microprocessors with low-power, high speed CMOS technology. It features a 2K*13 bits Electrical One Time Programmable Read Only Memory (OTP-ROM) and provides a protect bit to prevent from intruding on code, as well as 12 Option bits to accommodate user' s requirements.

2. FEATURES

- Operating voltage range: 2.3V~5.5V
- Operating temperature range: 0°C~70°C
- Operating frequency range: (Base on 2 clocks)
  - *** Crystal mode: DC ~ 20MHz/2clks,5V; DC ~ 8MHz/2clks,3V**
  - *** RC mode: DC ~ 4MHz/2clks,5V; DC ~ 4MHz/2clks,3V**
- Low power consumption:
  - *** less then 1.5 mA at 5V/4MHz**
  - *** typical of 15 μA, at 3V/32KHz**
  - *** typical of 1 μA, during the sleep mode**
- Built-in RC oscillator(4MHz,1MHz,455KHz,32.768KHz)
- RC oscillator mode with Internal Capacitor
- Programmable oscillator set-up time (1ms:18ms)
- Independent Programmable prescaler of WDT.
- One configuration register to match the user' s requirements, and provide user' s ID code for customer use
- 80× 8 on chip registers (SRAM, general purpose register)
- 2K× 13 on chip ROM
- Bi-directional I/O ports.
- 8 level stacks for subroutine nesting
- 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt.
- 4 sets of comparators.
- Easy-implemented IR (Infrared remote control) application circuit.
- Easy-implemented MOUSE application circuit.
- Power down (SLEEP) mode
- Five interrupt sources
  - *** TCC overflow interrupt**
  - *** Input-port status changed interrupt(wake up from the sleep mode)**
  - *** External interrupt**
  - *** IR OUT interrupt**
  - *** Comparators status change interrupt**
- Programmable free running watchdog timer
- 8 programmable pull-high I/O pins

- 8 programmable open-drain I/O pins
- 8 programmable pull-down I/O pins.
- Two clocks per instruction cycle.
- Package types:

  *** 18 pin DIP 300mil : EM78P257AP**

  *** 20 pin DIP 300mil : EM78P257BP**

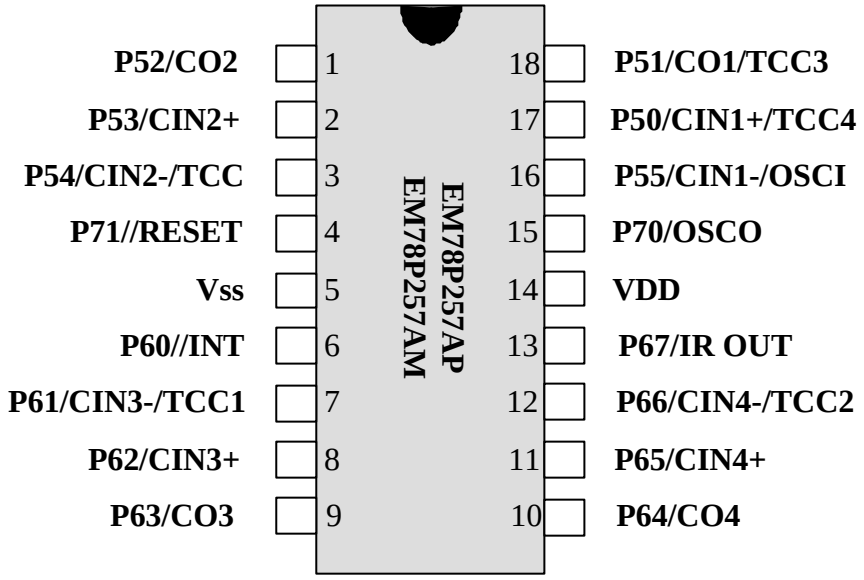
  *** 18 pin SOP 300mil : EM78P257AM**

  *** 20 pin SOP 300mil : EM78P257BM**

  *** 20 pin SSOP 209mil : EM78P257AKM**

- Power on voltage detector available for both EM78P257A and EM78P257B.

3. PIN ASSIGNMENT



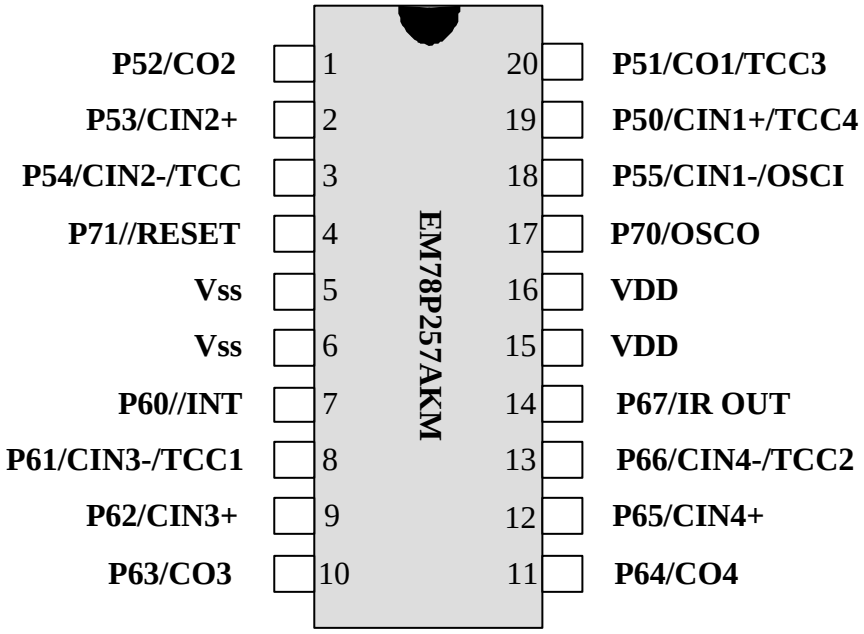


Fig. 1 Pin Assignment - EM78P257AP/AM/AKM

Table 1 Pin Description- EM78P257AP/AM

Symbol	Pin No.	Type	Function
VDD	14	-	Power supply.
OSCI	16	I	* XTAL type: Crystal input terminal or external clock input pin. * RC type: RC oscillator input pin.
OSCO	15	I/O	* XTAL type: output terminal for crystal oscillator or external clock input pin. * RC type: clock output with a duration of one instruction cycle. * External clock signal input.
P70~P71	4,15	I/O	* General purpose I/O pin. (P71 is input pin only) * Default value after a power on reset.
P60~P67	6~13	I/O	* General purpose I/O pin. * Open_drain * Default value after a power on reset.
P50~P55	1~3 16~18	I/O	* General purpose I/O pin. * Pull_high/pull_down. * Wake up from sleep mode when the status of the pin changes. * Default value after a power on reset.
IR OUT	13	O	* IR mode output pin, capable of sinking 20mA
/INT	6	I	* External interrupt pin triggered by falling edge.
CIN1-,CIN1+ CIN2-,CIN2+ CIN3-,CIN3+ CIN4-,CIN4+ CO1,CO2 CO3,CO4	16,17 3,2 7,8 12,11 18,1 9,10	I I I I O O	* “-“ -> the input pin of Vin- of a comparator. * “+” -> the input pin of Vin+ of a comparator. * Pin CO1~4 are the outputs of the comparators.
TCC TCC1,TCC2, TCC3,TCC4	3 ,7,12 18,17	I	* External Counter input.
/RESET	4	I	* If set as /RESET and remains at logic low, the device will be reset. * Voltage on /RESET/Vpp must not exceed Vdd during the normal mode. * Pull_high is on if defined as /RESET.
VSS	5	-	Ground.

Table 2 Pin Description- EM78P257AKM

Symbol	Pin No.	Type	Function
VDD	15,16	-	Power supply.
OSCI	18	I	* XTAL type: Crystal input terminal or external clock input pin. * RC type: RC oscillator input pin.
OSCO	17	I/O	* XTAL type: output terminal for crystal oscillator or external clock input pin. * RC type: clock output with a duration of one instruction cycle. * External clock signal input.
P70,P71	17,4	I/O	* General purpose I/O pin. (P71 is input pin only) * Default value after a power on reset.
P60~P67	7~14	I/O	* General purpose I/O pin. * Open_drain. * Default value after a power on reset.
P50~P55	1~3 18~20	I/O	* General purpose I/O pin. * Pull_high/pull_down.

			* Wake up from sleep mode when the status of the pin changes. * Default value after a power on reset.
IR OUT	14	O	* IR mode output pin, capable of sinking 20mA
/INT	7	I	* External interrupt pin triggered by falling edge.
CIN1-, CIN1+ CIN2-, CIN2+ CIN3-, CIN3+ CIN4-, CIN4+ CO1,CO2 CO3,CO4	18,19 3,2 8,9 13,12 20,1 10,11	I I I I O O	* " -" -> the input pin of Vin- of a comparator. * " +" -> the input pin of Vin+ of a comparator. * Pin CO1~4 are the outputs of the comparators.
TCC TCC1,TCC2 TCC3,TCC4	3 8,13 20,19	I	External Counter input.
/RESET	4	I	* If set as /RESET and remains at logic low, the device will be reset. * Voltage on /RESET/Vpp must not exceed Vdd during the normal mode. * Pull_high is on if defined as /RESET.
VSS	5,6	-	Ground.

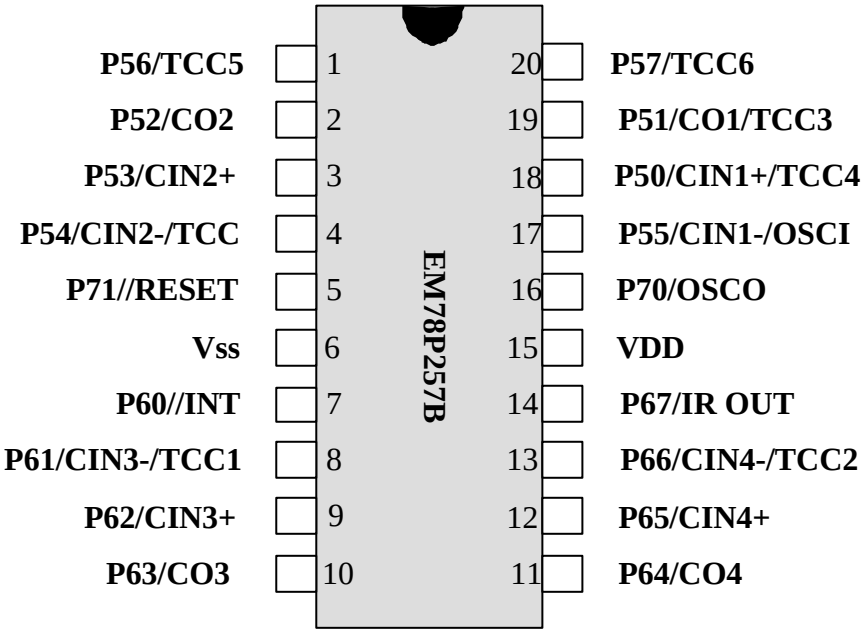


Fig. 2 Pin Assignment - EM78P257BP/BM

Table 3 Pin Description-EM78P257BP/BM/BKM

Symbol	Pin No.	Type	Function
VDD	15	-	Power supply.
OSCI	17	I	* XTAL type: Crystal input terminal or external clock input pin. * RC type: RC oscillator input pin.
OSCO	16	I/O	* XTAL type: output terminal for crystal oscillator or external clock input pin.

			* RC type: clock output with a duration of one instruction cycle. * External clock signal input.
P70,P71	16,5	I/O	* General purpose I/O pin. (P71 is input pin only) * Default value after a power on reset.
P60~P67	7~14	I/O	* General purpose I/O pin. * Open_drain. * Default value after a power on reset.
P50~P57	1~4 17~20	I/O	* General purpose I/O pin. * Pull_high/pull_down. * Wake up from sleep mode when the status of the pin changes. * Default value after a power on reset.
IR OUT	14	O	* IR mode output pin, capable of sinking 20mA
/INT	7	I	* External interrupt pin triggered by falling edge.
CIN1-, CIN1+ CIN2-, CIN2+ CIN3-, CIN3+ CIN4-, CIN4+ CO1,CO2 CO3,CO4	17,18 4,3 8,9 13,12 19,2 10,11	I I I I O O	* “-“ -> the input pin of Vin- of a comparator. * “+” -> the input pin of Vin+ of a comparator. * Pin CO1~4 are the outputs of the comparators.
TCC TCC1,TCC2 TCC3,TCC4 TCC5,TCC6	4 8,13 19,18 1,20	I	External Counter input.
/RESET	5	I	* If set as /RESET and remains at logic low, the device will be reset. * Voltage on /RESET/Vpp must not exceed Vdd during the normal mode. * Pull_high is on if defined as /RESET.
VSS	6	-	Ground.

4. FUNCTION DESCRIPTION

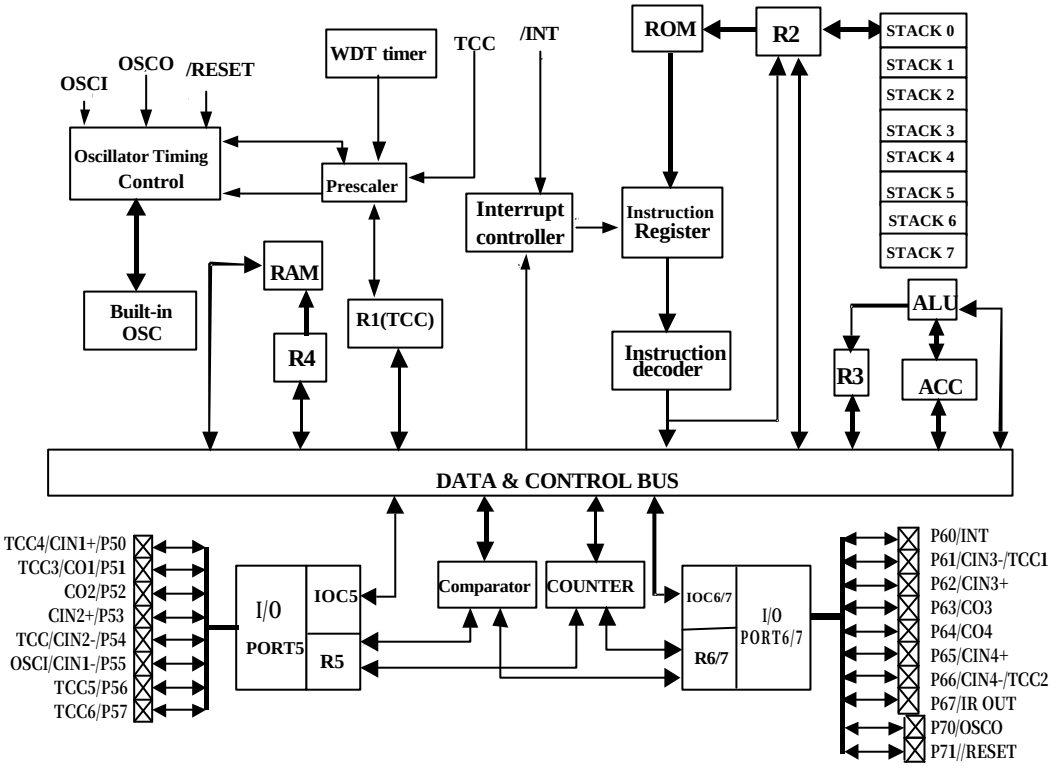


Fig. 3 Functional block diagram

4.1 Operational Registers

1. R0 (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to be an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

2. R1 (Time Clock /Counter)/TCC

- Increased by an external signal edge which is defined by the TE bit (CONT-4) through the TCC pin, or by the instruction cycle clock.
- Writable and readable as any other registers.
- The prescaler (RC) is assigned to TCC.
- The contents of the prescaler counter is cleared only when a value is written to TCC register.

3. R2 (Program Counter) & Stack/PC

- Depending on the device type, R2 and hardware stack are 11-bits wide. The structure is depicted in Fig. 4.
- Generates 2K×13 on-chip ROM addresses to the relative programming instruction codes. One program page is 1K words long.
- R2 is set as all "0"s when under RESET condition.
- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows PC go to any location within a page.
- "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.
- "ADD R2,A" allows the contents of ' A' to be added to the current PC, and the ninth and tenth bits of the PC are cleared.
- "MOV R2,A" allows to load an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits of the PC are cleared.
- Any instruction that is written to R2 (e.g. "ADD R2,A", "MOV R2,A", "BC R2,6",····) will cause the ninth and tenth bits (A8~A9) of the PC to be cleared. Thus, the computed jump is limited to the first 256 locations of a page.
- In case of EM78P257A/B, the second most significant bit(A10) will be loaded with the content of bit PS0 in the status register (R3) upon the execution of a "JMP", "CALL", or any other instructions which write to R2.
- All instructions are single cycle (fclk/2 or fclk/4), except for the instructions that would change the contents of R2. This instruction will need one more instruction cycle.

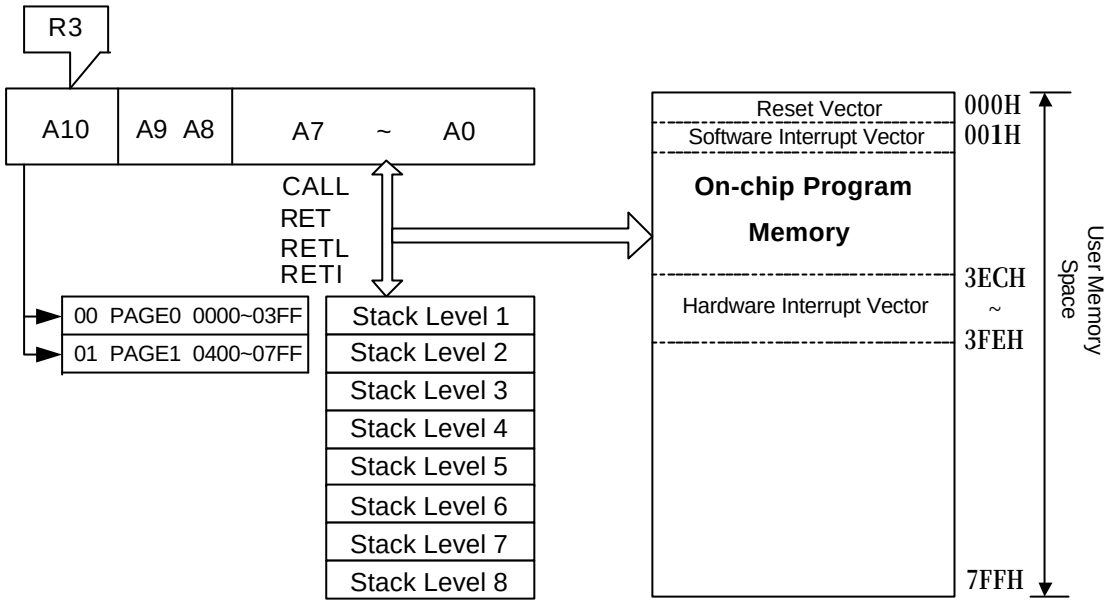


Fig. 4 Program counter organization

Address	R PAGE registers	IOCX0 PAGE registers	IOCX1 PAGE registers
00	**R0** (Indirect Addressing Register)	Reserve	Reserve
01	**R1** (Time Clock Counter)	**CONT** (Control Register)	Reserve
02	**R2** (Program Counter)	Reserve	Reserve
03	**R3** (Status Register)	Reserve	Reserve
04	**R4** (RAM Select Register)	Reserve	Reserve
05	**R5** (Port5)	**IOC50** (I/O Port Control Register)	**IOC51** (TCCA Counter)
06	**R6** (Port6)	**IOC60** (I/O Port Control Register)	**IOC61** (TCCBL Counter)
07	**R7** (Port7)	**IOC70** (I/O Port Control Register)	**IOC71** (TCCBH Counter)
08	Reserve	**IOC80** (TCC Control Register)	**IOC81** (TCCC Counter)
09	**R9** (CMPOUT Status Register & TCC Status Register)	**IOC90** (CMP Control Register)	**IOC91** (Low-time Register)
0A	**RA** (TCC Control Register(1))	**IOCA0** (CO-Input Combine sequence)	**IOCA1** (High-time Register)
0B	**RB** (TCC Control Register(2))	**IOCB0** (Pull-down Control Register)	**IOCB1** (Pulse time Register)
0C	**RC** (TCC Prescaler Register)	**IOCC0** (Open-drain Control Register)	Reserve
0D	**RD** (IR Control Register)	**IOCD0** (Pull-high Control Register)	Reserve
0E	**RE** (Mouse Control Register)	**IOCE0** (WDT Control Register)	Reserve
0F	**RF** (Interrupt Status Register)	**IOCF0** (Interrupt Mask Register)	Reserve
10 : 1F	General Registers		
20 : 3F	Bank0	Bank1	

Fig. 5 Data memory configuration

4. R3 (Status Register)

7	6	5	4	3	2	1	0
RST	IOCS	PS0	T	P	Z	DC	C

- **Bit 7 (RST)** Bit for reset type.

  Set to 1 if wake-up from sleep on pin change or comparator status change.

  Set to 0 if wake-up from other reset types

- **Bit6 (IOCS)** Select the Segment of the control register.

  0 = Segment 0(IOC50~IOCF0) selected;

  1 = Segment 1(IOC51~IOCC1) selected;

- **Bit5 (PS0)** Page select bits. PS0 is used to select a program memory page. When executing a "JMP", "CALL", or other instructions that causes the program counter to change (e.g. MOV R2,A), PS0 is loaded into the 11th bit of the program counter, selecting one of the available program memory pages. Note that RET (RETL, RETI) instruction does not change the PS0 bits. That is, the return will always be back to the page from where the subroutine was called, regardless of the current PS0 bit setting.

PS0	Program memory page [Address]
0	Page 0 [000-3FF]
1	Page 1 [400-7FF]

- **Bit 4 (T)** Time-out bit.

  Set to 1 with the "SLEP" and "WDTC" command, or during power on and reset to 0 by WDT time-out.

- **Bit 3 (P)** Power down bit.

  Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

- **Bit 2 (Z)** Zero flag.

  Set to "1" if the result of an arithmetic or logic operation is zero.

- **Bit 1 (DC)** Auxiliary carry flag.
- **Bit 0 (C)** Carry flag.

5. R4 (RAM Select Register)

- The Bit7 set to "0" as all time.
- Bit 6 is used to select bank 0 or bank 1.
- Bits 5~0 are used to select a register (address: 00~0F, 10~3F) in the indirect addressing mode.
- See the configuration of the data memory in Fig. 5.

6. R5 ~ R6 (Port 5 ~ Port 6)

- R5 and R6 are I/O registers.
- Only the lower 6 bits of R5 are available.(applicable to EM78P257A)
- The upper 2 bits of R5 are fixed to 0. (if EM78P257A is selected)

7. R7 (Port 7)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	I/O	I/O

- R7 is I/O registers.
- Only the lower 2 bits of R7 are available.

8. R9 (CMPOUT Status Register & TCC Status Register)

7	6	5	4	3	2	1	0
CMPOUT4	CMPOUT3	CMPOUT2	CMPOUT1	-	TCCCIF	TCCBIF	TCCAIF

- **Bit 7(CMPOUT4)** The output result of the comparator4.
- **Bit 6(CMPOUT3)** The output result of the comparator3.
- **Bit 5(CMPOUT2)** The output result of the comparator2.
- **Bit 4(CMPOUT1)** The output result of the comparator1.
- Bit 4~Bit 7 are read only.
- **Bit 3** Not used, read as' 0' .
- **Bit 2(TCCCIF)** TCCC overflowing interrupt flag. Set when TCCC overflow, reset by software.
- **Bit 1(TCCBIF)** TCCB overflowing interrupt flag. Set when TCCB overflow, reset by software.
- **Bit 0 (TCCAIF)** TCCA overflowing interrupt flag. Set when TCCA overflow, reset by software.

9. RA (TCC Control Register (1))

7	6	5	4	3	2	1	0
-	-	-	-	-	TCCAIE	-	-

- **Bit 7~Bit 3** Not used, read as ' 0' .
- **Bit 2(TCCAIE)** TCCAIF interrupt enable bit.

  0: disable TCCAIF interrupt

  1: enable TCCAIF interrupt
- **Bit 1** Set to "0" as all time.
- **Bit 0** Not used.

10. RB (TCC Control Register (2))

7	6	5	4	3	2	1	0
-	TCCBIE	-	-	-	TCCCIE	-	-

- **Bit 7** Not used.
- **Bit 6(TCCBIE)** TCCBIF interrupt enable bit.

  0: disable TCCBF interrupt

  1: enable TCCBIF interrupt
- **Bit 5** Set to "0" as all time.
- **Bit 4~3** Not used.
- **Bit 2(TCCCIE)** TCCCIF interrupt enable bit.

  0: disable TCCCIF interrupt

  1: enable TCCCIF interrupt
- **Bit 1** Set to "0" as all time.
- **Bit 0** Not used.

11. RC (TCC Prescaler Counter)

TCC prescaler counter can be read and written.

PSR2	PSR1	PSR0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	TCC Rate
0	0	0	-	-	-	-	-	-	-	V	1:2
0	0	1	-	-	-	-	-	-	V	V	1:4
0	1	0	-	-	-	-	-	V	V	V	1:8
0	1	1	-	-	-	-	V	V	V	V	1:16
1	0	0	-	-	-	V	V	V	V	V	1:32
1	0	1	-	-	V	V	V	V	V	V	1:64
1	1	0	-	V	V	V	V	V	V	V	1:128
1	1	1	V	V	V	V	V	V	V	V	1:256

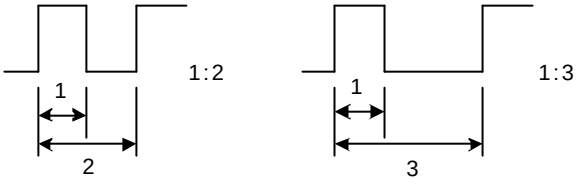
*V: valid value

12. RD (IR Control Register)

7	6	5	4	3	2	1	0
DP1	DP0	MF1	MF0	IRE	HF	LGP	PWM

- **Bit 7: Bit 6 (DP1:DP0)** : Ratios of duty and period of modulated frequency

DP1	DP0	Ratio
0	0	1:2(default)
0	1	1:3
1	0	1:4
1	1	-



- **Bit 5: Bit 4 (MF1:MF0)** : Modulated frequency

MF1	MF0	Fosco
0	0	Fosc/1
0	1	-
1	0	Fosc/4
1	1	Fosc/8

- **Bit 3(IRE)** Infrared Remote Enable bit

  0: Disable IRE. Disable H/W Modulator Function.

  1: Enable IRE. Disable RB (Bit4(TCCBTE) and Bit5(TCCBTS)), and TCCBX acts as a down counter. Enable H/W Modulator Function. Pin 67 defined as IR OUT.

- **Bit 2(HF)** High Frequency. When HF = 1; the Low-time part of the generated pulse is modulated with a frequency Fosco.

- **Bit 1(LGP)** Long Pulse. When LGP = 1, the contents of the High-time register are ignored. A single pulse is generated; its pulse is high.

  Pulse width = (Contents of Low-time register) x (number of pulse) x (1/Fosc)

  If HF = 1, this pulse is modulated with a frequency Fosco (selected by MF1, MF0).

- **Bit 0(PWM)** Pulse Width Modulation. When PWM = 1 and LGP = 0, the LSB Counter and MSB Counter are disabled, a continuous pulse train is generated, and the output signal is actually a PWM waveform format of PWM.

13. RE (Mouse Control Register)

7	6	5	4	3	2	1	0
MOUSEN	-	-	-	-	-	-	-

- **Bit 7 (MOUSEN)** Mouse application Enable bit.

  0: Disable MOUSEN. TCCA, TCCB and TCCC are increment counters.

  1: Enable MOUSEN. TCCA, TCCBL and TCCC work as up/down counters. The other pin assignment refers to IOC80 and IOC90.

- **Bit 6~Bit 0** Not used.

14. RF (Interrupt Status Register)

7	6	5	4	3	2	1	0
CMP4IF	CMP3IF	CMP2IF	CMP1IF	-	EXIF	ICIF	TCIF

"1" means interrupt request, and "0" means no interrupt occurs.

- **Bit 7 (CMP4IF)** Status changed interrupt flag. Set as change occurred in the output of Comparator CO4, and reset by software.
- **Bit 6 (CMP3IF)** Status changed interrupt flag. Set as change occurred in the output of Comparator CO3, and reset by software.
- **Bit 5 (CMP2IF)** Status changed interrupt flag. Set as change occurred in the output of Comparator CO2, and reset by software.
- **Bit 4 (CMP1IF)** Status changed interrupt flag. Set as change occurred in the output of Comparator CO1, and reset by software.
- **Bit 3** Unemployed, read as ' 0' ;
- **Bit 2 (EXIF)** External interrupt flag. Set by on /INT pin, and reset by software.
- **Bit 1 (ICIF)** Port 5 input status changed interrupt flag. Set when Port 5 input changes, and reset by software.
- **Bit 0 (TCIF)** TCC overflowing interrupt flag. Set when TCC overflows, and reset by software.
- RF can be cleared by instruction but cannot be set.
- IOCF0 is the relative interrupt mask register.

15. R10 ~ R3F

- All of these are the 8-bit general purpose registers.

4.2 Special Purpose Registers

1. A (Accumulator)

- Internal data transfer, or instruction operand holding
- It can not be addressed.

2. CONT (Control Register)

7	6	5	4	3	2	1	0
INTE	INT	TS	TE	-	PSR2	PSR1	PSR0

- **Bit 7 (INTE)** INT signal edge

  0: interrupt occurs at the rising edge on the INT pin

  1: interrupt occurs at the falling edge on the INT pin

- **Bit 6 (INT)** Interrupt enable

  0: masked by DISI or hardware interrupt

  1: enabled by ENI/RETI instructions

- **Bit 5 (TS)** TCC signal source

  0: internal instruction cycle clock

  1: transition on TCC pin

- **Bit 4 (TE)** TCC signal edge

  0: increment if the transition from low to high takes place on TCC pin

  1: increment if the transition from high to low takes place on TCC pin\

- **Bit 3** Not used.

- **Bit 2 (PSR2) ~ Bit 0 (PSR0)** TCC prescaler bits.

PSR2	PSR1	PSR0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

- The CONT register is both readable and writable.
- Bit 6 is read only.

3. IOC50 ~ IOC70 (I/O Port Control Registers)

- "1" put the relative I/O pin into high impedance, while "0" defines the relative I/O pin as output.
- Only the higher 2 bits of IOC5 can be defined. (for EM78P257B only)
- Only the lower 2 bits of IOC7 can be defined, the others bits are not available.

• IOC5 , IOC6 and IOC7 are both readable and writable.

4. IOC80 (TCC Control Register):

7	6	5	4	3	2	1	0
TCC2E	TCC4E	TCC6E	TCCBE	-	-	-	-

• **Bit 7 (TCC2E):** Control bit used to enable the second input of counter

For EM78P257A

1 = If MOUSEN equal to ‘ 1’ , pin 12 is defined as another input pin of TCCA. If MOUSEN equal to ‘ 0’ , pin 12 is a bi-directional I/O pin.

0 = Define P66 as a bi-directional I/O pin.

For EM78P257B

1 = If MOUSEN equal to ‘ 1’ , pin 13 is defined as another input pin of TCCA. If MOUSEN equal to ‘ 0’ , pin 13 is a bi-directional I/O pin.

0 = Define P66 as a bi-directional I/O pin.

• **Bit 6 (TCC4E):** Control bit used to enable the second input of counter

For EM78P257A

1 = If MOUSEN equal to ‘ 1’ , pin 17 is defined as another input pin of TCCB. If MOUSEN equal to ‘ 0’ , pin 17 is a bi-directional I/O pin.

0 = Define P50 as a bi-directional I/O pin.

For EM78P257B

1 = If MOUSEN equal to ‘ 1’ , pin 18 is defined as another input pin of TCCB. If MOUSEN equal to ‘ 0’ , pin 18 is a bi-directional I/O pin.

0 = Define P50 as a bi-directional I/O pin.

• **Bit 5 (TCC6E):** Control bit used to enable the second input of counter (for EM78P257B only)

For EM78P257B

1 = If MOUSEN equal to ‘ 1’ , pin 20 is defined as another input pin of TCCC. If MOUSEN equal to ‘ 0’ , pin 20 is a bi-directional I/O pin.

0 = Define P57 as a bi-directional I/O pin.

• **Bit 4 (TCCBE):** Control bit is used to enable the most significant byte of counter

1 = Enable the most significant byte of TCCBH. TCCB is a 16-bits counter.

0 = Disable the most significant byte of TCCBH (default value). TCCB is an 8-bits counter.

• **Bit 3~Bit 0** Not used.

5. IOC90 (CMP Control Register):

7	6	5	4	3	2	1	0
COIE4	COIE3	COIE2	COIE1	CE4	CE3	CE2	CE1

- **Bit 7 (COIE7):** Set P64 as the output of the comparator CO4(CE4 must be enabled)

  1 = output enabled;

  0 = output disabled, and carry out the function of P64.

- **Bit 6 (COIE3):** Set P63 as the output of the comparator CO3(CE3 must be enabled)

  1 = output enabled;

  0 = output disabled, and carry out the function of P63.

- **Bit 5 (COIE2):** Set P52 as the output of the comparator CO2(CE2 must be enabled)

  1 = output enabled;

  0 = output disabled, and carry out the function of P52.

- **Bit 4 (COIE1):** Set P51 as the output of the comparator CO1 (CE1 must be enabled)

  1 = output enabled;

  0 = output disabled, and carry out the function of P51.

- **Bit 3 (CE4):** Comparator **(CO4)** enable bit

  0 = Comparator is CO4 off (default value).

  For EM78P257A

  Pin 10 can choice P64 only.

  Pin 11 can choose P65 only.

  Pin 12 can choose P66 or TCC2 only. If MOUSEN is ‘ 1’ and TCC2E of IOC80 is also ‘ 1’ , then set pin to TCC2, otherwise set to P66.

  For EM78P257B

  Pin 11 can choose P64 only.

  Pin 12 can choose P65 only.

  Pin 13 can choose P66 or TCC2 only. If MOUSEN is ‘ 1’ and TCC2E of IOC80 is ‘ 1’ also, then set pin to TCC2, otherwise set to P66.

  1 = Comparator is CO4 on.

  For EM78P257A

  Pin 10 can choose P64 or CO4 only, and decided by COIE4 of IOC90.

  Pin 11 can choose CIN4+ only.

Pin 12 can choose P66 ,CIN4- or TCC2, and the choice is decided by IOCA0. If CIN4- was not chosen as comparator1(-) input, this pin will decide to set MOUSEN as ‘ 1’ and TCC2E of IOC80 is also set as ‘ 1’ , then set the pin to TCC2, otherwise set the pin to P66.

For EM78P257B

Pin 11 can choose P64 or CO4 only, and decided by COIE4 of IOC90.

Pin 12 can choose CIN3+ only.

Pin 13 can choose P66 ,CIN4- or TCC2, and the choice is decided by IOCA0. If CIN4- was not chosen as comparator1(-) input, this pin will decide to set MOUSEN as ‘ 1’ and TCC2E of IOC80 is also set as ‘ 1’ , then set the pin to TCC2, otherwise set the pin to P66.

- **Bit 2 (CE3):** Comparator **(CO3)** enable bit

0 = Comparator is CO3 off (default value).

For EM78P257A

Pin 9 can choose P63 only.

Pin 8 can choose P62 only.

Pin 7 can choose P61 or TCC1 only. If MOUSEN is ‘ 1’ , define pin as an input of TCCA (TCC1). If MOUSEN is ‘ 0’ , then the choice is decided by TCCATS of RA.

For EM78P257B

Pin 10 can choose P63 only.

Pin 9 can choose P62 only.

Pin 8 can choose P61 or TCC1 only. If MOUSEN is ‘ 1’ defined pin as an input of TCCA(TCC1) , if MOUSEN is ‘ 0’ , then the choice is decided by TCCATS of RA.

1 = Comparator is CO3 on.

For EM78P257A

Pin 9 can choose P63 or CO3 only, and decided by COIE3 of IOC90.

Pin 8 can choose CIN3+ only.

Pin 7 can choose P61 ,CIN3- or TCC1, and the choice is decided by IOCA0. If CIN3- was not chosen as comparator1(-) input, then this pin’ s status will be decided by TCCATS of RA. When TCCATS is ‘ 1’ , then Pin 7 is defined as TCC1, otherwise the status is defined as P61.

For EM78P257B

Pin 10 can choose P63 or CO3 only, and decided by COIE3 of IOC90.

Pin 9 can choose CIN3+ only.

Pin 8 can choose P61 ,CIN3- or TCC1, and is decided by IOCA0. If CIN3- was not chosen as comparator1(-) input, then this pin' s status will be decided by TCCATS of RA. When TCCATS is ' 1' , then Pin 8 is defined as TCC1, otherwise the status is defined as P61.

- **Bit 1 (CE2):** Comparator **(CO2)** enable bit

0 = Comparator is CO2 off (default value).

For EM78P257A

Pin 1 can choose P52 only.

Pin 2 can choose P53 only.

Pin 3 can choose P54 or TCC only, and is decided by Bit 5 of Control Register (CONT-5). When TS is ' 1' , then Pin 3 is defined as TCC, otherwise the status is defined as P54.

For EM78P257B

Pin 2 can choose P52 only.

Pin 3 can choose P53 only.

Pin 4 can choose P54 or TCC only, and is decided by Bit 5 of Control Register (CONT-5). When TS is ' 1' , then Pin 4 is defined as TCC, otherwise the status is defined as P54.

1 = Comparator is CO2 on.

For EM78P257A

Pin 1 can choose P52 or CO2 only, and decided by COIE2 of IOC90.

Pin 2 can choose CIN2+ only.

Pin 3 can choose P54 ,CIN2- or TCC, and is decided by IOCA0. If CIN2- was not chosen as comparator1(-) input, then this pin will be decided by Bit 5 of Control Register (CONT-5). When TS is ' 1' , then Pin 3 is defined as TCC, otherwise status is defined as P54.

For EM78P257B

Pin 2 can choose P52 or CO2 only, and decided by COIE2 of IOC90.

Pin 3 can choose CIN2+ only.

Pin 4 can choose P54 ,CIN2- or TCC as decided by IOCA0. If CIN2- was not chosen as comparator1(-) input, then this pin will be decided by Bit 5 of Control Register (CONT-5)**.** When TS is ' 1' , then Pin 4 is defined as TCC, otherwise status defined as P54.• **Bit 0 (CE1):** Comparator **(CO1)** enable bit

0 = Comparator CO1 is off (default value).

For EM78P257A

Pin 18 can choose P51 or TCC3 only. If MOUSEN is ' 1' , define as an input of TCCB (TCC3). If MOUSEN is ' 0' , then the choice is decided by TCCBTS of RB.

Pin 17 can choose P50 or TCC4 only. If MOUSEN is ' 1' and TCC4E of IOC80 is ' 1' also, then choose TCC4, otherwise choose P50.

Pin 16 can choose P55 or OSCI only, and the choice is decided by Bit 9,8,7 of CODE option. When choice is ' 1,1,1' , then Pin 16 is defined as P55, otherwise the status is defined as OSCI.

For EM78P257B

Pin 19 can choose P51 or TCC3 only. If MOUSEN is ' 1' , define as an input of TCCB (TCC3), if MOUSEN is ' 0' , then the choice is decided by TCCBTS of RB.

Pin 18 can choose P50 or TCC4 only. If MOUSEN is ' 1' and TCC4E of IOC80 is ' 1' also, then choose TCC4, otherwise choose P50.

Pin 17 can choose P55 or OSCI only, and the choice is decided by Bit 9,8,7 of CODE option. When choice is ' 1,1,1' , then Pin 17 is defined as P55, otherwise the status is defined as OSCI.

1 = Comparator CO1 is on.

For EM78P257A

Pin 18 can choose P51 or CO1 only, and the choice is decided by COIE1 of IOC90.

Pin 17 can choose CIN1+ only.

Pin 16 can choose P55 ,CIN1- or OSCI, and is decided by IOCA0. If CIN1- was not chosen as comparator1(-) input, then this pin' s status will be decided by Bit 9,8,7 of CODE option. When choice is ' 1,1,1' , then Pin 16 is defined as P55, otherwise the status is defined as OSCI.

For EM78P257B

Pin 19 can choose P51 or CO1 only, and the choice is decided by COIE1of IOC90.

Pin 18 can choose CIN1+ only.

Pin 17 can choose P55 ,CIN1- or OSCI, and is decided by IOCA0. If CIN1- was not chosen as comparator1(-) input, then this pin' s status will be decided by Bit 9,8,7 of CODE option. When choice is ' 1,1,1' , then Pin 17 is defined as P55, otherwise the status is defined as OSCI.

6. IOCA0 (CO- INPUT Combine sequence)

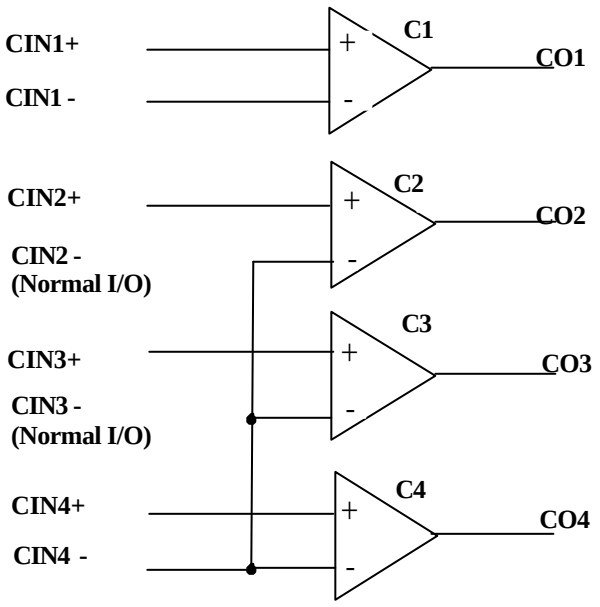
• There are 16 combinations of the negative inputs of the four comparators.

7	6	5	4	3	2	1	0
-	-	-	-	CI3	CI2	CI1	CI0

Table 4 The list of CO-INPUT combine sequence

CI3	CI2	CI1	CI0	CO- Input combine status	Comment
0	0	0	0	N/A	1,2,3, and 4 -> negative inputs,
0	0	0	1	1,2	CIN2- -> negative input; CIN1- -> normal I/O pin;
0	0	1	0	1,3	CIN3- -> negative input; CIN1- -> normal I/O pin;
0	0	1	1	1,4	CIN4- -> negative input; CIN1- -> normal I/O pin;
0	1	0	0	2,3	CIN3- -> negative input; CIN2- -> normal I/O pin;
0	1	0	1	2,4	CIN4- -> negative input; CIN2- -> normal I/O pin;
0	1	1	0	3,4	CIN4- -> negative input; CIN3- -> normal I/O pin;
0	1	1	1	1,2,3	CIN3- -> negative input; CIN(1,2)- -> normal I/O pin;
1	0	0	0	1,2,4	CIN4- -> negative input; CIN(1,2)- -> normal I/O pin;
1	0	0	1	1,3,4	CIN4- -> negative input; CIN(1,3)- -> normal I/O pin;
1	0	1	0	2,3,4	CIN4- -> negative input; CIN(2,3)- -> normal I/O pin;
1	0	1	1	1,2,3,4	CIN4- -> negative input; CIN(1,2,3)- -> normal I/O pin;
1	1	0	0	3,2	CIN2- -> negative input; CIN3- -> normal I/O pin;
1	1	0	1	4,2	CIN2- -> negative input; CIN4- -> normal I/O pin;
1	1	1	0	4,3,2	CIN2- -> negative input; CIN(3,4)- -> normal I/O pin;
1	1	1	1	1,4,3	CIN3- -> negative input; CIN(1,4)- -> normal I/O pin;

Example: (CI3,CI2,CI1,CI0)= (1010) => Comparator 4(-) combined together with Comparator 3(-) and Comparator 2(-), and both CIN2- and CIN3- work as normal I/O pins.



7. IOCB0 (Pull-down Control Register)

7	6	5	4	3	2	1	0
/PD57	/PD56	/PD55	/PD54	/PD53	/PD52	/PD51	/PD50

- **Bit 7 (/PD57)** Control bit is used to enable the pull-down of P57 pin. (for EM78P257B only)

  0: Enable internal pull-down

  1: Disable internal pull-down

- **Bit 6 (/PD56)** Use to enable the pull-down of P56 pin. (for EM78P257B only)
- **Bit 5 (/PD55)** Use to enable the pull-down of P55 pin.
- **Bit 4 (/PD54)** Use to enable the pull-down of P54 pin.
- **Bit 3 (/PD53)** Use to enable the pull-down of P53 pin.
- **Bit 2 (/PD52)** Use to enable the pull-down of P52 pin.
- **Bit 1 (/PD51)** Use to enable the pull-down of P51 pin.
- **Bit 0 (/PD50)** Use to enable the pull-down of P50 pin.
- IOCB0 Register is both readable and writable.

8. IOCC0 (Open-drain Control Register)

7	6	5	4	3	2	1	0
OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60

- **Bit 7 (OD67)** Use to enable the open-drain of P67 pin.

  0: Disable open-drain output

  1: Enable open-drain output
- **Bit 6 (OD66)** Use to enable the open-drain of P66 pin.
- **Bit 5 (OD65)** Use to enable the open-drain of P65 pin.
- **Bit 4 (OD64)** Use to enable the open-drain of P64 pin.
- **Bit 3 (OD63)** Use to enable the open-drain of P63 pin.
- **Bit 2 (OD62)** Use to enable the open-drain of P62 pin.
- **Bit 1 (OD61)** Use to enable the open-drain of P61 pin.
- **Bit 0 (OD60)** Use to enable the open-drain of P60 pin.
- IOCC0 Register is both readable and writable.

9. IOCD0 (Pull-high Control Register)

7	6	5	4	3	2	1	0
/PH57	/PH56	/PH55	/PH54	/PH53	/PH52	/PH51	/PH50

- **Bit 7 (/PH57)** Use to enable the pull-high of P57 pin. (for EM78P257B only)

  0: Enable internal pull-high

  1: Disable internal pull-high
- **Bit 6 (/PH56)** Use to enable the pull-high of P56 pin. (for EM78P257B only)
- **Bit 5 (/PH55)** Use to enable the pull-high of P55 pin.
- **Bit 4 (/PH54)** Use to enable the pull-high of P54 pin.
- **Bit 3 (/PH53)** Use to enable the pull-high of P53 pin.
- **Bit 2 (/PH52)** Use to enable the pull-high of P52 pin.
- **Bit 1 (/PH51)** Use to enable the pull-high of P51 pin.

- **Bit 0 (/PH50)** Use to enable the pull-high of P50 pin.
- IOCD0 Register is both readable and writable.

10. IOCE0 (WDT Control Register)

7	6	5	4	3	2	1	0
WDTE	EIS	-	-	-	PSW2	PSW1	PSW0

- **Bit 7 (WDTE)** Control bit is used to enable Watchdog timer.

  0: Disable WDT.

  1: Enable WDT.

  WDTE is both readable and writable.

- **Bit 6 (EIS)** Control bit is used to define the function of P60(/INT) pin.

  0: P60, bi-directional I/O pin.

  1: /INT, external interrupt pin. In this case, the I/O control bit of P60 (bit 0 of IOC6) must be set to "1". When EIS is "0", the path of /INT is masked. When EIS is "1", the status of /INT pin can also be read by way of reading Port 6 (R6). Refer to Fig. 8.

  EIS is both readable and writable.

- **Bit5~3** Not used.
- **Bit 2 (PSW2) ~ Bit 0 (PSW0)** WDT prescaler bits.

PSW2	PSW1	PSW0	WDT Rate
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:32
1	1	0	1:64
1	1	1	1:128

11. IOCF0 (Interrupt Mask Register)

7	6	5	4	3	2	1	0
CMP4IE	CMP3IE	CMP2IE	CMP1IE	PPC/CMP	EXIE	ICIE	TCIE

- **Bit 7 (CMP4IE)** CMP3IF interrupt enable bit.

  0: disable CMP4IF interrupt

  1: enable CMP4IF interrupt

- **Bit 6 (CMP3IE)** CMP3IF interrupt enable bit.

  0: disable CMP3IF interrupt

  1: enable CMP3IF interrupt

- **Bit 5 (CMP2IE)** CMP2IF interrupt enable bit.

0: disable CMP2IF interrupt

1: enable CMP2IF interrupt

- **Bit 4 (CMP1IE)** CMP1IF interrupt enable bit.

  0: disable CMP1IF interrupt

  1: enable CMP1IF interrupt

- **Bit 3 (CMP/PPC)** Wake-up by which Interrupt sources.

  0: PPC, wake-up by Port 5 input status change. (if enabled)

  1: CMP, wake-up by comparators status change. (if enabled)

- **Bit 2 (EXIE)** EXIF interrupt enable bit.

  0: disable EXIF interrupt

  1: enable EXIF interrupt

- **Bit 1 (ICIE)** ICIF interrupt enable bit.

  0: disable ICIF interrupt

  1: enable ICIF interrupt

- **Bit 0 (TCIE)** TCIF interrupt enable bit.

  0: disable TCIF interrupt

  1: enable TCIF interrupt

- Individual interrupt is enabled by setting its associated control bit in the IOCF0 to "1".
- Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Fig. 10.
- IOCF0 register is both readable and writable.

12. IOC51 (TCCA Counter)

An eight-bit clock counter. It can be read, written and cleared on any reset condition. When in Mouse-Mode, it is Up/Down Counter, else it is UP Counter.

13. IOC61 (TCCBL Counter) /LSB Counter

An eight-bit clock counter is for the least significant byte of TCCBX. TCCBL. It can be read, written and cleared on any reset condition. When in Mouse-Mode, it is Up/Down Counter; When in IR-Mode, it is Down Counter, else it is Up Counter.

14. IOC71 (TCCBH Counter) /MSB Counter

An eight-bit clock counter is for the most significant byte of TCCBX. TCCBH. It can be read, written and cleared on any reset condition. When TCCBE(IOC80) is "0" THEN TCCBH is disable, TCCBE is"1" then TCCB is 16 bit length counter. When it is in IR-Mode, it is Down Counter, else it is UP Counter.

15. IOC81 (TCCC Counter)

An eight-bit clock counter. It can be read, written and cleared on any reset condition. When in Mouse-Mode, it is Up/Down Counter, else it is UP Counter.

16. IOC91 (Low-time Register)

The 8-bit Low-time register controls the active or Low period of the pulse.

The decimal value of its contents determines the number of oscillator cycles and verifies that the IR OUT pin is active. The active period of IR OUT can be calculated as follows:

t_{Low}=(decimal value held in Low-time register)/fosc

17. IOCA1 (High-time Register)

The 8-bit High-time register controls the inactive or High period of the pulse.

The decimal value of its contents determines the number of oscillator cycles and verifies that the IR OUT pin is inactive. The inactive period of IR OUT can be calculated as follows:

t_{High}=(decimal value held in High-time register)/fosc

18. IOCB1 (Pulse timer Register)

The contents of the Low-time and High-time register are loaded alternately into the Pulse timer. When loaded, the contents of Pulse timer are decremented on every oscillator cycle. Upon reaching zero, the Pulse timer will be loaded with the contents of the other.

4.3 TCC/WDT & Prescaler

There are two 8-bit counters available as prescalers for the TCC and WDT respectively. The PSR0~PSR2 bits of the CONT register are used to determine the ratio of the prescaler of TCC. Likewise, the PWR0~PWR2 bits of the IOCE0 register are used to determine the prescaler of WDT. The prescaler (PSR0~PSR2) will be cleared by the instructions each time they are written into TCC. The WDT and prescaler will be cleared by the "WDTC" and "SLEP" instructions. Fig.6 depicts the circuit diagram of TCC/WDT.

- R1(TCC) is an 8-bit timer/counter. The clock source of TCC can be internal clock or external singal input (edge selectable from the TCC pin). If TCC signal source is from internal clock, TCC will increase by 1 at every instruction cycle (without prescaler). As illustrated in Fig. 6, selection of CLK=Fosc/2 or CLK=Fosc/4 depends on the CODE Option bit <CLKS>. CLK=Fosc/2 is selected if the CLKS bit is "0", and CLK=Fosc/4 is selected if the CLKS bit is "1". If TCC signal source is from external clock input, TCC will increase by 1 at every falling edge or rising edge of the TCC pin.

- The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e. in sleep mode). During the normal operation or the sleep mode, a WDT time-out (if

enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during the normal mode by software programming. Refer to WDTE bit of IOCE0 register. With no prescaler, the WDT time-out period is approximately 18 ms[1] or 1ms[2] (one oscillator start-up timer period).

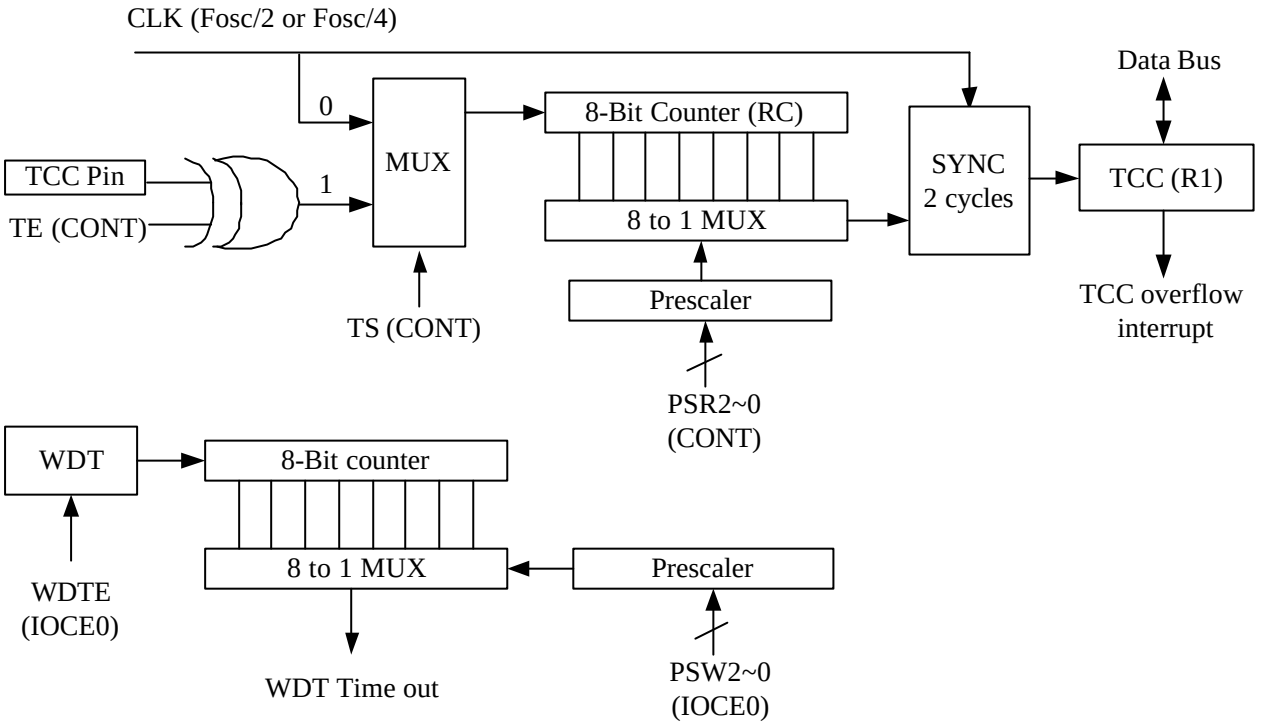


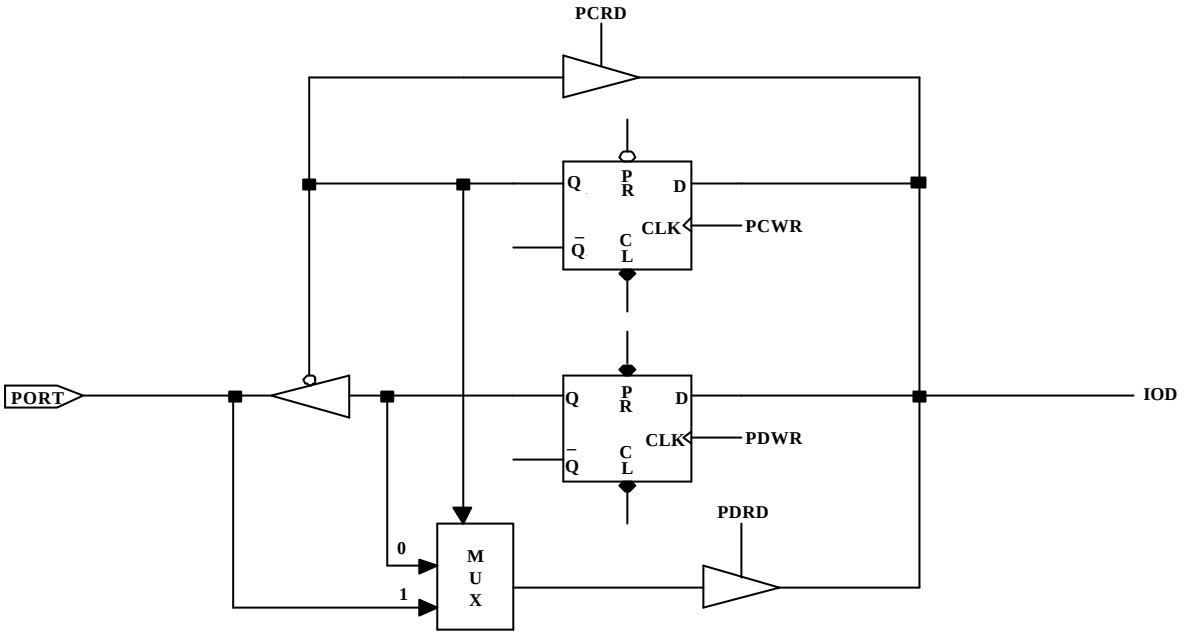
Fig. 6 Block Diagram of TCC and WDT

4.4 I/O Ports

The I/O registers, (Port 5, Port 6, and Port 7), are bi-directional tri-state I/O ports. Port 5 is pulled-high internally by software. Likewise, P6 has its open-drain output also through software. Port 5 features an input status changed interrupt (or wake-up) function and is pulled-down by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC7). The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5, Port 6 and Port7 are shown in Fig. 7, Fig. 8, and Fig. 9 respectively.

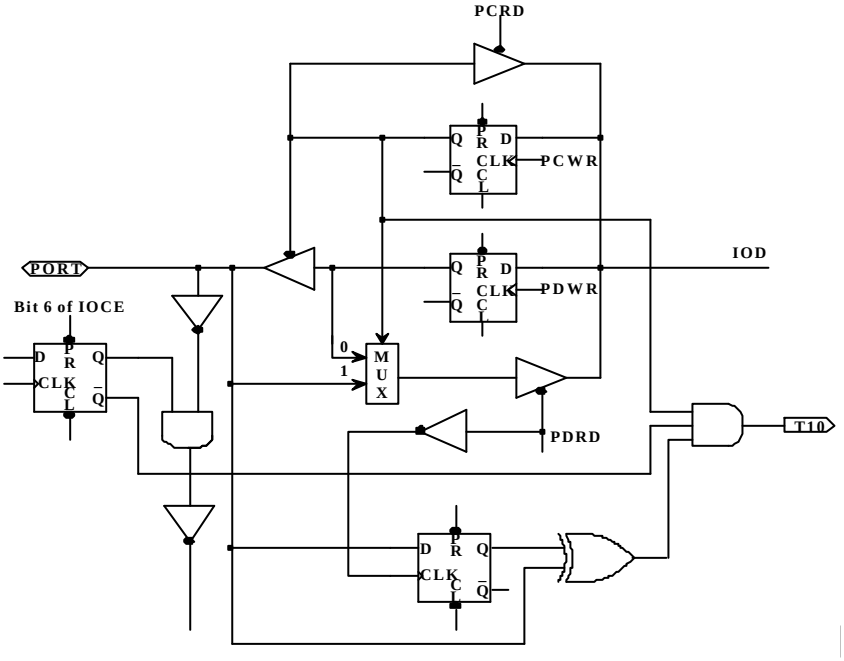
[1] NOTE: VDD=5V, Setup time period = 15.4ms ± 30%.
VDD=3V, Setup time period = 17.6ms ± 30%.

[2] NOTE: VDD=5V, Setup time period = 1.07ms ± 30%.
VDD=3V, Setup time period = 1.22ms ± 30%.



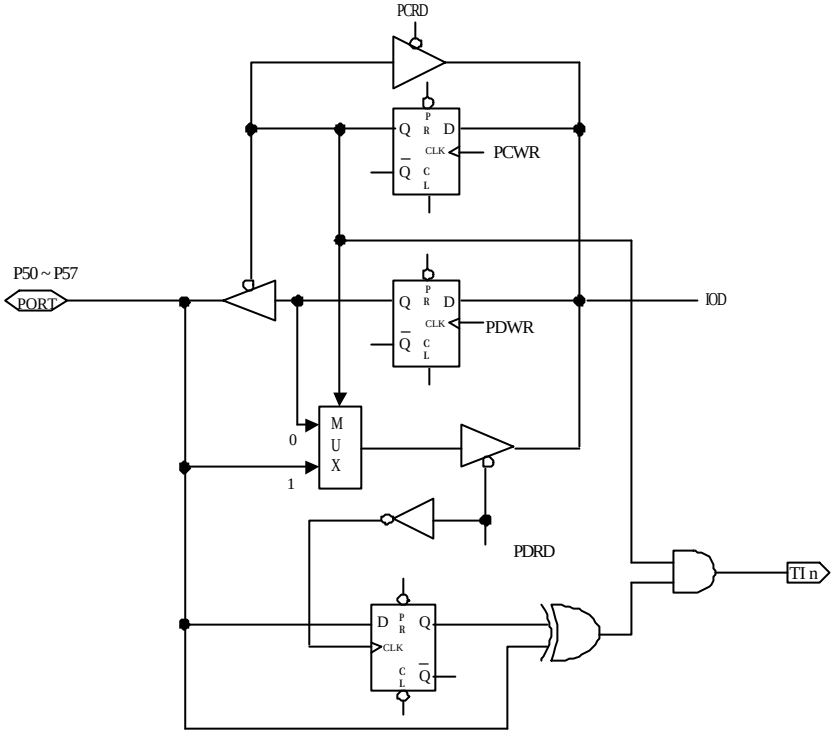
NOTE: Open-drain is not shown in the figure.

Fig. 7 The circuit of I/O port and I/O control register for Port 6 and Port7



NOTE: Open-drain is not shown in the figure.

Fig. 8 The Circuit of I/O Port and I/O Control Register for P60(/INT)



NOTE: Pull-high(down) is not shown in the figure.

Fig. 9 The Circuit of I/O Port and I/O Control Register for P50~P57

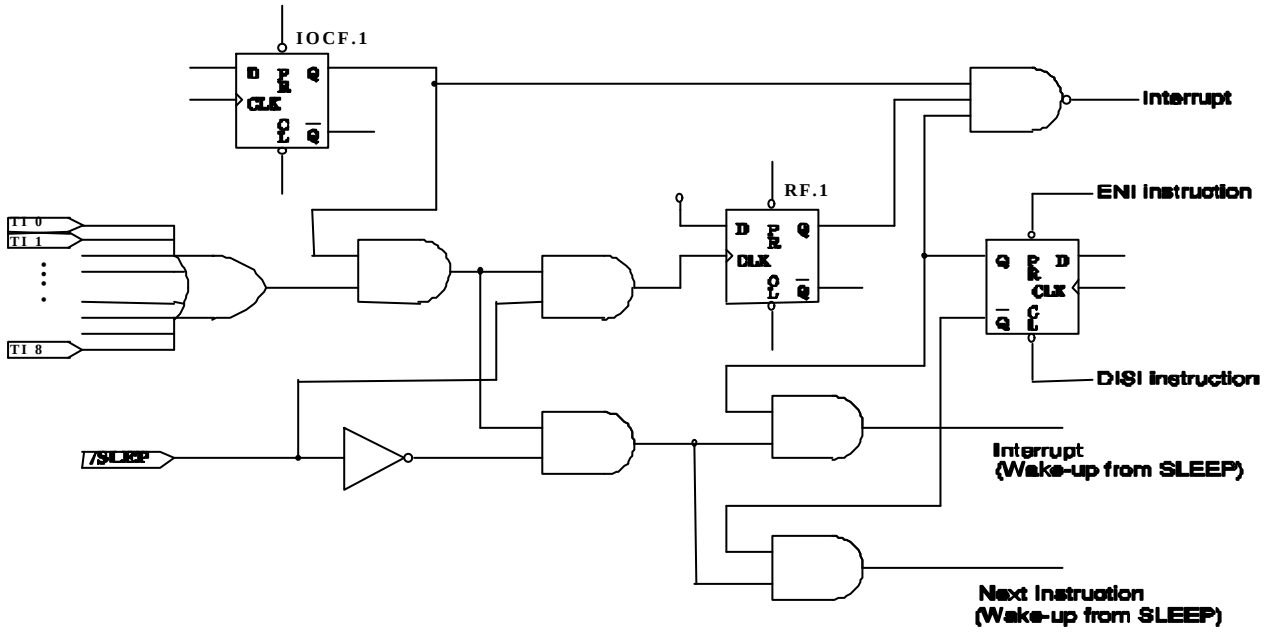


Fig. 10 Block Diagram of I/O Port 5 with Input Change Interrupt/Wake-up

Table 5 Usage of Port 5 Input Status Changed Wake-up/Interrupt Function

Usage of Port 5 input status changed Wake-up/Interrupt	
(I) Wake-up from Port 5 Input Status Change (a) Before SLEEP 1. Disable WDT 2. Read I/O Port 5 (MOV R5,R5) 3. Execute "ENI" or "DISI" 4. Enable interrupt (Set IOCF0.1) 5. Execute "SLEP" instruction (b) After Wake-up 1. IF "ENI" → Interrupt vector (3FEH) 2. IF "DISI" → Next instruction	**(II)** Port 5 Input Status Change Interrupt 1. Read I/O Port 5 (MOV R5,R5) 2. Execute "ENI" 3. Enable interrupt (Set IOCF0.1) 4. IF Port 5 change (interrupt) → Interrupt vector (3FEH)

4.5 RESET and Wake-up

1. RESET

A RESET is initiated by one of the following events-

(1) Power on reset;

(2) /RESET pin input "low", or

(3) Watch dog timer time-out (if enabled).

The device is kept in aRESET condition for a period of approximately 18ms[1] or 1ms[2] (one oscillator start-up timer period) after the reset is detected. **The initial address is 000h**.Once the RESET occurs, the following events are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.
- When power is switched on, the upper 3 bits of R3 are cleared.
- The bits of the CONT register are set to all "1" except for the Bit 6 (INT flag).
- The bits of the IOCB0 register are set to all "1".
- The IOCC0 register is cleared.
- The bits of the IOCD0 register are set to all "1".

[1] NOTE: VDD=5V, Setup time period = 15.4ms ± 30%.
VDD=3V, Setup time period = 17.6ms ± 30%.

[2] NOTE: VDD=5V, Setup time period = 1.07ms ± 30%.
VDD=3V, Setup time period = 1.22ms ± 30%.

- Bit 7 of the IOCE0 register is set to "1", and the others are cleared.
- RF and IOCF0 register are cleared.

The sleep (power down) mode is attained by executing the " SLEP" instruction. While entering sleep mode, WDT (if enabled) is cleared but keeps on running. The controller can be awakened by

(1) external reset input on /RESET pin.

(2) WDT time-out (if enabled).

(3) Port 5 input status changed (if enabled).

(4) Comparator status changed.

The first two cases will cause the EM78P257A/B to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Case 3 is considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) decides whether or not the controller branches to the interrupt vector following wake-up. If ENI is executed before SLEP, the instruction will begin to execute from the address 3FEH after wake-up. If DISI is executed before SLEP, the operation will restart from the instruction right next to SLEP after wake-up.

Only one of Cases 2 and 3 can be enabled before entering the sleep mode. That is,

[a] if Port 5 input status changed interrupt is enabled before SLEP , WDT must be disabled by software. However, the WDT bit in the option register remains enabled. Hence, the EM78P257A/B can be awakened only by Case 1 or 3. Similarly, the same procedures should be applied if comparator status change interrupt is used. The device can be awakened only by Case 1 or 4.

[b] if WDT is enabled before SLEP, Port 5 Input Status Change Interrupt must be disabled. Hence, the EM78P257A/B can be awakened only by Case 1 or 2. Refer to the section on Interrupt.

If Port 5 Input Status Change Interrupt is used to wake-up the EM78P257A/B, the following instructions must be executed before SLEP:

```
MOV A, @xx000110b       ; Select internal TCC clock
CONTW
CLR R1                  ; Clear TCC and prescaler
MOV A, @xxxx1110b       ; Select WDT prescaler
CONTW
WDTC                    ; Clear WDT and prescaler
MOV A, @0xxxxxxxb       ; Disable WDT
IOW RE
MOV R5, R5              ; Read Port 5
MOV A, @00000x1xb       ; Enable Port 5 input change interrupt
IOW RF
ENI (or DISI)           ; Enable (or disable) global interrupt
SLEP                    ; Sleep
NOP
```

In a similar way, if the Comparator Status Changed Interrupt is used to wake-up the EM78P257A/B , the following instructions must be executed before SLEP:

```
MOV A, @0bxx000110      ; Select internal TCC clock
CONTW
CLR R1                  ; Clear TCC and prescaler
MOV A, @0bxxxx1110      ; Select WDT prescaler
CONTW
WDTC                    ; Clear WDT and prescaler
MOV A, @0b0xxxxxxx      ; Disable WDT
IOW RE
MOV A, @0b1111xxxx      ; Enable comparator high interrupt
IOW RF
ENI (or DISI)           ; Enable (or disable) global interrupt
SLEP                    ; Sleep
NOP
```

One problem user must be aware of, is that after waking up from the sleep mode, WDT will enable automatically. The WDT operation (being enabled or disabled) should be handled appropriately by software after waking up from the sleep mode.

Table 6 Summary of the Initialized Values for Registers

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC50	Bit Name	C57	C76	C55	C54	C53	C52	C51	C50
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC60	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC70	Bit Name	X	X	X	X	X	X	C71	C70
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC80 (TCCCR)	Bit Name	TCC2E	TCC4E	TCC6E	TCCBE	X	X	X	X
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC90 (CMPCR)	Bit Name	COIE4	COIE3	COIE2	COIE1	CE4	CE3	CE2	CE1
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCA0 (COICS)	Bit Name	X	X	X	X	CI3	CI2	CI1	CI0
		Power-On	1	1	1	1	0	0	0	0
		/RESET and WDT	1	1	1	1	0	0	0	0

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCB0 (PDCR)	Bit Name	/PD57	/PD56	/PD55	/PD54	/PD53	/PD52	/PD51	/PD50
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCC0 (ODCR)	Bit Name	OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCD0 (PHCR)	Bit Name	/PH57	/PH56	/PH55	/PH54	/PH53	/PH52	/PH51	/PH50
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCE0	Bit Name	WDTC	EIS	X	X	X	PSW2	PSW1	PSW0
		Power-On	0	0	1	1	1	1	1	1
		/RESET and WDT	0	0	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	1	1	1	P	P	P
N/A	IOCF0	Bit Name	CMP4IE	CMP3IE	CMP2IE	CPM1IE	PPC/CMP	EXIE	ICIE	TCIE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC51 (TCCA)	Bit Name	TCCA7	TCCA6	TCCA5	TCCA4	TCCA3	TCCA2	TCCA1	TCCA0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC61 (TCCBL)	Bit Name	TCCBL7	TCCBL6	TCCBL5	TCCBL4	TCCBL3	TCCBL2	TCCBL1	TCCBL0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC71 (TCCBH)	Bit Name	TCCBH7	TCCBH6	TCCBH5	TCCBH4	TCCBH3	TCCBH2	TCCBH1	TCCBH0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC81 (TCCC)	Bit Name	TCCC7	TCCC6	TCCC5	TCCC4	TCCC3	TCCC2	TCCC1	TCCC0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC91 (LTR)	Bit Name	LTR7	LTR6	LTR5	LTR4	LTR3	LTR2	LTR1	LTR0
		Power-On	0	0	0	0	0	0	0	0

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCA1 (HTR)	Bit Name	HTR7	HTR6	HTR5	HTR4	HTR3	HTR2	HTR1	HTR0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCB1 (PTR)	Bit Name	PTR7	PTR6	PTR5	PTR4	PTR3	PTR2	PTR1	PTR0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	INTE	INT	TS	TE	X	PSR2	PSR1	PSR0
		Power-On	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x00	R0(IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x01	R1(TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	00	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x02	R2(PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	Jump to address 0x08 or continue to execute next instruction							
0x03	R3(SR)	Bit Name	RST	IOCS	PS0	T	P	Z	DC	C
		Power-On	0	0	0	1	1	U	U	U
		/RESET and WDT	P	0	0	t	t	P	P	P
		Wake-Up from Pin Change	P	P	P	t	t	P	P	P
0x04	R4(RSR)	Bit Name	GP1	BS	X	X	X	X	X	X
		Power-On	U	0	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x05	R5	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x06	R6	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x7	R7	Bit Name	-	-	-	-	-	-	P71	P70
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x8	R8	Bit Name	-	-	-	-	-	-	-	-
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x9	R9	Bit Name	CMPOUT4	CMPOUT3	CMPOUT2	CMPOUT1	-	TCCCIF	TCCBIF	TCCAIF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0xA	RA (TCCCR1)	Bit Name	-	-	-	-	-	TCCAIE	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0xB	RB (TCCCR2)	Bit Name	-	TCCBIE	-	-	-	TCCCIE	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0xC	RC (TCCPR)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0xD	RD (TMR2H)	Bit Name	DP1	DP0	MF1	MF0	IRE	HF	LGP	PWM
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0xE	RE (TMR2L)	Bit Name	MOUSEN	-	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0xF	RF (ISR)	Bit Name	CMP4IF	CMP3IF	CMP2IF	CMP1IF	-	EXIF	ICIF	TCIF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	0	0	0	0	0	0
0x10~0x3F	R10~R3F	Bit Name	-	-	-	-	-	-	-	-
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P

X: not used. U: unknown or don' t care. P: previous value before reset.

t: check Table 6

2. /RESET Configure

Refer to Fig.11 When the RESET bit in the OPTION word is programmed to 0, the external /RESET is enabled. When programmed to 1, the internal /RESET is enabled, tied to the internal Vdd and the pin is defined as P71.

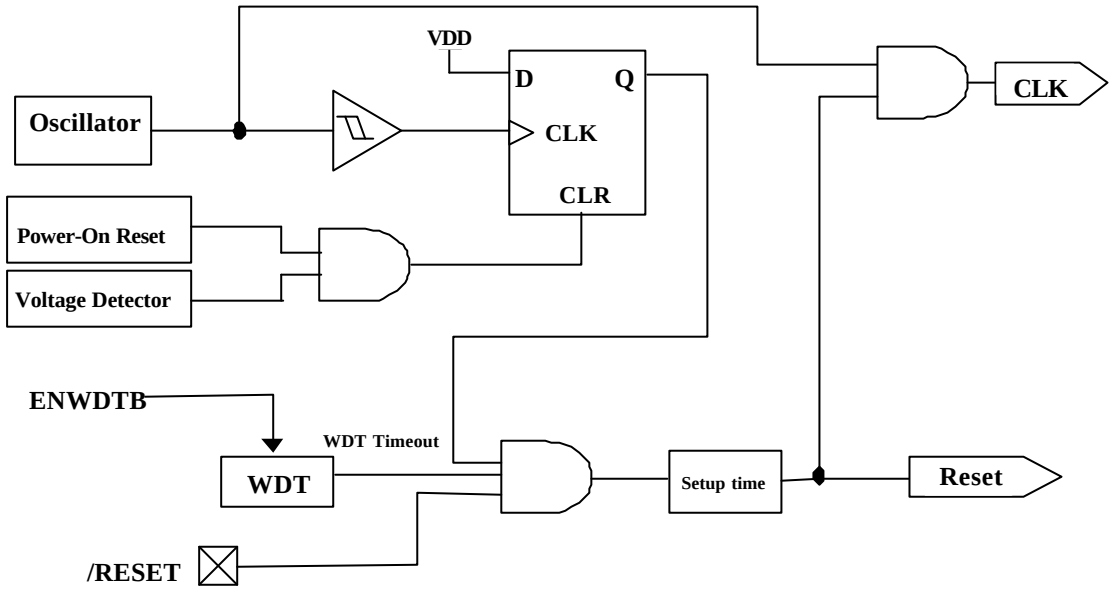


Fig. 11 Block Diagram of Reset of Controller

3. The status of RST, T, and P of STATUS register

A RESET condition is initiated by one of the following events:

1. A power-on condition.
2. A high-low-high pulse on the /RESET pin, or
3. Watchdog timer time-out.

The values of RST, T, and P, as listed in Table 7 below. are used to check how the processor wakes up.

Table 8 shows the events which may affect the status of RST, T, and P.

Table 7 The Values of RST, T, and P after RESET

Reset Type	RST	T	P
Power on	0	1	1
/RESET during Operating mode	0	*P	*P
/RESET wake-up during SLEEP mode	0	1	0
WDT during Operating mode	0	0	1
WDT wake-up during SLEEP mode	0	0	0
Wake-Up on pin change during SLEEP mode	1	1	0

*P: Previous status before reset

Table 8 The Status of RST, T, and P being Affected by Events

Event	RST	T	P
Power on	0	1	1
WDTC instruction	*P	1	1
WDT time-out	0	0	*P
SLEP instruction	*P	1	0
Wake-Up on pin change during SLEEP mode	1	1	0

*P: Previous value before reset

4.6 Interrupt

The EM78P257A/B has five interrupt sources as listed below:

(1) TCC overflow interrupt.

(2) Port 5 Input Status Changed Interrupt.

(3) External interrupt [(P60, /INT) pin].

(4) Comparators status change.

(5) IR OUT interrupt.

Before the Port 5 Input Status Change Interrupt is enabled, reading Port 5 (e.g. "MOV R5,R5") is necessary. Each Port 5 pin will have this feature if its status changes The Port 5 Input Status Change Interrupt will wake up the EM78P257A/B from the sleep mode if it is enabled prior to going into the sleep mode by executing SLEP instruction. When wake-up occurs, the controller will continue to execute program in-line if the global interrupt is disabled. . If the global interrupt is enabled, it will branch out to the interrupt vector 3FEH.

RF is the interrupt status register that records the interrupt requests in the relative flags/bits. IOCF0 is an interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in RF. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine to avoid recursive interrupts.

The flag (except ICIF0 bit) in the Interrupt Status Register (RF) is set regardless of the status of its mask bit or the execution of ENI. Note that the outcome of RF will be the logic AND of RF and IOCF0 (refer to Fig.12), The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

When an interrupt is generated by the Timer clock/counter (when enabled), the next instruction will be fetched from address 3FA,3F8,3F6, and 3F4H(TCC,TCCA,TCCB, and TCCC). When an interrupt is generated by the Comparators (when enabled), the next instruction will be fetched from address 3F2,3F0,3EE, or 3ECH individually(CO1,CO2,CO3, or CO4). Before the interrupt subroutine is executed, the contents of ACC and the R3 register will be saved by hardware. If another interrupt occurred, the ACC and R3 will be replaced by the new interrupt. After the interrupt service routine is finished, ACC and R3 will be pushed back.

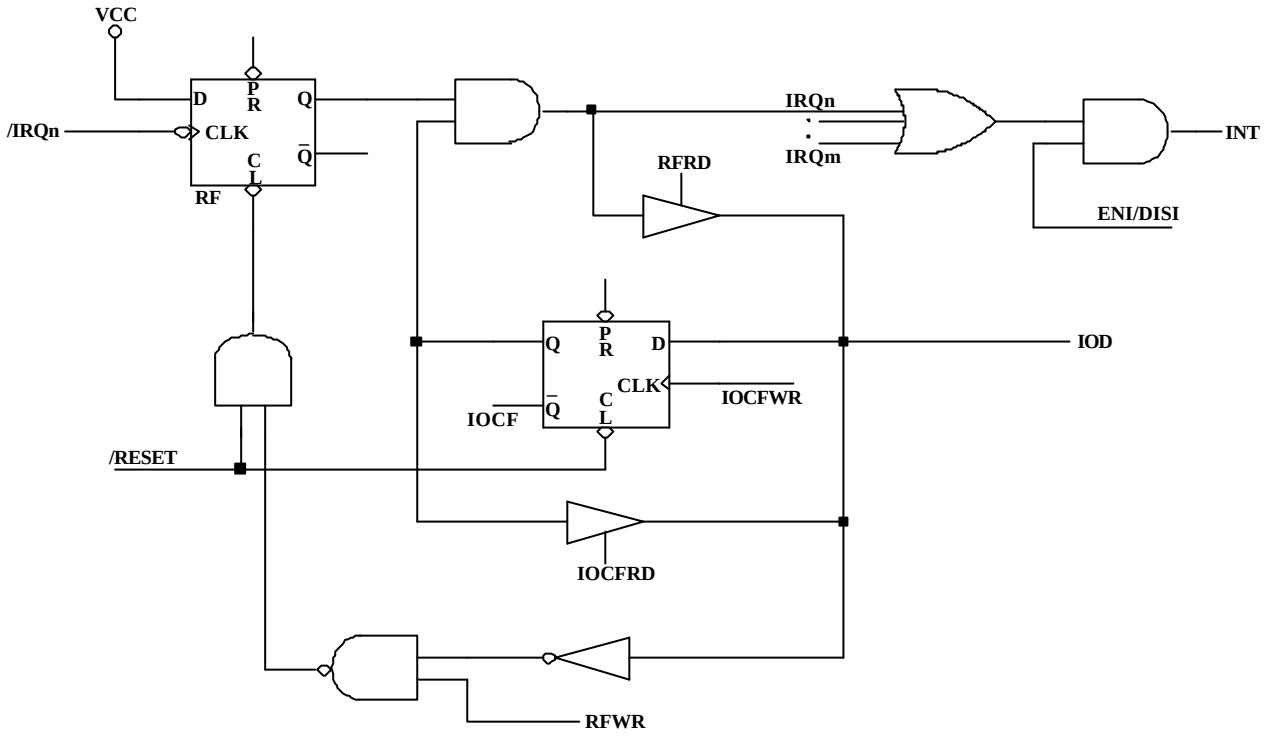


Fig. 12 Interrupt input circuit

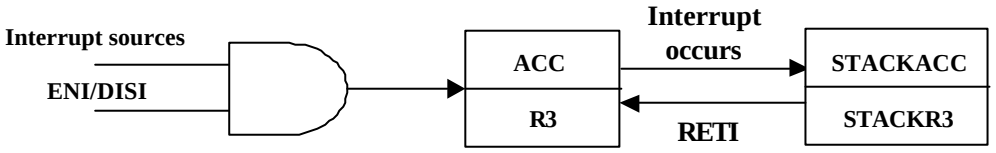


Fig. 13 Interrupt backup diagram

In EM78P257A/B, each individual interrupt source has its own interrupt vector as depicted in Table 9.

Table 9 Interrupt vector

Interrupt vector	Interrupt status
3EC	Comparator CO4 interrupt
3EE	Comparator CO3 interrupt
3F0	Comparator CO2 interrupt
3F2	Comparator CO1 interrupt
3F4	TCCC overflow interrupt
3F6	TCCB overflow interrupt
3F8	TCCA overflow interrupt
3FA	TCC overflow interrupt
3FC	External interrupt
3FE	Port 5 pin change

4.7 Timer/Counter

1. Overview

Timer1 (TCCA) and Timer3 (TCCC) are eight-bit clock counters. Timer2 (TCCB) is a 16-bit clock counter. TCCA, TCCB, and TCCC can be read and written, and cleared at every reset condition.

2. Function Description

Fig.14 shows the TIMER block diagram. Each signal and block is described as follows:

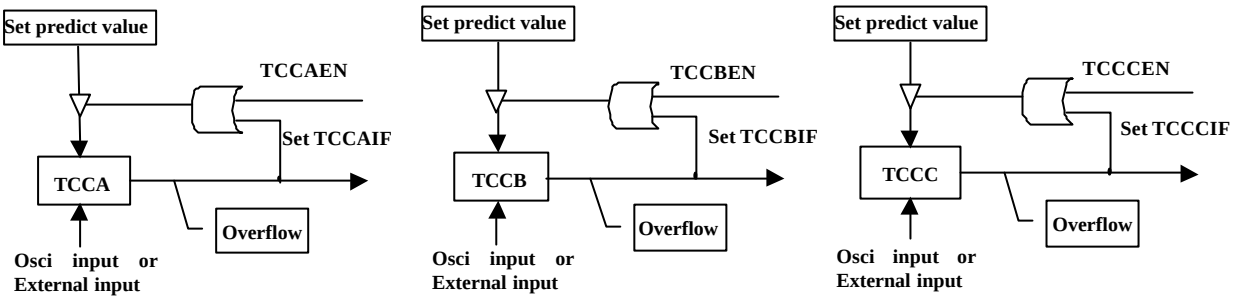


Fig. 14 TIMER Block Diagram

- **Osci input** : Input clock.
- **TCCX**: Timer 1~3 register; TCCX increases until it matches with zero, and then reload the previous value. If TCCXIE is enabled, TCCXIF will be set at the same time.

3. Programming the Related Registers

When defining TCCX, refer to the related registers of its operation as shown in the Table 10 and Table 11 below.

Table 10 Related Control Registers of the TCCX

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0A	TCR(1)/RA	0	0	0	0	0	TCCAIE/0	TCCATS/0	TCCATE/0
0x0B	TCR(2)/RB	0	TCCBIE/0	TCCBTS/0	TCCBTE/0	0	TCCCIE/0	TCCCTS/0	TCCCTE/0
0x08	TCCCR/IOC80	TCC2E	TCC4E	TCC6E	TCCBE	0	0	0	0

Table 11 Related Status/Data Registers of TCCX

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x09	TCCSR/R9	CMPOUT4	CMPOUT3	CMPOUT2	CMPOUT1	0	TCCCIF	TCCBIF	TCCAIF
0x05	TCCA/IOC51	TCCA7	TCCA6	TCCA5	TCCA4	TCCA3	TCCA2	TCCA1	TCCA0
0x06	TCCBL/IOC61	TCCBL7	TCCBL6	TCCBL5	TCCBL4	TCCBL3	TCCBL2	TCCBL1	TCCBL0
0x07	TCCBH/IOC71	TCCBH7	TCCBH6	TCCBH5	TCCBH4	TCCBH3	TCCBH2	TCCBH1	TCCBH0
0x08	TCCC/IOC81	TCCC7	TCCC6	TCCC5	TCCC4	TCCC3	TCCC2	TCCC1	TCCC0
0x09	LTR/IOC91	LTR7	LTR6	LTR5	LTR4	LTR3	LTR2	LTR1	LTR0
0x0A	HTR/IOCA1	HTR7	HTR6	HTR5	HTR4	HTR3	HTR2	HTR1	HTR0
0x0B	PTR/IOCB1	PTR7	PTR6	PTR5	PTR4	PTR3	PTR2	PTR1	PTR0

4.8 Comparator

EM78P257A/B has four comparators, consisting of two analog inputs and one output. The comparators can be employed to wake up from sleep mode. Fig. 15 and Fig. 16 show the circuit of the comparator.

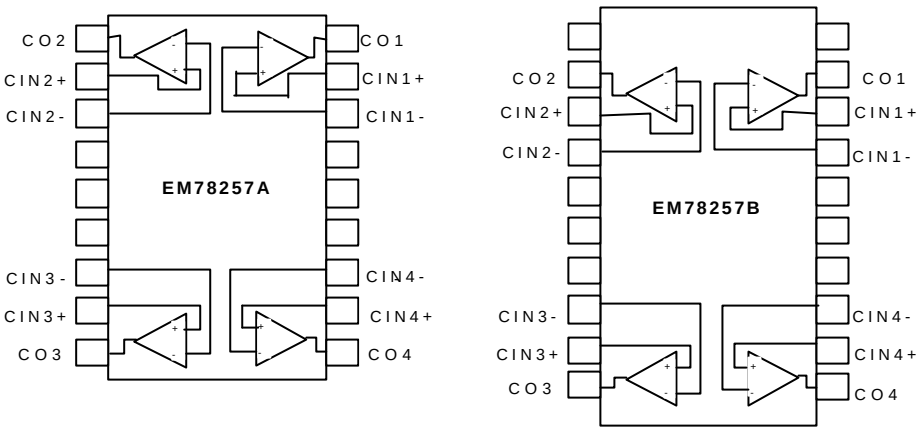


Fig. 15 Comparator Pin Assignments

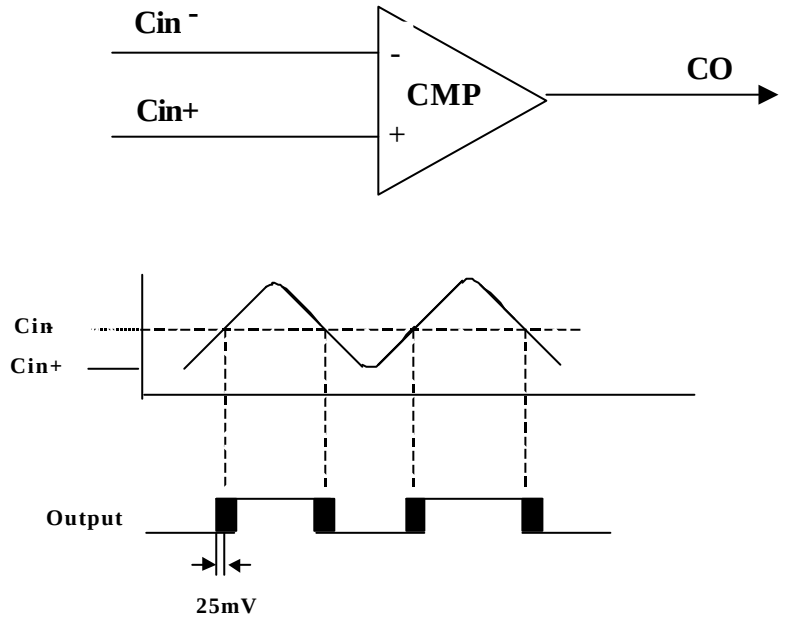


Fig. 16 Comparator Operating Modes

1. External Reference Signal

The analog signal that is presented at Cin- compares to the signal at Cin+, and the digital output (CO) of the comparator is adjusted accordingly.

- The reference signal must be between Vss and Vdd

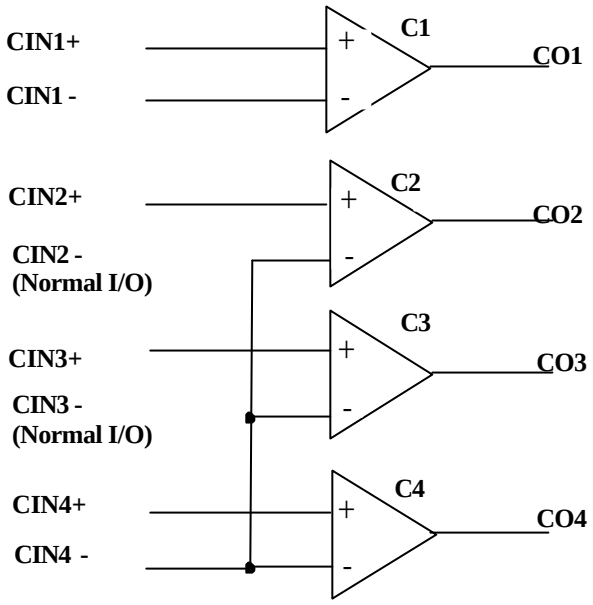
- The reference voltage can be applied to either pin of a comparator
- Threshold detector applications may use the same references
- The comparator can operate from the same or different reference sources
- There are 16 combinations of the negative inputs of the four comparators

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMPCR/IOC90	-	-	-	-	CI3	CI2	CI1	CI0

Table 12 The List of CO-INPUT Combine Sequence

CI3	CI2	CI1	CI0	CO- Input combine status	Comment
0	0	0	0	N/A	1,2,3, and 4 -> negative inputs,
0	0	0	1	1,2	CIN2- -> negative input; CIN1- -> normal I/O pin;
0	0	1	0	1,3	CIN3- -> negative input; CIN1- -> normal I/O pin;
0	0	1	1	1,4	CIN4- -> negative input; CIN1- -> normal I/O pin;
0	1	0	0	2,3	CIN3- -> negative input; CIN2- -> normal I/O pin;
0	1	0	1	2,4	CIN4- -> negative input; CIN2- -> normal I/O pin;
0	1	1	0	3,4	CIN4- -> negative input; CIN3- -> normal I/O pin;
0	1	1	1	1,2,3	CIN3- -> negative input; CIN(1,2)- -> normal I/O pin;
1	0	0	0	1,2,4	CIN4- -> negative input; CIN(1,2)- -> normal I/O pin;
1	0	0	1	1,3,4	CIN4- -> negative input; CIN(1,3)- -> normal I/O pin;
1	0	1	0	2,3,4	CIN4- -> negative input; CIN(2,3)- -> normal I/O pin;
1	0	1	1	1,2,3,4	CIN4- -> negative input; CIN(1,2,3)- -> normal I/O pin;
1	1	0	0	3,2	CIN2- -> negative input; CIN3- -> normal I/O pin;
1	1	0	1	4,2	CIN2- -> negative input; CIN4- -> normal I/O pin;
1	1	1	0	4,3,2	CIN2- -> negative input; CIN(3,4)- -> normal I/O pin;
1	1	1	1	1,4,3	CIN3- -> negative input; CIN(1,4)- -> normal I/O pin;

Example: (CI3,CI2,CI1,CI0)= (1010) => Comparator 4(-) combine together with Comparator 3(-) and Comparator 2(-), and both of CIN3- and CIN2- work as normal I/O pins.



2. Comparator Outputs

- The compared result are stored in the CMPOUT of R9
- The comparator outputs can output to P51, P52, P63 and P64 by programming Bits 4, 5, 6, and 7 <IOC90> of the CMP control register to 1
- P52, P51, P63 and P64 must be configured as output if implemented
- Fig. 17 shows the comparator output block diagram.

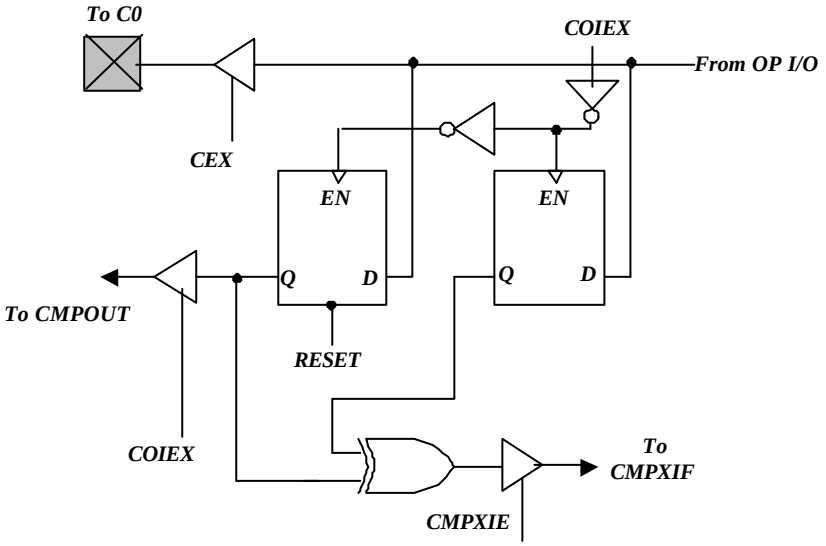


Fig. 17 The Output Configuration of a Comparator

3. Programming the Related Registers

When defining Comparators, refer to the related registers of its operation as shown in Table 13 and Table 14 below.

Table 13 Related Control Registers of the Comparators

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x09	CMPCR/IOC90	COIE4/0	COIE3/0	COIE2/0	COIE1/0	CE4/0	CE3/0	CE2/0	CE1/0
0x0A	COICS/IOCA0	0	0	0	0	CI3/0	CI2/0	CI1/0	CI0/0
0x0F	IMR/IOCF0	CMP4IE/0	CMP3IE/0	CMP2IE/0	CMP1IE/0	PPC/CMP	EXIE/0	ICIE/0	TCIE/0

Table 14 Related Status/Data Registers of Comparators

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x09	CMPOUT/R9	CMPOUT4/0	CMPOUT3/0	CMPOUT2/0	CMPOUT1/0	0	TCCCIF/0	TCCBIF/0	TCCAIF/0
0x0F	ISR/RF	CMP4IF/0	CMP3IF/0	CMP2IF/0	CMP1IF/0	0	EXIF/0	ICIF/0	TCIF/0

4. Interrupt

- INT, and CMPXIE must be enable
- Interrupt occurs whenever a change takes place on the output pin of the comparators
- The actual changes on the pins can be determined by reading the bits CMPOUTX and R9<P7~P4>
- CMPXIF, the comparator interrupt flag, can only be cleared by software

5. Wake-Up from SLEEP mode

- If enabled, the comparators remains active and the interrupt stays functional during SLEEP mode.
- If a mismatch occurs, the interrupt will wake up the device from SLEEP mode.
- The power consumption should be taken into consideration for the sake of power saving.
- If the function is unemployed during the SLEEP mode, turn off comparators before entering into sleep mode.

4.9 Oscillator

1. Oscillator Modes

The EM78P257A/B can be operated in the five different oscillator modes, such as Internal RC oscillator mode (IRC), RC oscillator with Internal capacitor mode(IC),External RC oscillator mode(ERC), High XTAL oscillator mode(HXT), and Low XTAL oscillator mode(LXT). User can select oneof them by programming OSC2,OCS1 and OSC0 in the CODE Option register. Table15 depicts how these five modes are defined.

The up-limited operation frequency of crystal/resonator on the different VDDs is listed in Table 16

Table 15 Oscillator Modes defined by OSC2,OSC1 and OSC0

Mode	OSC2	OSC1	OSC0
IRC(Internal RC oscillator mode)	1	1	1
IC(Internal C oscillator mode)	1	1	0

ERC(External RC oscillator mode)	1	0	1
HXT(High XTAL oscillator mode)	0	0	1
LXT(Low XTAL oscillator mode)	0	0	0

<Note> The transient point of system frequency between HXT and LXT is around 400 KHz.

Table 16 The summary of maximum operating speeds

Conditions	VDD	Fxt max.(MHz)
Two clocks	2.3	4
	3.0	8
	5.0	20

2. Crystal Oscillator/Ceramic Resonators(XTAL)

EM78P257A/B can be driven by an external clock signal through the OSCI pin as shown in Fig.18 below.

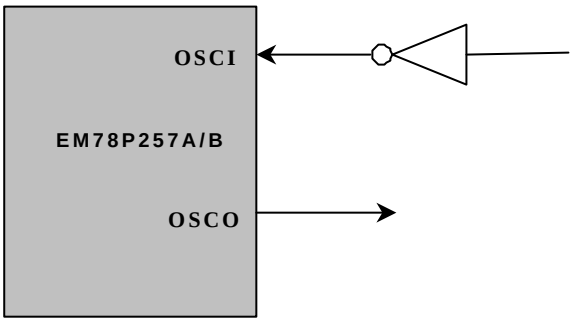


Fig. 18 Circuit for External Clock Input

In most applications, pin OSCI and pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Fig. 19 depicts such circuit. The same thing applies whether it is in the HXT mode or in the LXT mode. Table 17 provides the recommended values of C1 and C2. Since each resonator has its own attribute, user should refer to its specification for appropriate values of C1 and C2. RS, a serial resistor, may be necessary for AT strip cut crystal or low frequency mode.

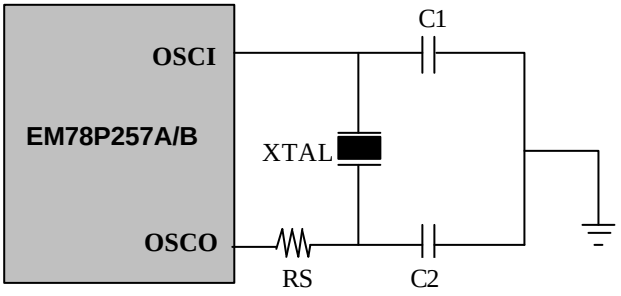


Fig. 19 Circuit for Crystal/Resonator

Table 17 Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonators

Oscillator Type	Frequency Mode	Frequency	C1(pF)	C2(pF)
Ceramic Resonators	HXT	455 kHz	100~150	100~150
		2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30
Crystal Oscillator	LXT	32.768kHz	25	15
		100KHz	25	25
		200KHz	25	25
	HXT	455KHz	20~40	20~150
		1.0MHz	15~30	15~30
		2.0MHz	15	15
		4.0MHz	15	15

3. External RC Oscillator Mode

For some applications that do not need to have its timing to be calculated precisely, the RC oscillator (IV.12.3-1) offers a lot of cost savings. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to the manufacturing process variation.

In order to maintain a stable system frequency, the values of the Cext should not be less than 20pF, and that the value of Rext should not be greater than 1 M ohm. If they cannot be kept in this range, the frequency is easily affected by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator becomes unstable because the NMOS cannot discharge the current of the capacitance correctly.

Based on the reasons above, it must be kept in mind that all of the supply voltage, the operation temperature, the components of the RC oscillator, the package types, the way the PCB is layout, will affect the system frequency

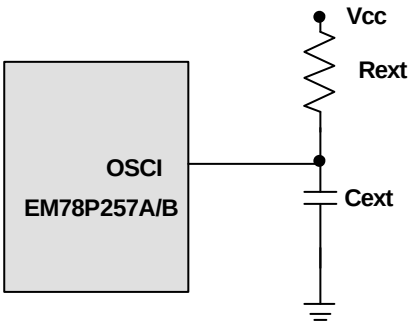


Fig. 20 Circuit for External RC Oscillator Mode

Table 18 RC Oscillator Frequencies

Cext	Rext	Average Fosc 5V,25°C	Average Fosc 3V,25°C
20 pF	3.3k	3.18 MHz	2.75MHz
	5.1k	2.1 MHz	2.0MHz
	10k	1.14 MHz	1.12 MHz
	100k	118 KHz	121 KHz
100 pF	3.3k	1.25 MHz	1.20 KHz
	5.1k	830 KHz	815 KHz
	10k	435 KHz	440 KHz
	100k	46KHz	48 KHz
300 pF	3.3k	560 KHz	545 KHz
	5.1k	370 KHz	360 KHz
	10k	195 KHz	195 KHz
	100k	20 KHz	21 KHz

<Note> 1. Measured on DIP packages.

2. Design reference only

3. The frequency drift about ±30%.

4. RC Oscillator Mode with Internal Capacitor

If both precision and cost are taken into consideration, EM78P257A/B also offers a special oscillation mode, which is equipped with an internal capacitor and an external resistor connected to Vcc. The internal capacitor functions as temperature compensator. In order to obtain more accurate frequency, a precise resistor is recommended.

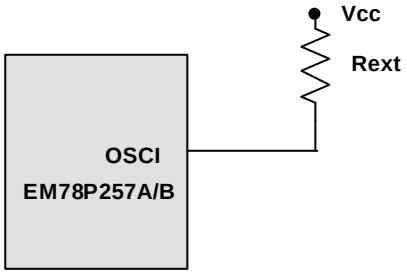


Fig. 21 Circuit for Internal C Oscillator Mode

Table 19 R Oscillator Frequencies

Rext	Average Fosc 5V,25°C	Average Fosc 3V,25°C
51k	4.3 MHz	4.3 MHz
100k	2.5 MHz	2.4 MHz
300k	800KHz	800 KHz

<Note> 1. Measured on DIP packages.

2. Design reference only

3. The frequency drift about ±30%.

5. Internal RC Oscillator Mode

EM78P257A/B offers a versatile internal RC mode with default frequency of 4MHz. The frequency can be configured by programming the bit RCM0 and bit RCM1 of the Option code. Table 20 describes a typical instance of the calibration.

Table 20 Calibration Selection for Internal RC Mode

RCM 1	RCM 0	Frequency(MHz)
1	1	4
1	0	1
0	1	455kHz
0	0	32.768kHz

<Note> 1. Measured on DIP packages.

2. Design reference only, the frequency value vary with temperature ,VDD and process.

3. The frequency drift about ±35%.

4.10 Power On Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply stabilizes at its steady state.

EM78P257A/B POR voltage range is 1.2V~1.8V.Under customer application, when power is OFF, Vdd must drop to below 1.2V and remains OFF for 10us before power can be switched ON again. This way, the EM78P257A/B will reset and work normally. The extra external reset circuit will work well if Vdd can rise at very fast speed (50 ms or less). However, under most cases where critical applications are involved, extra devices are required to assist in solving the power-up problems.

1. Programmable Oscillator Set-Up Time

The Option word (SUT) is used to define the oscillator Set-Up time (18ms or 1ms). Theoretically, the range is from 1 ms to 18 ms. For most of crystal or ceramic resonators, the lower the operation frequency, the longer is the required Set-up time.

2. External Power On Reset Circuit

The circuit shown in Fig.22 implements an external RC to produce the reset pulse. The pulse width (time constant) should be kept long enough for Vdd to reach minimum operation voltage. This circuit is used when the power supply has slow rise time. Because the current leakage from the /RESET pin is about ±5μA, it is recommended that R should not be greater than 40 K. In this way, the voltage in pin /RESET will be held below 0.2V. The diode

(D) acts as a short circuit at the moment of power down. The capacitor C will discharge rapidly and fully. Rin, the current-limited resistor, will prevent high current discharge or ESD (electrostatic discharge) from flowing to pin /RESET.

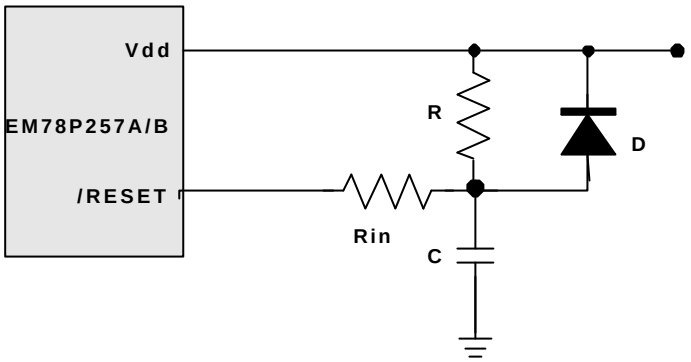


Fig. 22 External Power on Reset Circuit

3. Residue-Voltage Protection

When battery is replaced, device power (Vdd) is taken off but residue-voltage remains. The residue-voltage may trips below Vdd minimum, but not to zero. This condition may cause a poor power on reset. Fig.23 and Fig.24 show how to build a residue-voltage protection circuit

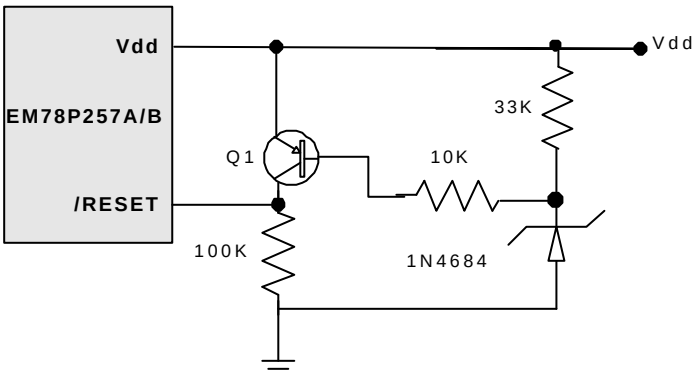


Fig. 23 Circuit 1 for the residue voltage protection

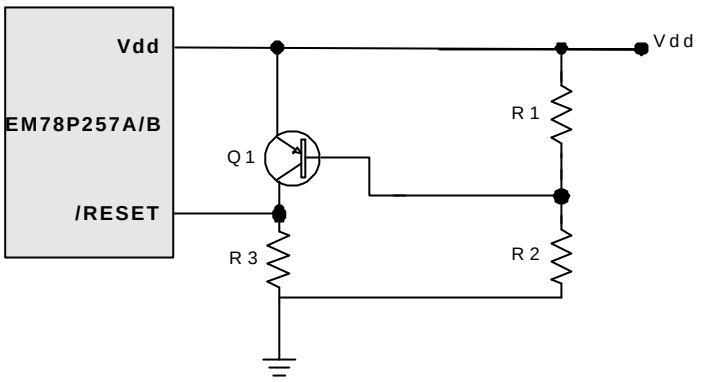


Fig. 24 Circuit 2 for the residue voltage protection

4.11 MOUSE APPLICATION MODE

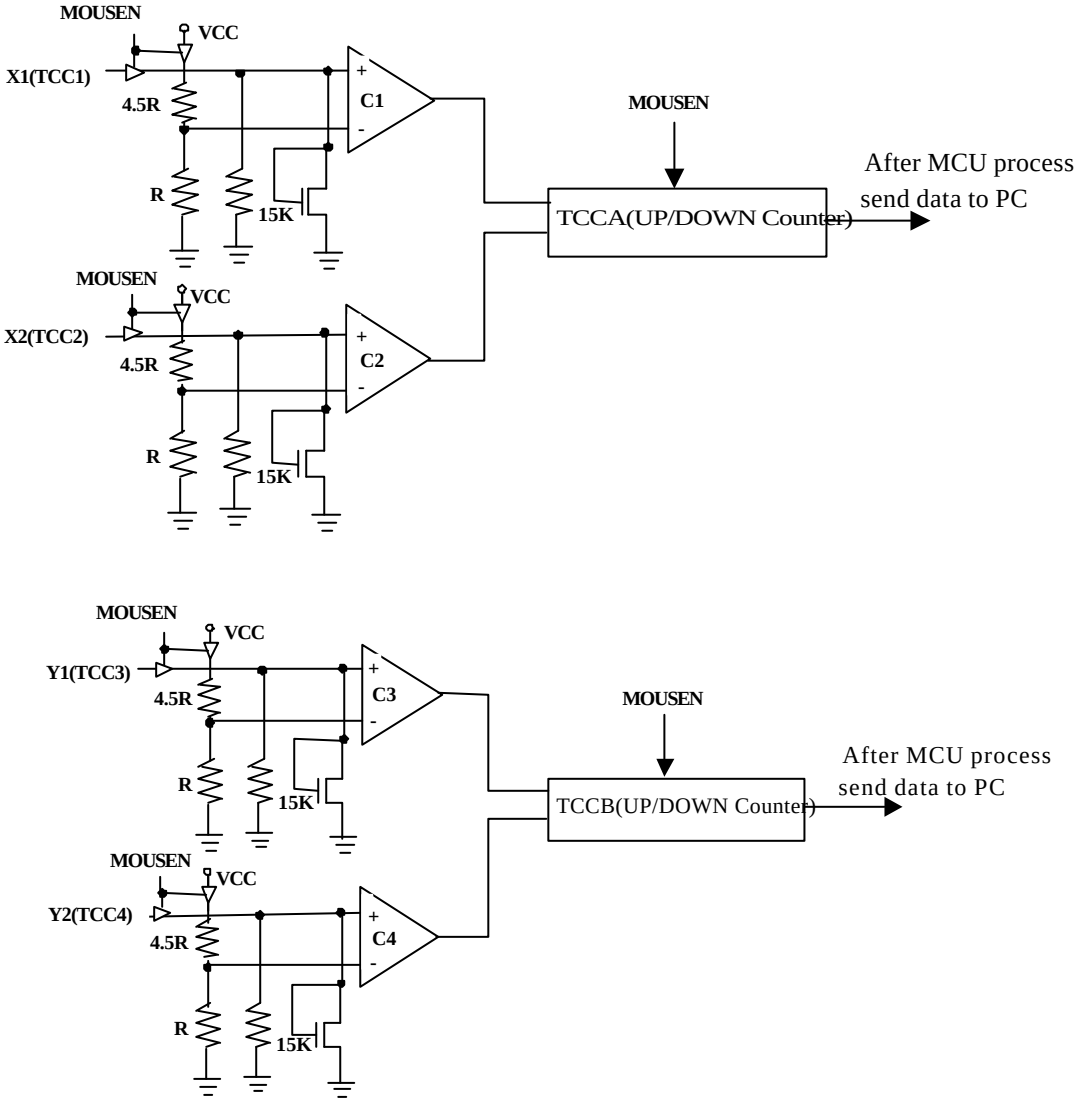
1. Overview & Features

Overview:

Fig.25 shows how EM78P257A/B communicates with PS/2 connector of PC.

Features:

- RC oscillation.
- Six photo-couples input.



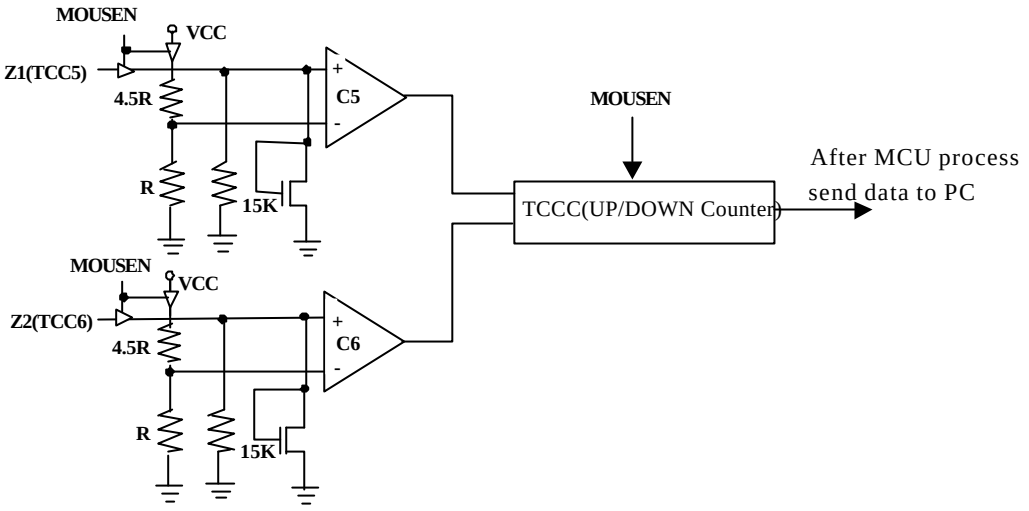


Fig. 25 Mouse Function Diagram

2. Function Description

The following describes the function of each block and signal of Fig.25 depicting how to complete a Mouse function.

P61/X1 P66/X2 P51/Y1 P50/Y2	Use current comparator to measure photo-couples "ON",or "OFF". Four photo-couple singles denoting UP, DOWN, LEFT, and RIGHT states. During scanning period, as long as the photo-couples state changes, the value of vertical or horizontal counter will increase or decrease accordingly.
P56/Z1 P57/Z2	Z-axis inputs. Photo mode: Current comparator input.
Comparator	Output level is decided by comparing the value of its two (+,-) pins.
Counter	Recording the horizontal, vertical, or rolling shifting values.

3. Programming the Related Registers

When defining MOUSE mode, refer to the related register of its operation as shown in the Table 21 and Table 22 below.

Table 21 Related Control Registers of the MOUSE Mode

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
	CONT	INTE/0	INT/0	TS/0	TE/0	0	PSR2/0	PSR1/0	PSR0/0
0X08	*INTC/IOC80	TCC2E/0	TCC4E/0	TCC6E/0	TCCBE/0	0	0	0	0
0x0A	TCR(1)/RA	0	0	0	0	0	TCCAIE/0	TCCATS/0	TCCATE/0
0X0B	TCR(2)/RB	0	TCCBIE/0	TCCBTS/0	TCCBTE/0	0	TCCCIE/0	TCCCTS/0	TCCCTE/0
0X0E	MCR/RE	MOUSEN/0	0	0	0	0	0	0	0

<Note> *Bit name/initial value

Table 22 Related Status/Data Register of the MOUSE Mode

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0

0x01	TCC/R1	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
0X09	TCCSR/R9	CMPOUT4	CMPOUT3	CMPOUT2	CMPOUT1	0	TCCCIF	TCCBIF	TCCAIF
0X05	TCCA/IOC51	TCCA7	TCCA6	TCCA5	TCCA4	TCCA3	TCCA2	TCCA1	TCCA0
0x06	TCCBL/IOC61	TCCB7	TCCB6	TCCB5	TCCB4	TCCB3	TCCB2	TCCB1	TCCB0

- TCCA: An eight-bit time clock/counter A. In MOUSE mode, it will load X-axis data into TCCA, it is defined as an increment/decrement counter.
- TCCB: An eight-bit time clock/counter B. In MOUSE mode, it will load Y-axis data into TCCB, it is defined as an increment/decrement counter.
- TCCC: An eight-bit time clock/counter C. In MOUSE mode, it will load Z-axis data into TCCC, it is defined as an increment/decrement counter.

Table 23 TCCX Status Register (1)

7	6	5	4	3	2	1	0
-	-	-	-	-	TCCAIE	TCCATS	TCCATE

- **Bit 7~Bit 3** Not used, read as ‘ 0’ .
- **Bit 2(TCCAIE)** TCCAIF interrupt enable bit.

  0: disable TCCAIF interrupt

  1: enable TCCAIF interrupt
- **Bit 1(TCCATS)** TCCA signal source

  0: internal instruction cycle clock

  1: transition on the TCC1 pin
- **Bit 0(TCCATE)** TCCA signal edge

  0: increment if the transition from low to high (leading edge) takes place on the TCC2 pin

  1: increment if the transition from high to low (leading edge) takes place on the TCC2 pin

Table 24 TCCX Status Register (2)

7	6	5	4	3	2	1	0
-	TCCBIE	TCCBTS	TCCBTE	-	TCCCIE	TCCCTS	TCCCTE

- **Bit 7** Not used.
- **Bit 6(TCCBIE)** TCCBIF interrupt enable bit.

  0: disable the TCCBIF interrupt

  1: enable the TCCBIF interrupt
- **Bit 5(TCCBTS)** TCCB signal source

  0: internal instruction cycle clock

  1: transition on the TCC3 pin
- **Bit 4(TCCBTE)** TCCB signal edge

  0: increment if the transition from low to high (leading edge) takes place on the TCC4 pin

  1: increment if the transition from high to low (leading edge) takes place on the TCC4 pin

- **Bit 3** Not used
- **Bit 2(TCCCIE)** TCCCIF interrupt enable bit.

  0: disable the TCCCIF interrupt

  1: enable the TCCCIF interrupt
- **Bit 1(TCCCTS)** TCCC signal source

  0: internal instruction cycle clock

  1: transition on the TCC5 pin.
- **Bit 0(TCCCTE)** TCCC signal edge

  0: increment if the transition from low to high (leading edge) takes place on the TCC6 pin

  1: increment if the transition from high to low (leading edge) takes place on the TCC6 pin

Table 25 MOUSE Control Register

7	6	5	4	3	2	1	0
MOUSEN	-	-	-	-	-	-	-

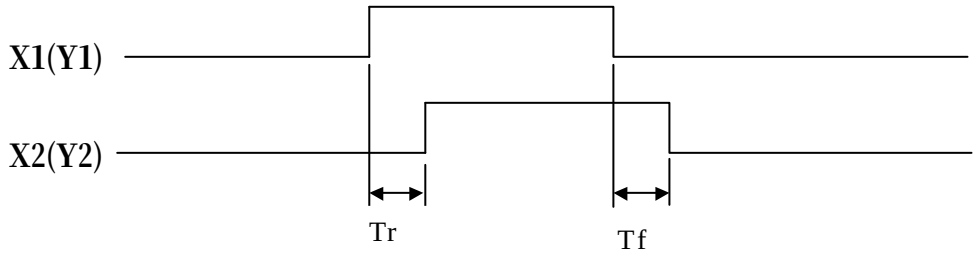
- **Bit 7 (MOUSEN)** Mouse application Enable bit.

  0: Disable MOUSEN. TCCA,TCCB and TCCC are increment counters.

  1: Enable MOUSEN. RA(disable Bit0(TCCATE), Bit1(TCCATS) is ‘1’, Bit2(TCCAIE) is ‘0’), RB(disable Bit0(TCCCTE), Bit1(TCCCTS) is ‘1’, Bit2(TCCCIE) is ‘0’, Bi, disable Bit4(TCCBTE), Bit5(TCCBTS) is ‘1’, Bit6(TCCBIE) is ‘0’), and TCCA, TCCBL and TCCC work as up/down counters. For other pin assignments, refer to IOC80.
- **Bit 6~Bit 0** Not used.

4. MOUSE mode Timing

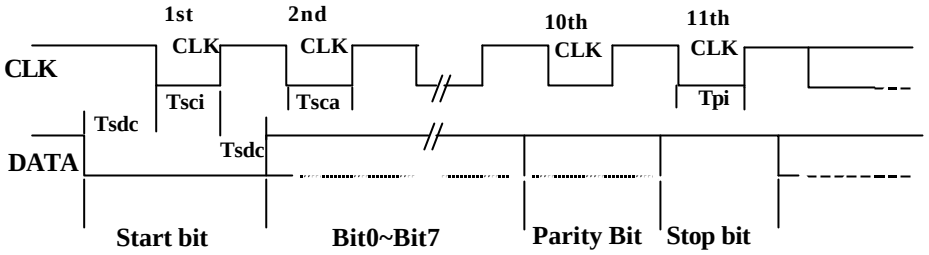
(1)Photo-couples pulse width:



Counter increment if the rising/falling edge of X1 is leading the one on X2.

Counter decrement if the rising/falling edge of X1 is falling behind the one on X2.

(2) Sending DATA (data from EM78P257A/B to system)

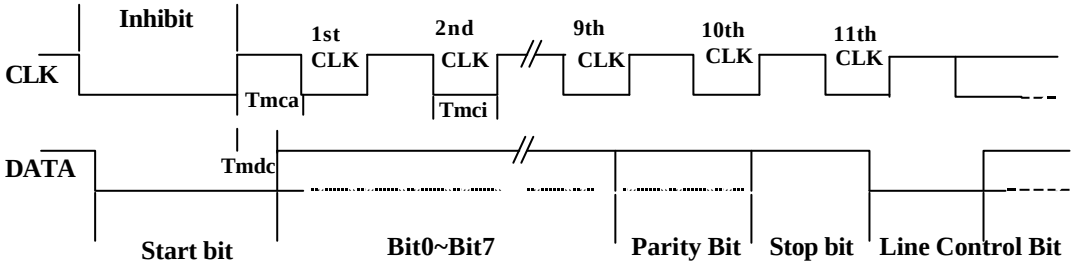


If CLK is low (inhibit status), no data transmission occurs.

If CLK is high and DATA is low (request-to-send), data is updated. Data is received from the system and no transmission is started by EM78A/B until CLK and DATA are both high. IF CLK and DATA are both high, the transmission is ready. DATA is valid prior to the falling edge of CLK and beyond the rising edge of CLK. During transmission, EM78P257A/B check for line contention by checking for an inactive level on CLK at interval not to exceed 100u seconds. Contention occurs when the system lowers CLK to inhibit EM78P257A/B output after EM78P257A/B has started a transmission. If this occurs before the rising edge of the tenth clock, EM78P257A/B internally stores its buffer and returns DATA and CLK to an active level. If the contention does not occur by the tenth clock, the transmission is completed.

Following a transmission, the system inhibits EM78P257A/B by holding CLK low until it can service the input or until the system receives a request to send a response from EM78P257A/B.

(3) Receiving DATA (from system to EM78P257A/B)



System first checks if EM78P257A/B is transmitting data. If transmitting, the system can override the output by forcing CLK to an inactive level prior to the tenth clock. If EM78P257A/B transmission is beyond the tenth clock, the system receives the data. If EM78P257A/B is not transmitting or if the system choose to override the output, the system forces CLK to an inactive level for a period of not less than 100us while preparing for output. When the system is ready to output start bit (0), it allows CLK to go to active level. If request-to-send is detected, EM78P257A/B clocks 11 bits. Following the tenth clock, EM78P257A/B checks for an active level on the DATA line, and if found, forces

DATA to low, and clock once more. If framing error occurs, EM78P257A/B continues to clock until DATA is high, then clocks the line control bit and requests for a Resend. When the system sends out a command or data transmission that requires a response, the system waits for EM78P257A/B to respond before sending its next output.

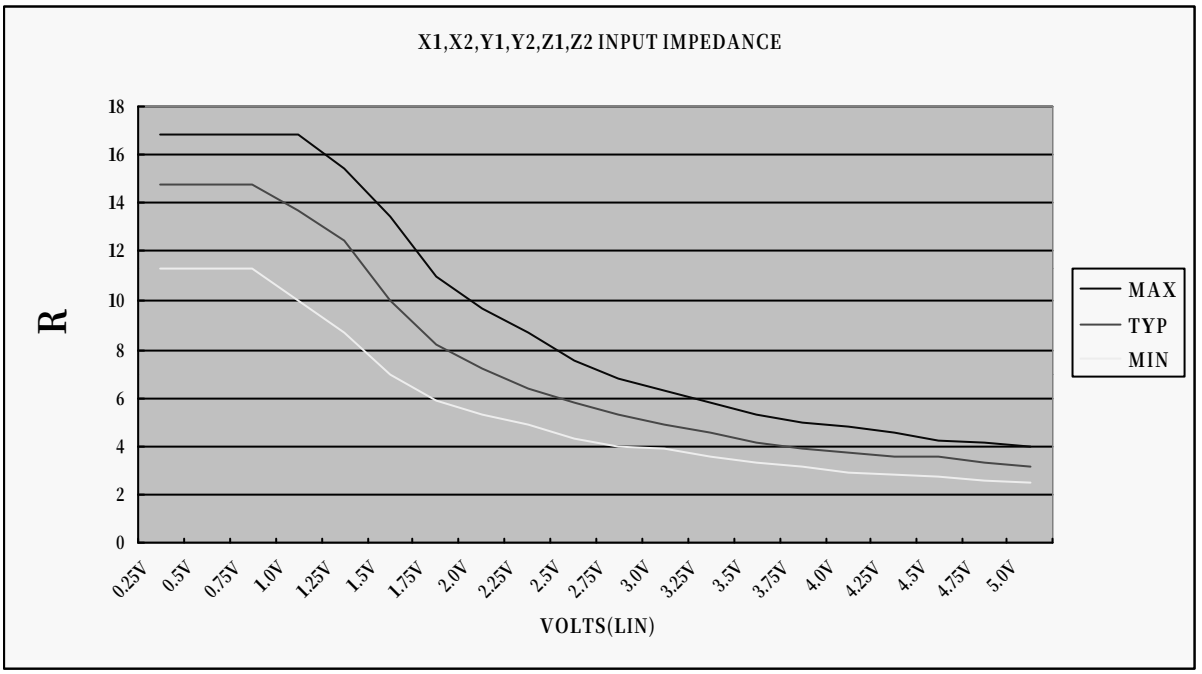


Table 26 MOUSE AC electrical characteristics (T_A = 0℃ to 70℃)

Parameters	Sym.	Min.	Typ.	Max.	Unit
Key Debounce	Tkd	-	12	-	ms
Rising Edge Crossed Width Fosc=35 KHz	Tr	14.3	-	-	us
Falling Edge Crossed Width Fosc=35 KHz	Tf	14.3	-	-	us
Mouse CLK Active Time	Tmca	-	42.9	-	us
Mouse CLK Inactive Time	Tmci	-	42.9	-	us
Mouse Sample DATA from CLK rising Edge	Tmdc	-	14.3	-	us
System CLK Active Time	Tsca	-	42.9	-	us
System CLK Inactive Time	Tsci	-	42.9	-	us
Time from DATA Transition to Falling Edge of CLK	Tsdc	-	14.3	-	us
Time from rising Edge of CLK to DATA Transition	Tscd	-	28.6	-	us
Time to mouse Inhibit after the 11th CLK to ensure mouse does not start another Transmission	Tpi	0	-	50	us

In Oscillating Frequency = 34.3 KHz.

4.12 INFRARED REMOTE APPLICATION MODE

1. Overview & Features

Overview:

EM78P257A/B is designed for use in universal infrared remote commander applications. Fig.26 shows the hardware modulator of EM78P257A/B. It can generate programmable pulse trains for driving an infrared LED.

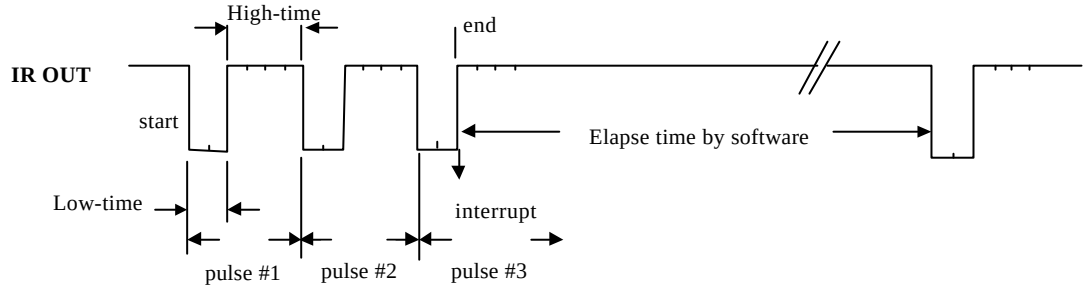
Features:

- Power saving : Idle and Stop modes are provided
- Hardware Modulator providing pulse bursts , with:

-- programmable duty factor for each pulse

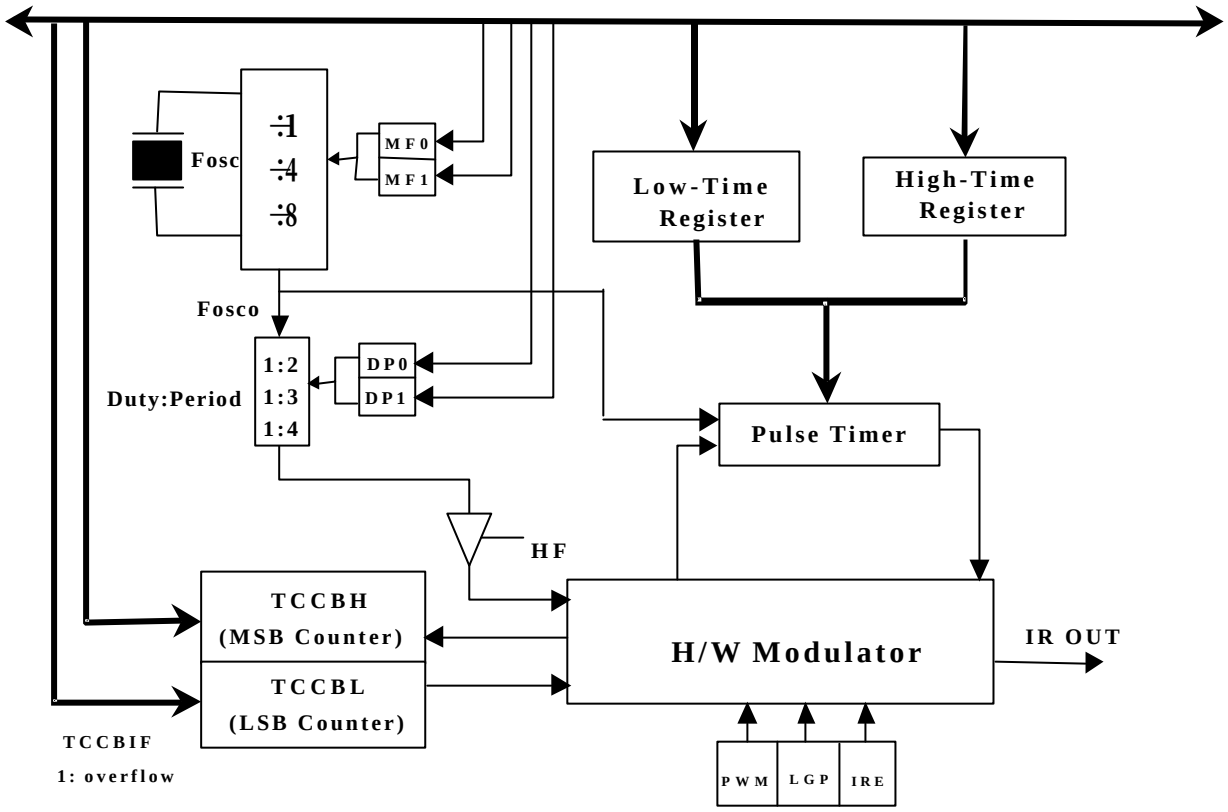
-- programmable number of pulse

- Watchdog timer to keep the transmitter from being locked or malfunction
- On-chip oscillator: 455kHz to 24MHz



Low-time = 2 (Low-time register = 2) High-time = 4(High-time register = 4) number of pulse = 3

Fig. 26 Example Pulse Train Output of IR OUT Pin



<Note> In software design, Low-time and High-time registers cannot set "0" at initial state.

Fig. 27 Hardware Modulator

2. Function Description

The following describes the function of each block and single for Fig.27 which depicts how to complete IR kernel (hardware modulator).

Low-time Register	The 8-bit Low-time register controls the active or Low period of the pulse. The decimal value of its contents determines the number of oscillator cycles indicating that the IR OUT pin is active. The active period of IR OUT can be calculated as follow: t_{Low}=(decimal value held in Low-time register)/fosco
High-time Register	The 8-bit High-time register control the inactive or High period of the pulse. The decimal value of its contents determines the number of oscillator cycles indicating that the IR OUT pin is active. The inactive period of IR OUT can be calculated as follow: t_{High}=(decimal value held in High-time register)/fosco
Pulse Timer	The contents of the Low-time and High-time Latch registers are loaded alternately into the Pulse timer. When loaded, the Pulse timer contents are decremented by "1" every oscillator cycle and upon reaching zero, the Pulse timer will be loaded with the contents of the other register.
IR control register	Contains the bits that control various possibilities for the output pulse

LSB Counter MSB Counter	Loaded by software with the number of pulses required in a pulse burst; loading ' 0' is not allowed.
IRE	Infrared Remote Enable bit
IR OUT	IR output port.I_{IROUT} = 20mA, when the output voltage drops to 2.4V, at Vdd = 5V

2.1 Operation of the Hardware Modulator

1. Enable IRE , set parameter for IR (RD)

2. Load Low-time register (IOC91)

3. Load High-time register (IOCA1)

4. Load MSB and LSB Counter register (IOC61, IOC71)

The Low-time, High-time, MSB Counter, and LSB Counter register are loaded by software. The following instructions is an example for generating five pulses train**:**

```
MOV A,@0B00001000
MOV 0x0D,A          ;(Enable IR)
MOV A, @0x10
IOW 0x08            ;(Enable TCCBH)
BS 0x03,6           ;(Select control register segment 1)
MOV A,@0x10
IOW 0x09            ;(Set Low-Time Register=10h)
MOV A,@0x20
IOW 0x0A            ;(Set High-Time Register=20h)
MOV A,@0x5          ;(Set pulse number = 5   => LSB=5, MSB=0)
IOW 0x06            ;LSB=5
MOV A,@0x00
IOW 0x07            ;MSB=0
```

As soon as the LSB Counter Register is loaded, the Hardware Modulator is started and IR OUT becomes active (LOW). Simultaneously, the contents of the Low-time register are loaded into the Pulse Timer, which is then decremented by ' 1' every oscillator clock cycle. When the value held in the Pulse Timer becomes zero the contents of the LSB & MSB Counter are decremented by ' 1' and IR OUT become inactive (HIGH).

The contents of the High-time register are now loaded into the Pulse Timer which is decremented by ' 1' every oscillator clock cycle. When the value held in the Pulse Timer becomes zero, IR OUT becomes active (LOW). One pulse cycle has now been generated.

The process of alternately loading the contents of the Low-time register and High-time register into the Pulse Timer continues until the contents of the LSB & MSB Counter become zero. When this occurs TCCBIF is asserted; an interrupt to the CPU is generated and the interrupt flag is raised stopping the operation of the Hardware Modulator (If TCCBIF want to be clear ,the IR must be disable firstly). The programmed pulse train has now been generated. If the Hardware Modulator

want to be restarted , we must disable IR in advance and then enable IR again.The time delay between two pulse trains is determined by software.

3. Pin Description

SYMBOL	PIN	DESCRIPTION
P60 to P66	7~13	Standard I/O Port lines, generally used for keypad scanning
P50 to P57	1~4,17~20	Standard I/O Port lines, generally used for keypad sensing
P67(IR OUT)	14	Pulse train output pin, capable of sinking 30mA
OSCO	16	External clock signal input
OSCI	17	External clock signal input
Vdd	15	Power supply
Vss	6	Ground

4. Programmed the Related Registers

When defining IR mode is defined, refer to the related register of its operation as shown in the Table 27 and Table 28 below.

Table 27 Related Control Registers of the IR Mode

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
0x0B	TCR(2)/RB	0	TCCBIE/0	TCCBTS/0	TCCBTE/0	0	TCCCIE/0	TCCCTS/0	TCCCTE/0
0x08	TCCCR/IOC80	TCC2E	TCC4E	TCC6E	TCCBE	-	-	-	-
0x0D	IRCR/RD	DP1/0	DP0/0	MF1/0	MF0/0	IRE/0	HF/0	LGP/0	PWM/0

<Note> *Bit name/initial value

Table 28 Related status/data register of the IR mode

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
0x06	TCCBL/IOC61	TCCBL7	TCCBL6	TCCBL5	TCCBL4	TCCBL3	TCCBL2	TCCBL1	TCCBL0
0x07	TCCBH/IOC71	TCCBH7	TCCBH6	TCCBH5	TCCBH4	TCCBH3	TCCBH2	TCCBH1	TCCBH0
0x09	LTR/IOC91	LTR7	LTR6	LTR5	LTR4	LTR3	LTR2	LTR1	LTR0
0x0A	HTR/IOCA1	HTR7	HTR6	HTR5	HTR4	HTR3	HTR2	HTR1	HTR0
0X0B	PTR/IOCB1	PTR7	PTR6	PTR5	PTR4	PTR3	PTR2	PTR1	PTR0

- TCCBL : An eight-bit clock counter is for the least significant byte of TCCBX. TCCBL, which can be read, written, and cleared at any reset condition.
- TCCBH : An eight-bit clock counter is for the most significant byte of TCCBX. TCCBH, which can be read, written, and cleared at any reset condition.
- Low-time Register :The 8-bit Low-time register that controls the active or Low period of the pulse. The High-time register controls the inactive or High period of the cycle.
- The decimal value of its contents determines the number of oscillator cycles indicating that the IR OUT pin is active. The active period of IR OUT can be calculated as follow:

  t_{Low}=(decimal value held in Low-time register)/fosco
- High-time Register :The 8-bit High-time register control the inactive or High period of the pulse.

- The decimal value of its contents determines the number of oscillator cycles indicating that the IR OUT pin is active. The inactive period of IR OUT can be calculated as follow:

  t_{High}=(decimal value held in High-time register)/fosco

- Pulse timer Register :The contents of the Low-time and High-time registers which are loaded alternately into the Pulse timer. When loaded, the Pulse timer contents are decremented by "1" every oscillator cycle. Upon reaching zero, the Pulse timer will be loaded with the contents of the other register.

Table 29 TCCX Status Register (2)

7	6	5	4	3	2	1	0
-	TCCBIE	TCCBTS	TCCBTE	-	TCCCIE	TCCCTS	TCCCTE

- **Bit 6(TCCBIE)** TCCBIF interrupt enable bit.

  0: disable TCCBIF interrupt

  1: enable TCCBIF interrupt

Table 30 TCCX Control Register

7	6	5	4	3	2	1	0
TCC2E	TCC4E	TCC6E	TCCBE	-	-	-	-

- **Bit 4 (TCCBE):** Control bit which is used to enable most significant byte of counter

  1 = Enable most significant byte of TCCBH.

  0 = Disable most significant byte of TCCBH (default value).

Table 31 IR Control Register

7	6	5	4	3	2	1	0
DP1	DP0	MF1	MF0	IRE	HF	LGP	PWM

- **Bit7:Bit6 (DP1:DP0)** : Duty and Period ratio

DP1	DP0	Ratio
0	0	1:2(default)
0	1	1:3
1	0	1:4
1	1	-

- **Bit 5:Bit 4 (MF1:MF0)** : Modulated frequency

MF1	MF0	Fosco
0	0	Fosc/1
0	1	-
1	0	Fosc/4
1	1	Fosc/8

- **Bit 3(IRE)** Infrared Remote Enable bit

  0: Disable IRE. Disable H/W Modulator Function.

1: Enable IRE. Ignored RB(Bit4(TCCBTE); Bit5(TCCBTS)), and TCCBX set as decrement counter. Enable H/W Modulator Function.

- **Bit 2(HF)** High Frequency. When HF = 1; the Low-time part of the generated pulse is modulated with Frequency Fosco.
- **Bit 1(LGP)** Long Pulse. When LGP = 1; the contents of the High-time register are ignored. A single pulse is generated. Its pulse is determined as shown below.

  Pulse width = (Contents of Low-time register) x (number of pulse) x (1/Fosco)

  If HF = 1; this pulse is modulated with Frequency Fosco (selected by M1,M0).
- **Bit 0(PWM)** Pulse Width Modulation. When PWM = 1 and LGP = 0, the LSB Counter & MSB Counter are disabled, a continuous pulse train is generated, and the output signal is actually a PWM waveform format of PWM.

5. IR mode timing

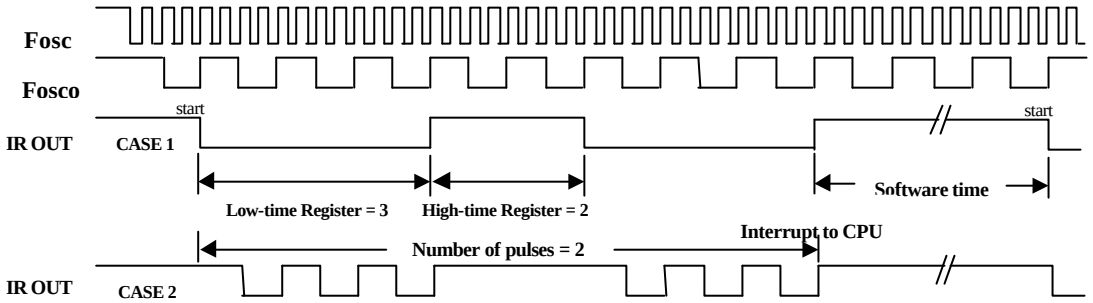


Fig. 28 CASE 1shows a typical pulse train(DP=00;MF=10;HF=0;LGP=0;PWM=0); CASE 2 shows the same pulse train after being modulated with a frequency of 1/4Fosc (DP=00 ;MF=10 ;HF=1;LGP=0;PWM=0).

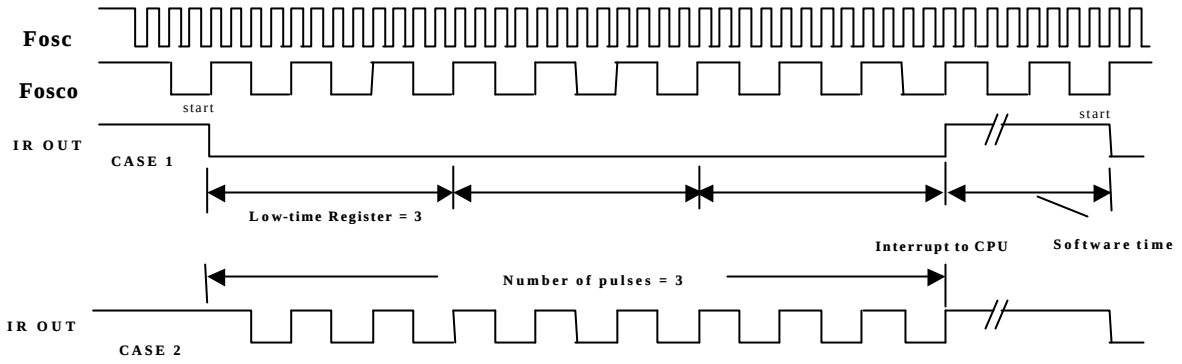


Fig. 29 CASE 1 shows a typical long pulse(DP=00;MF=10;HF=1;LGP=1;PWM=0); CASE 2 shows the same long pulse after being modulated with a frequency of 1/4Fosc (DP=00;MF=10;HF=1;LGP=1;PWM=0).

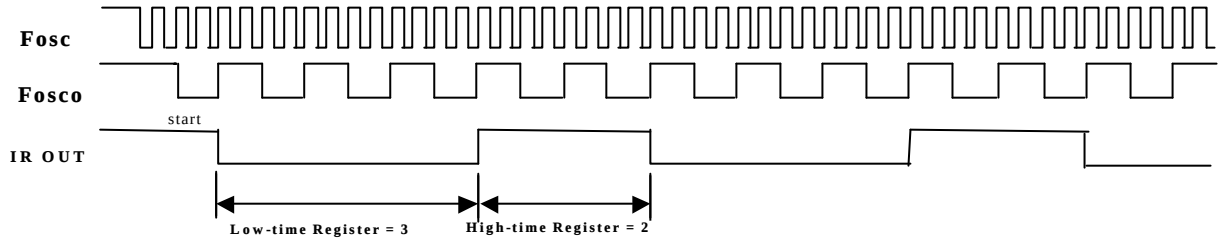


Fig. 30 Continuous pulse train (DP=00;MF=10;HF=0;LGP=0;PWM==1).

4.13 CODE OPTION

EM78P257A/B has one CODE option word and one Customer ID word, which are not a part of the normal program memory.

Word 0	Word 1
Bit12~Bit0	Bit12~Bit0
Code option12~0	Customer' s ID

1. Code Option Register (Word 0)

Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
/RESETEN	/ENWDT	CLKS	OSC2	OSC1	OSC0	/PTB	SUT	TYP	RCOUT	RCM1	RCM0	-

- **Bit 12 (/RESETEN)**: Define Pin4(EM78P257A) or Pin5(EM78P257B) as a reset pin

  0: /RESET enable

  1: /RESET disable

- **Bit 11 (/ENWDT)**: Watchdog timer enable bit.

0: Enable

1: Disable

- **Bit 10 (CLKS)**: Instruction period option bit.

  0: Two clocks

  1: Four clocks

  Refer to the section on Instruction Set.

- **Bit 9, 8 and 7 (OSC2,OSC1 and OSC0)**: Oscillator Modes Selection bits.

Table 32 Oscillator Modes Defined by OSC2,OSC1 and OSC0

Mode	OSC2	OSC1	OSC0
IRC(Internal RC oscillator mode)	1	1	1
IC(Internal C oscillator mode)	1	1	0
ERC(External RC oscillator mode)	1	0	1
HXT(High XTAL oscillator mode)	0	0	1
LXT(Low XTAL oscillator mode)	0	0	0

<Note> The transient point of system frequency between HXT and LXY is around 400 KHz.

- **Bit 6 (/PTB)**: Protect bit.

  0: Enable

  1: Disable

- **Bit 5 (SUT)**: Set-Up Time of device bits.

SUT	*Set-Up Time
1	18 ms
0	1 ms

*Theoretical values, for reference only

- **Bit 4 (TYP)**: Type selection for EM78P257A or EM78P257B.

TYPE	Series
0	EM78P257B
1	EM78P257A

- **Bit 3 (RCOUT)**: A selecting bit of Oscillator Output or I/O port for RC Oscillator.

RCOUT	Pin Function
0	P70
1	OSCO

- **Bit 2, and Bit 1 (RCM1, RCM0)**: IRC mode selection bits

RCM 1	RCM 0	*Frequency(MHz)
1	1	4
1	0	1
0	1	455kHz
0	0	32.768kHz

<Note> *Theoretical values, for reference only. In fact, the values may be inaccurate by ±35%.

- **Bit0** : Not used

2. Customer ID Register (Word 1)

Bit12~Bit0
XXXXXXXXXXXXX

• Bit 12~ 0: Customer' s ID code

4.14 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g. "SUB R2,A", "BS(C) R2,6", "CLR R2", ····). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows:

(A) Modify one instruction cycle to consist of 4 oscillator periods.

(B) Execute within two instruction cycles the "JMP", "CALL", "RET", "RETL", "RETI" commands, or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") which were tested to be true. The instructions that are written to the program counter, should also take two instruction cycles.

Case (A) is selected by the CODE Option bit, called CLKS. One instruction cycle consists of two oscillator clocks if CLKS is low, and four oscillator clocks if CLKS is high.

Note that once 4 oscillator periods within one instruction cycle is selected under Case (A), the internal clock source to TCC will be CLK=Fosc/4 (not Fosc/ 2) as illustrated in Fig.6.

In addition, the instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

The symbol "R" represents a register designator that specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction. "b" represents a bit field designator that selects the value for the bit which is located in the register "R", and affects the operation. "k" represents an 8 or 10-bit constant or literal value.

Table 33 The List of the Instruction Set of EM78P257A/B

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 0000 0000 0000	0000	NOP	No Operation	None

0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None <Note1>
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None <Note1>
0 0000 0010 0000	0020	TBL	R2+A → R2 Bit8,9 do not clear	Z,C,DC
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z,C,DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z,C,DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ VR → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ VR → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z,C,DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z,C,DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None <Note2>
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None <Note3>
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None

1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC
1 1110 0000 0001	1E01	INT	PC+1 → [SP], 001H → PC	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC

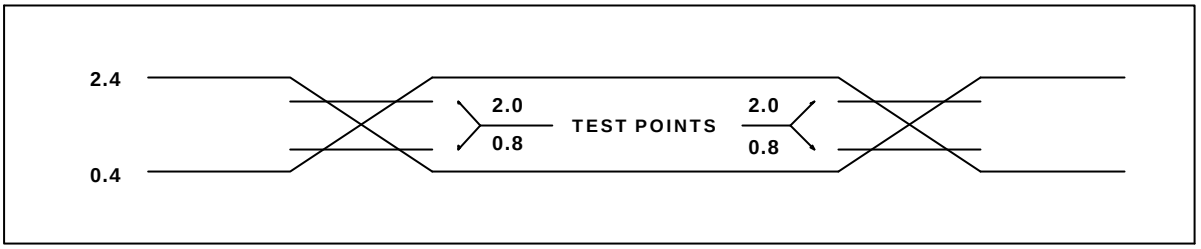
<Note 1> This instruction is applicable to IOC50~IOC60, IOCB0~IOCF0 only.

<Note 2> This instruction is not recommended for RF operation.

<Note 3> This instruction cannot operate under RF.

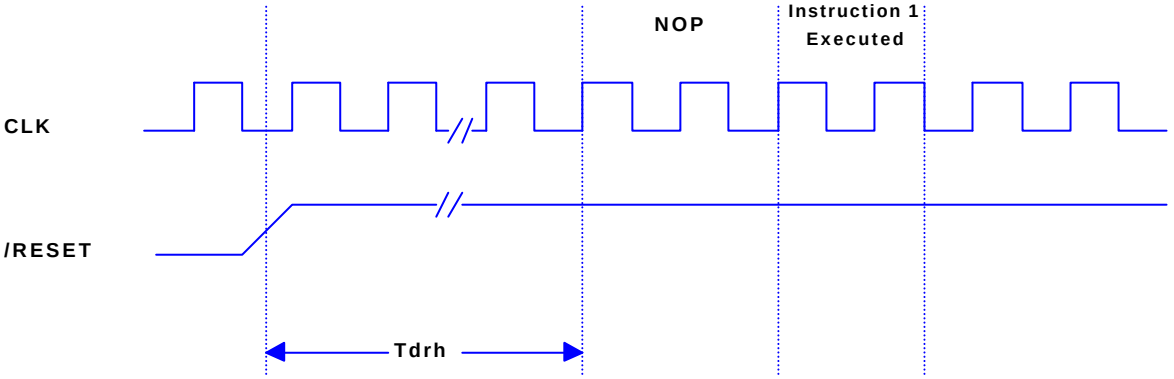
4.15 Timing Diagrams

AC Test Input/Output Waveform

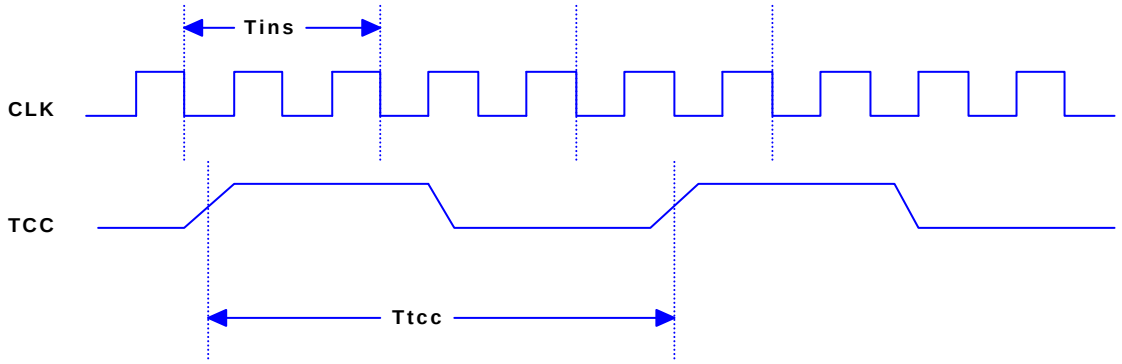


AC Testing : Input is driven at 2.4V for logic "1",and 0.4V for logic "0".Timing measurements are made at 2.0V for logic "1",and 0.8V for logic "0".

RESET Timing (CLK="0")



TCC Input Timing (CLKS="0")



5. ABSOLUTE MAXIMUM RATINGS

Items	Rating		
Temperature under bias	0°C	to	70°C
Storage temperature	-65°C	to	150°C
Input voltage	-0.3V	to	+6.0V
Output voltage	-0.3V	to	+6.0V

6. ELECTRICAL CHARACTERISTICS

6.1 DC Electrical Characteristic

(Ta=0~70° C, VDD=5.0V±5%, VSS=0V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Fxt	XTAL (VDD to 2.3V)	Two cycle with two clocks	DC		4	MHz
	XTAL (VDD to 3V)		DC		8	MHz
	XTAL (VDD to 5V)		DC		20	MHz
	ERC (VDD to 5V)	R: 5.1KΩ, C: 100 pF	F±30%	830	F±30%	KHz
	IRC (VDD to 5 V)	4MHz, 1MHz, 455KHz, 32.768KHz	F±35%	F	F±35%	Hz
	IC, ER (VDD to 5V)	R: 51KΩ	F±30%	4.3	F±30%	MHz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS			±1	µA
VIH1	Input High Voltage (VDD=5V)	Ports 5, 6	2.0			V
VIL1	Input Low Voltage (VDD=5V)	Ports 5, 6			0.8	V
VIHT1	Input High Threshold Voltage (VDD=5V)	/RESET, TCC	2.0			V
VILT1	Input Low Threshold Voltage (VDD=5V)	/RESET, TCC			0.8	V
VIHX1	Clock Input High Voltage ,(VDD=5V)	OSCI	2.5			V
VILX1	Clock Input Low Voltage(VDD=5V)	OSCI			1.0	V
VIH2	Input High Voltage (VDD=3V)	Ports 5, 6	1.5			V
VIL2	Input Low Voltage (VDD=3V)	Ports 5, 6			0.4	V
VIHT2	Input High Threshold Voltage (VDD=3V)	/RESET, TCC	1.5			V
VILT2	Input Low Threshold Voltage (VDD=3V)	/RESET, TCC			0.4	V
VIHX2	Clock Input High Voltage (VDD=3V)	OSCI	1.5			V
VILX2	Clock Input Low Voltage (VDD=3V)	OSCI			0.6	V
VOH1	Output High Voltage (Ports 5, 6)	IOH = -9.0 mA	2.4			V
VOL1	Output Low Voltage (Ports 5, 6)	IOL = 9.0 mA			0.4	V
VOH2	Output High Voltage (P67 set to IR OUT)	IOH = -20.0 mA	2.4			V
VOL2	Output Low Voltage (P67 set to IR OUT)	IOL = 20.0 mA			0.4	V
IPH	Pull-high current	Pull-high active, input pin at VSS	-50	-100	-240	µA
IPD	Pull-down current	Pull-down active, input pin at VDD	25	50	120	µA
ISB1	Power down current	All input and I/O pins at VDD, output pin floating, WDT disabled			1	µA
ISB2	Power down current	All input and I/O pins at VDD, output pin floating, WDT enabled		1	10	µA
ICC1	Operating supply current (VDD=3V) at two clocks	/RESET= 'High', Fosc=32KHz (Crystal type, two clocks), output pin floating, WDT disabled		15	30	µA
ICC2	Operating supply current (VDD=3V) at two clocks	/RESET= 'High', Fosc=32KHz (Crystal type, two clocks), output pin floating, WDT enabled		19	35	µA
ICC3	Operating supply current (VDD=5.0V) at two clocks	/RESET= 'High', Fosc=2MHz (Crystal type, two clocks), output pin floating			2.0	mA
ICC4	Operating supply current (VDD=5.0V) at two clocks	/RESET= 'High', Fosc=4MHz (Crystal type, two clocks), output pin floating			4.0	mA

* These parameters are characterizes and tested.

* Data in the Minimum, Typical, Maximum(“Min”,“Typ”,”Max”) column are based on characterization results at 25℃. This data is for design guidance and is tested.

6.2 AC Electrical Characteristic

(Ta=0~70° C, VDD=5V±5%, VSS=0V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle		45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type RC type	100 500		DC DC	ns ns
Ttcc	TCC input period		(Tins+20)/N*			ns
Tdrh	Device reset hold time	Ta = 25°C	10.78	15.4	20.2	ms
Trst	/RESET pulse width	Ta = 25°C	2000			ns
Twdt1*	Watchdog timer period	Ta = 25°C	10.78	15.4	20.2	ms
Twdt2*	Watchdog timer period	Ta = 25°C	0.75	1.07	1.39	ms
Tset	Input pin setup time			0		ms
Thold	Input pin hold time			20		ms
Tdelay	Output pin delay time	Cload=20pF		50		ms

* Twdt1: The Option word (SUT) is used to define the oscillator Set-Up time. WDT timeout length is the same as set-up time(18ms).

* Twdt2: The Option word (SUT) is used to define the oscillator Set-Up time. WDT timeout length is the same as set-up time(1ms).

* These parameters are characterizes but not tested.

* Data in the Minimum, Typical, Maximum(“Min”,“Typ”,”Max”) column are based on characterization results at 25℃. This data is for design guidance and is not tested.

* N= selected prescaler ratio.

* The duration of watch dog timer is determined by option code (bit5).

6.3 Device Characteristic

The graphs provided following note that based on a limited number of samples and they are provided for information only. The device characteristic listed herein is not guaranteed. In some graphs, the data maybe out of the specified operating warranted range.

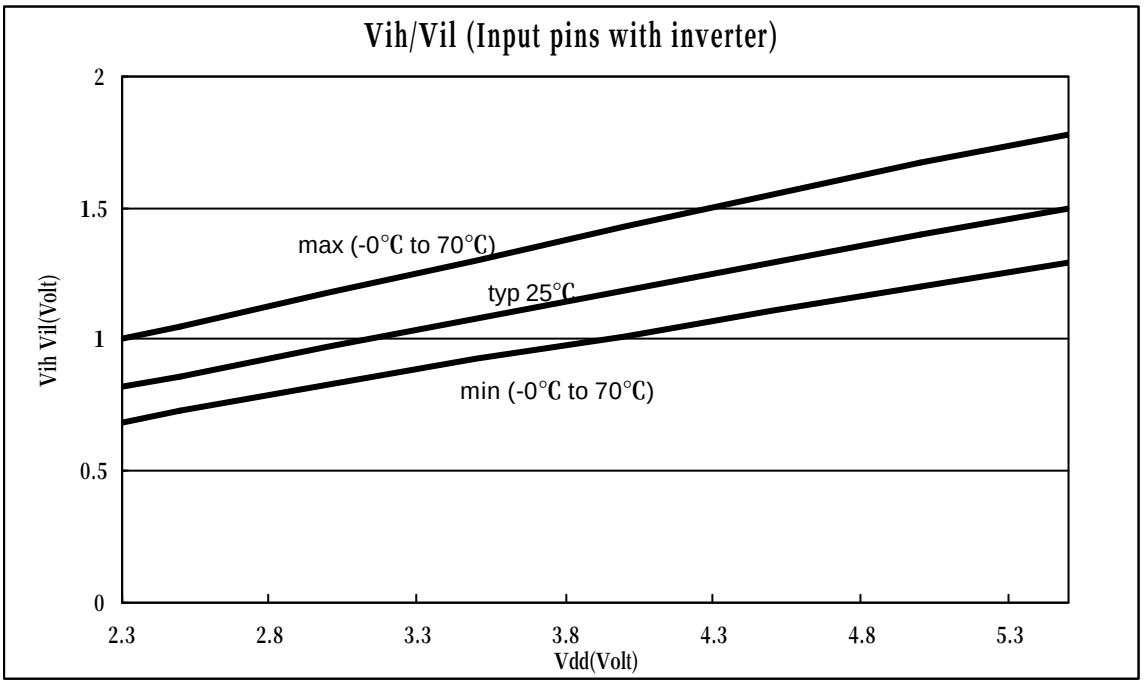


Fig. 31 Vth (Threshold voltage) of Port5, Port6 and Port7 vs. VDD

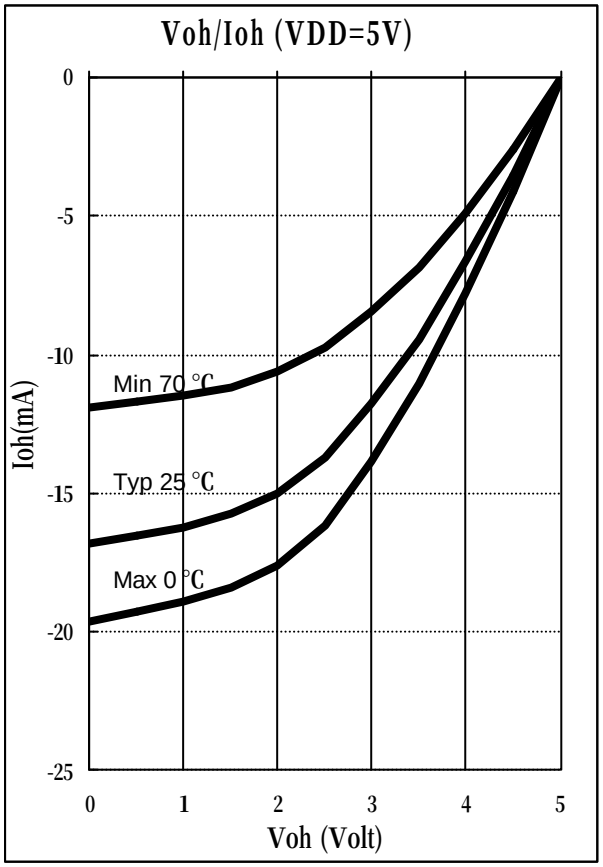


Fig. 32 Port5, Port6 and Port7 Voh vs. Ioh, VDD=5V

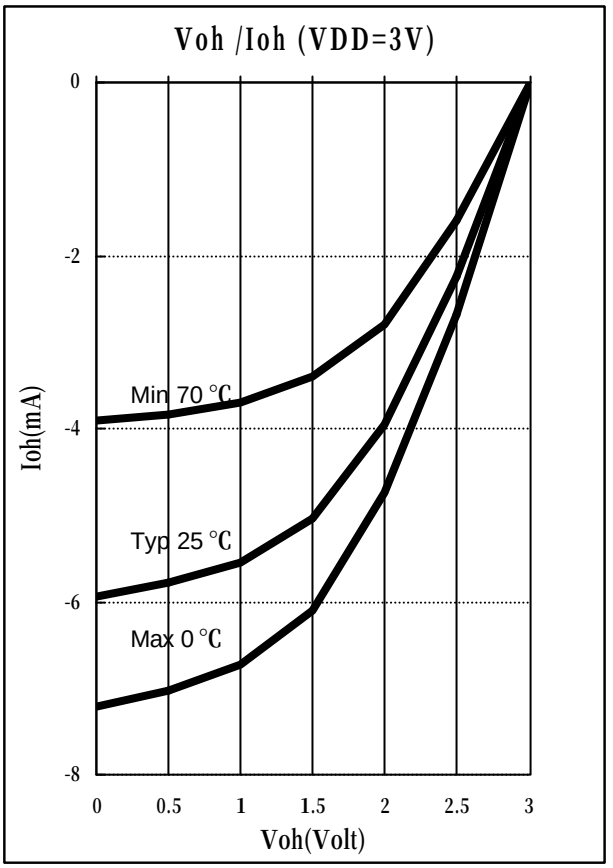


Fig. 33 Port5, Port6 and Port7 Voh vs. Ioh, VDD=3V

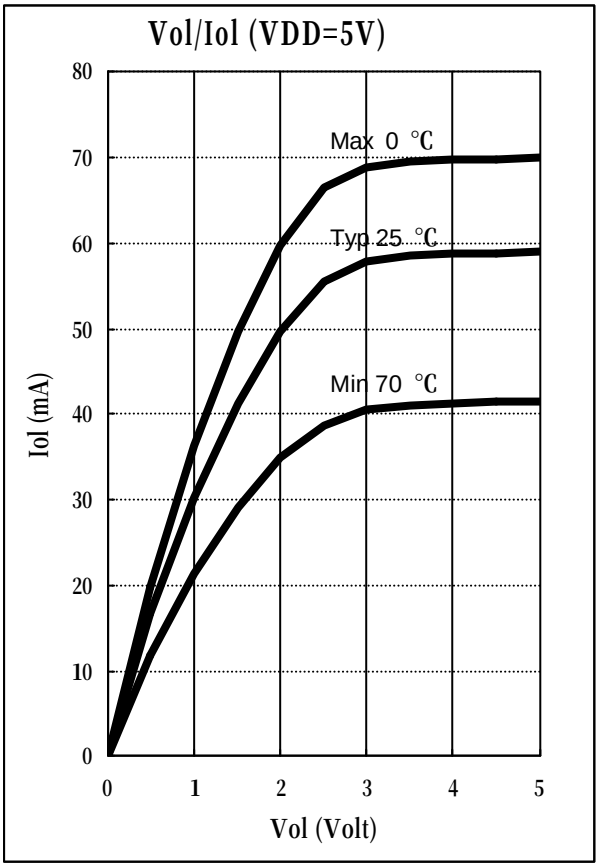


Fig. 34 Port5, Port6 and Port7 Vol vs. Iol, VDD=5V

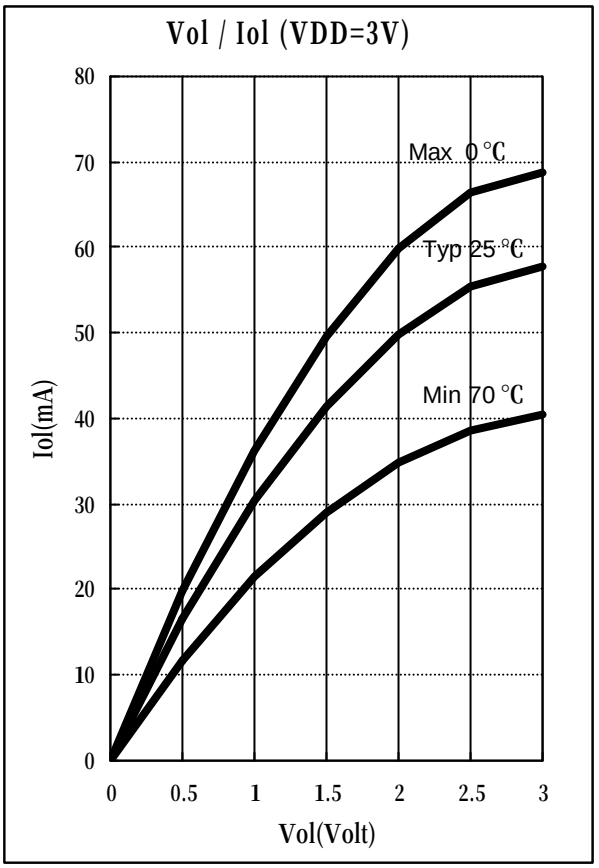


Fig. 35 Port5, Port6 and Port7 Vol vs. Iol VDD=3V

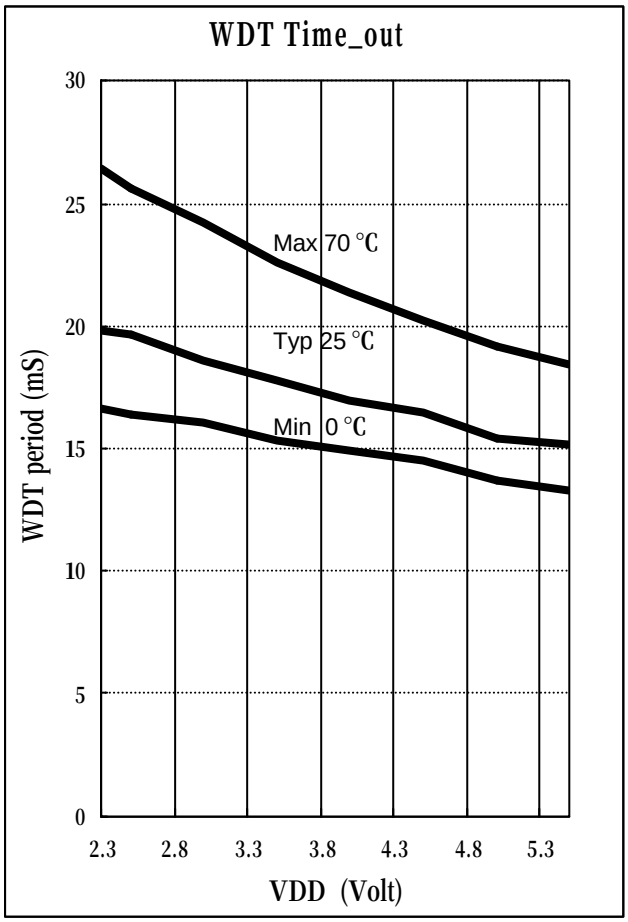


Fig. 36 WDT time out period vs. VDD

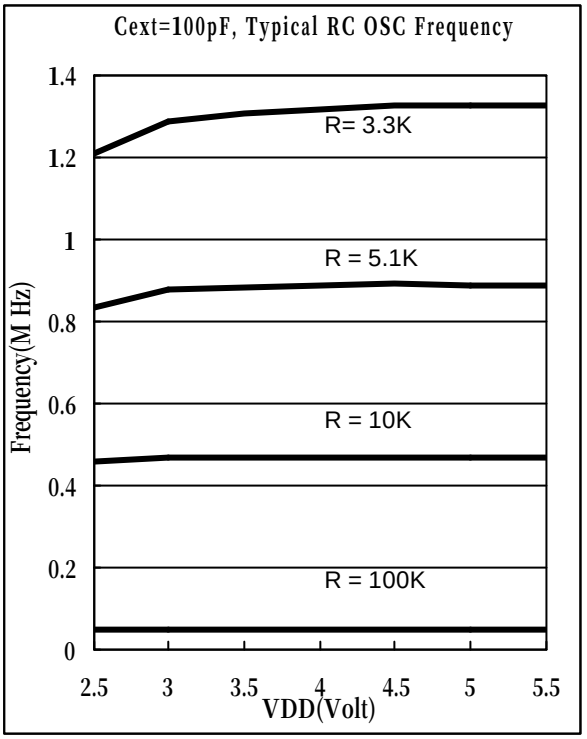


Fig. 37 Typical RC OSC Frequency vs. VDD (Cext=100pF, Temperature at 25℃)

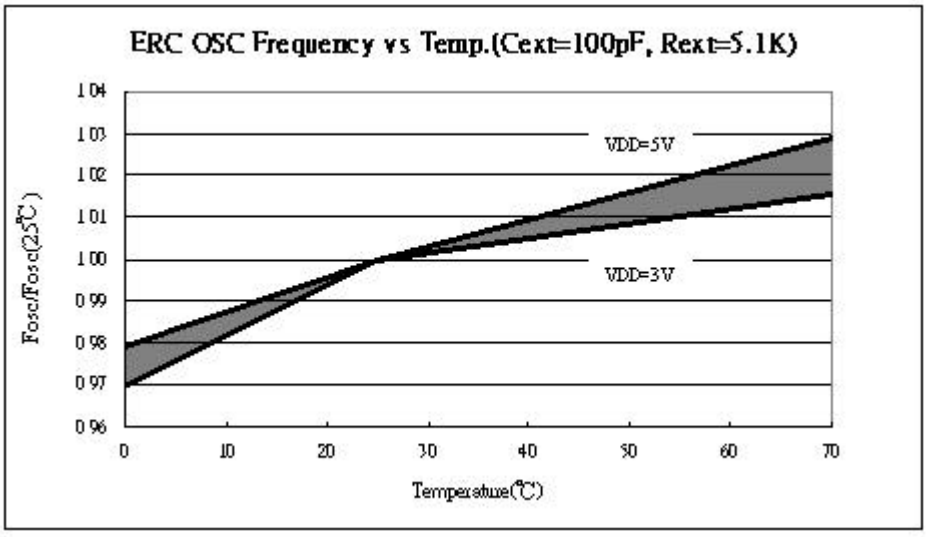


Fig. 38 Typical RC OSC Frequency vs. Temperature (R and C are ideal components)

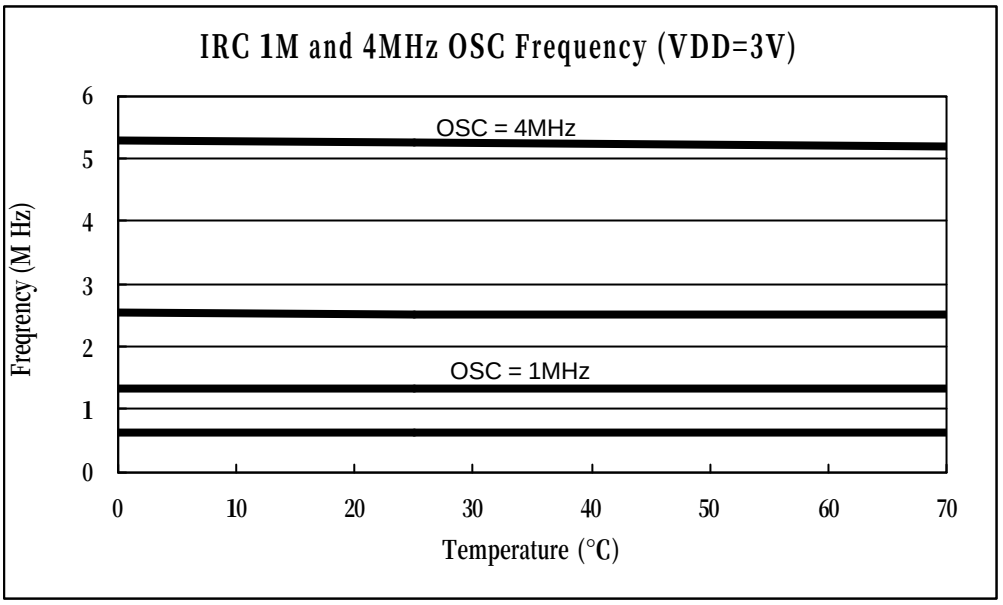


Fig. 39 Internal RC 1M and 4MHz OSC Frequency vs. Temperature Join Process Drifts, VDD=3V

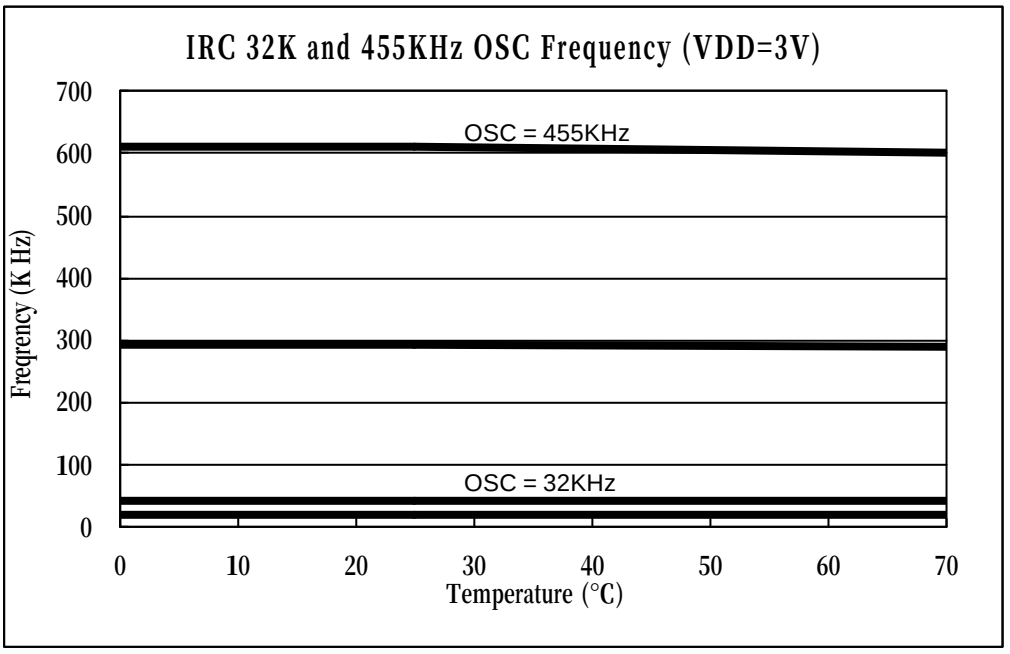


Fig. 40 Internal RC 32K and 455KHz OSC Frequency vs. Temperature Join Process Drifts, VDD=3V

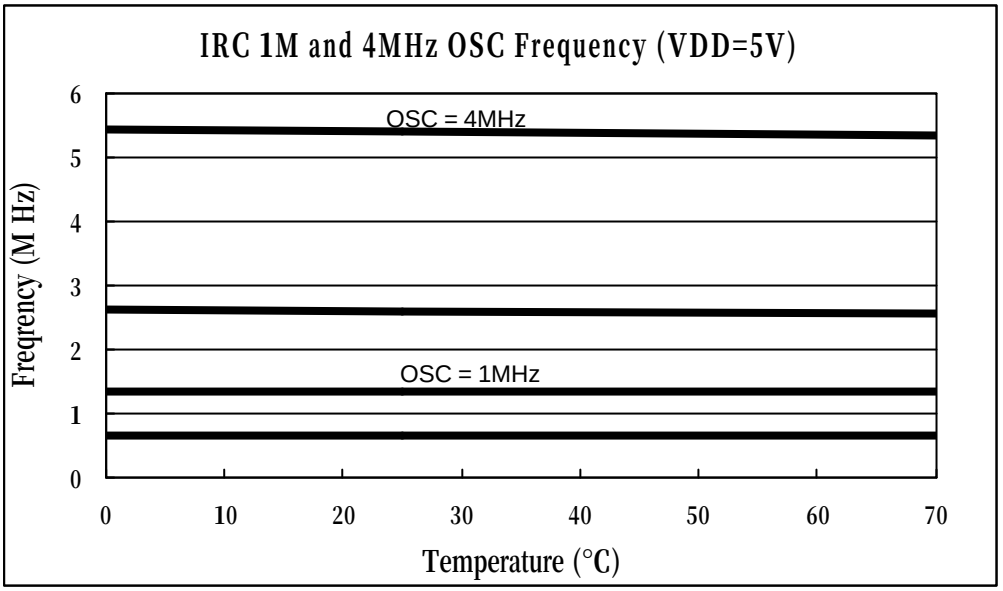


Fig. 41 Internal RC 1M and 4MHz OSC Frequency vs. Temperature Join Process Drifts, VDD=5V

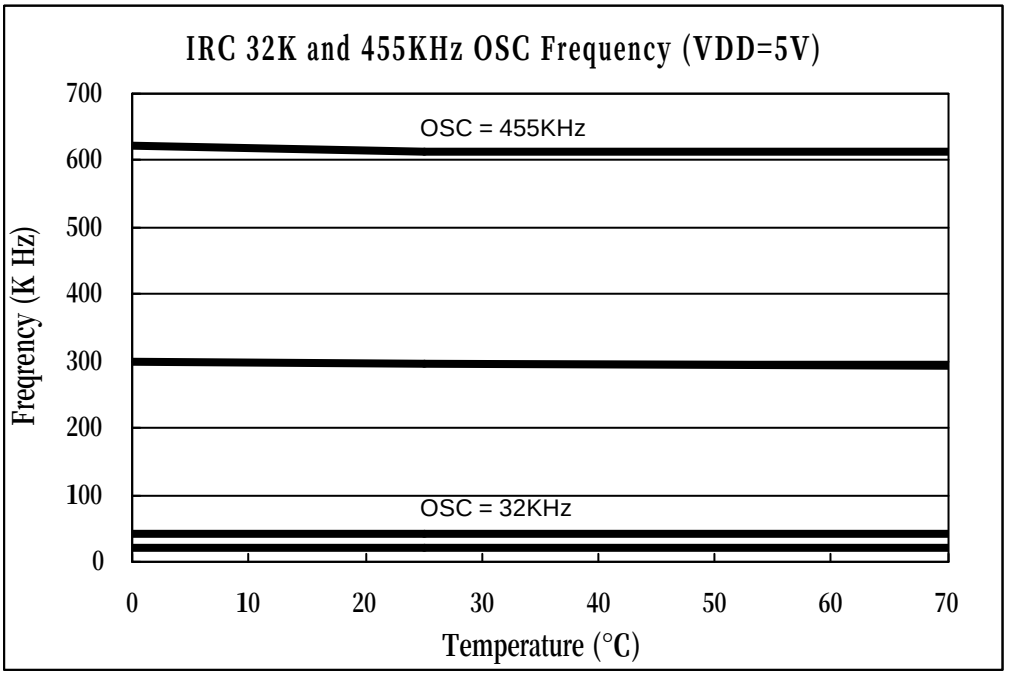


Fig. 42 Internal RC 32K and 455KHz OSC Frequency vs. Temperature Join Process Drifts VDD=5V

Four conditions exist with the Operating Current ICC1 to ICC4. These conditions are as follows:

ICC1: VDD=3V, Fosc=32K Hz, 2 clocks, WDT disable

ICC2: VDD=3V, Fosc=32K Hz, 2 clocks, WDT enable

ICC3: VDD=5V, Fosc=2M Hz, 2 clocks, WDT enable

ICC4: VDD=5V, Fosc=4M Hz, 2 clocks, WDT enable

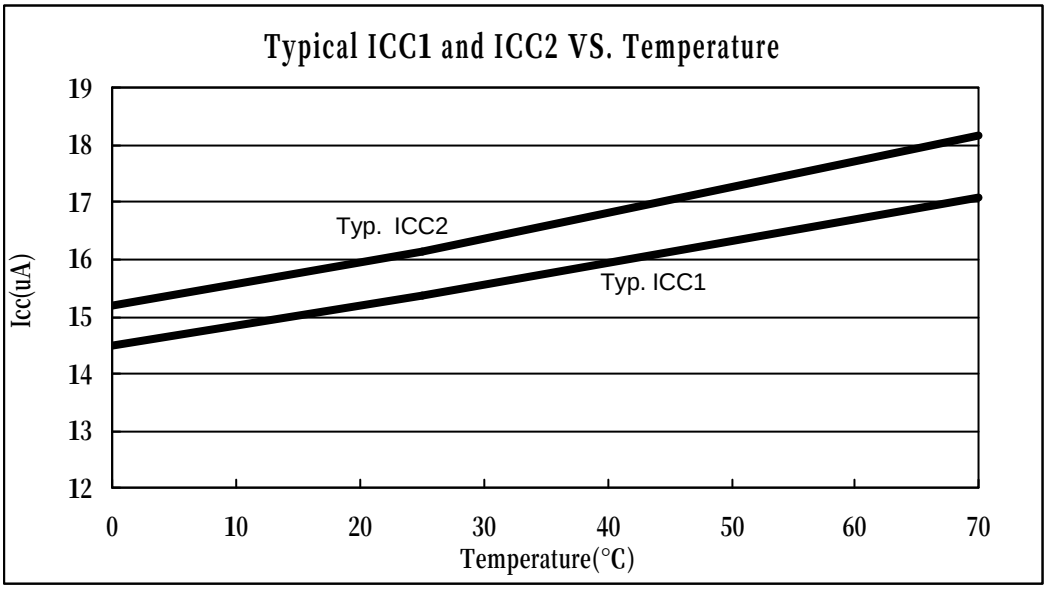


Fig. 43 Typical operating current (ICC1 and ICC2) vs. Temperature

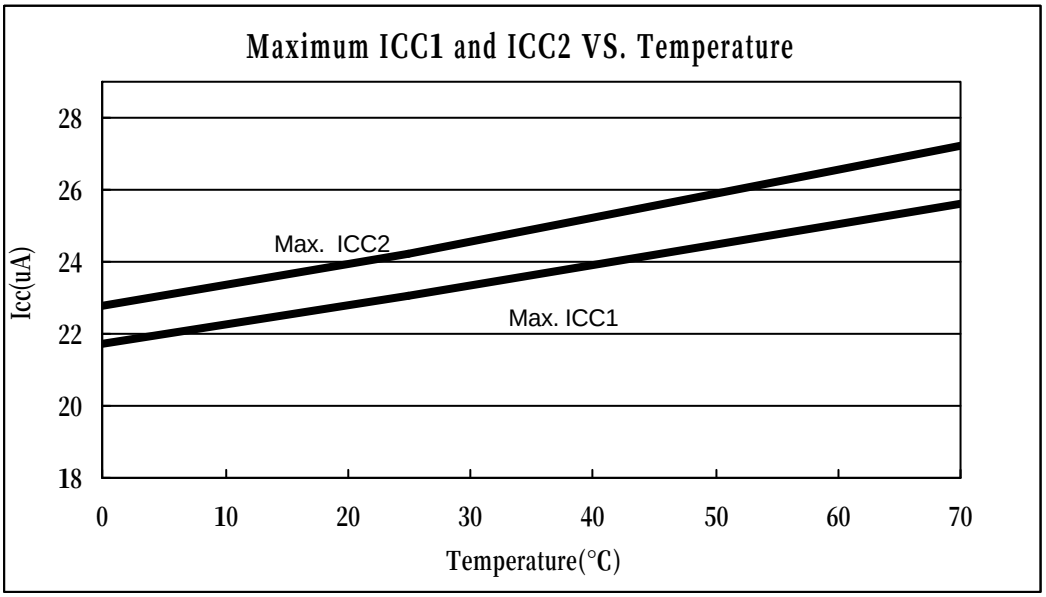


Fig. 44 Maximum operating current (ICC1 and ICC2) vs. Temperature

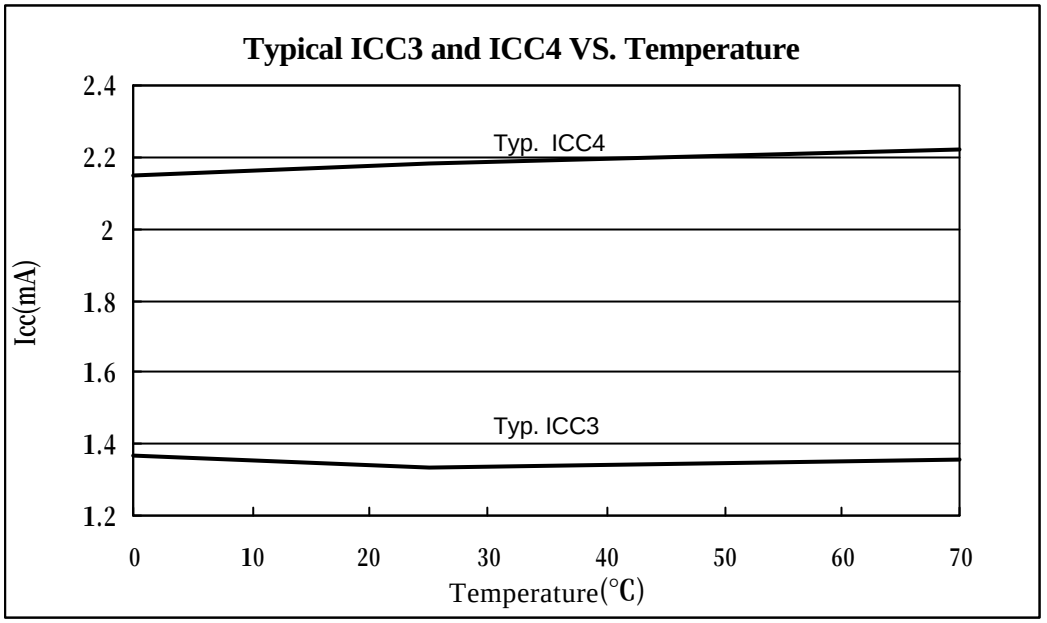


Fig. 45 Typical operating current (ICC3 and ICC4) vs. Temperature

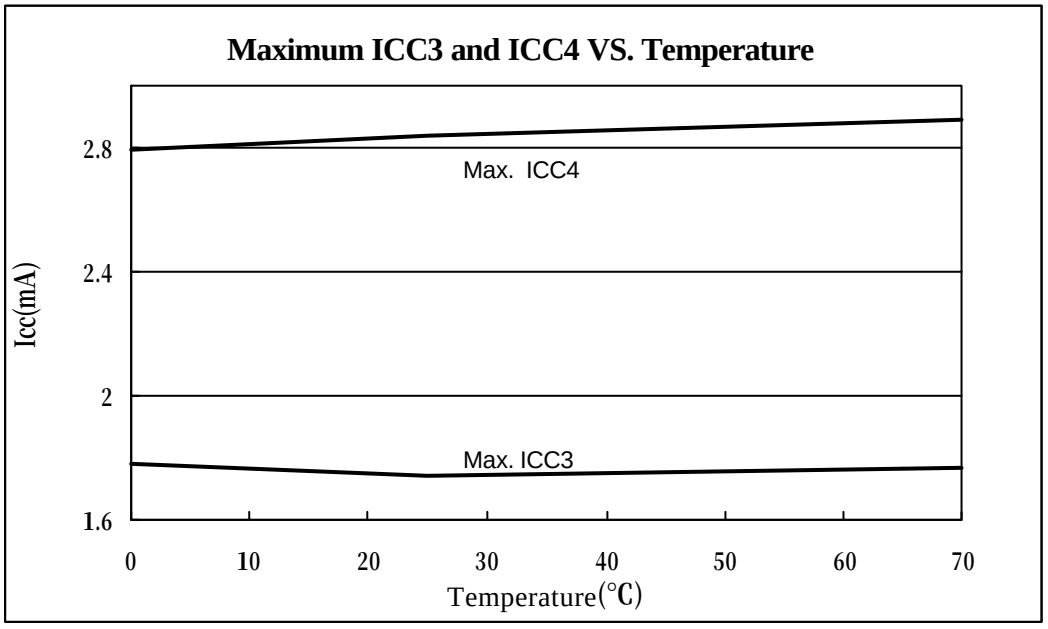


Fig. 46 Maximum operating current (ICC3 and ICC4) vs. Temperature

Two conditions exist with the Standby Current ISB1 and ISB2. These conditions are as follows:

ISB1: VDD=5V, WDT disable

ISB2: VDD=5V, WDT enable

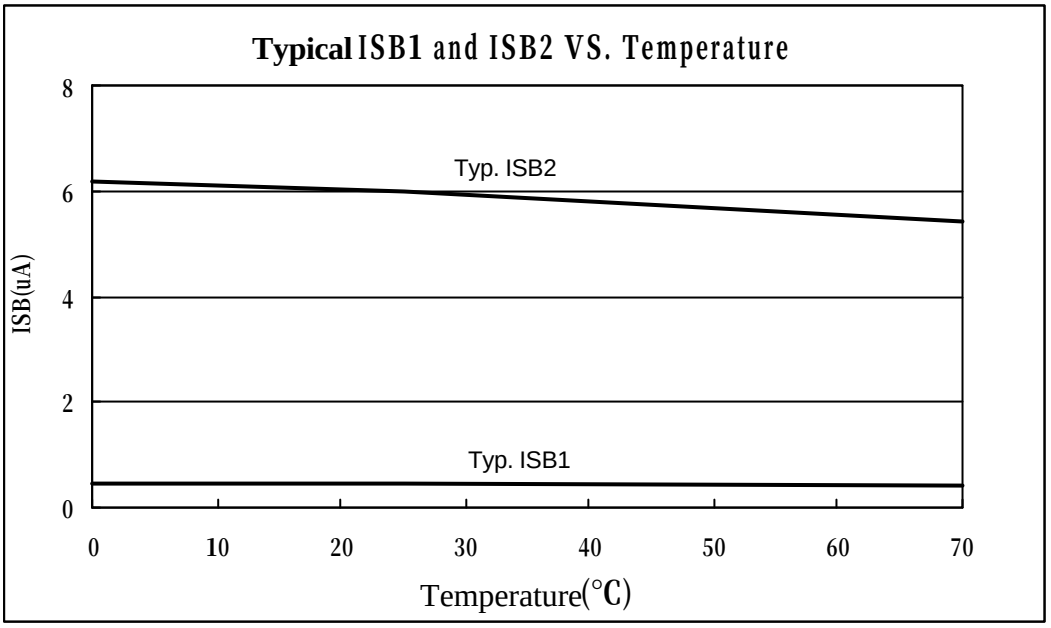


Fig. 47 Typical standby current (ISB1 and ISB2) vs. Temperature

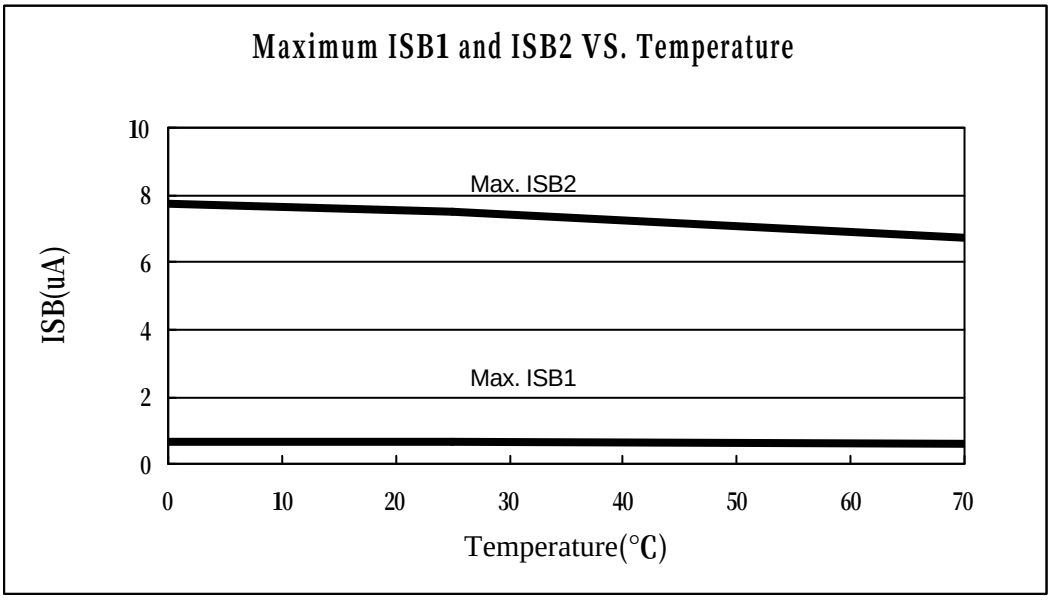


Fig. 48 Maximum standby current (ISB1 and ISB2) vs. Temperature

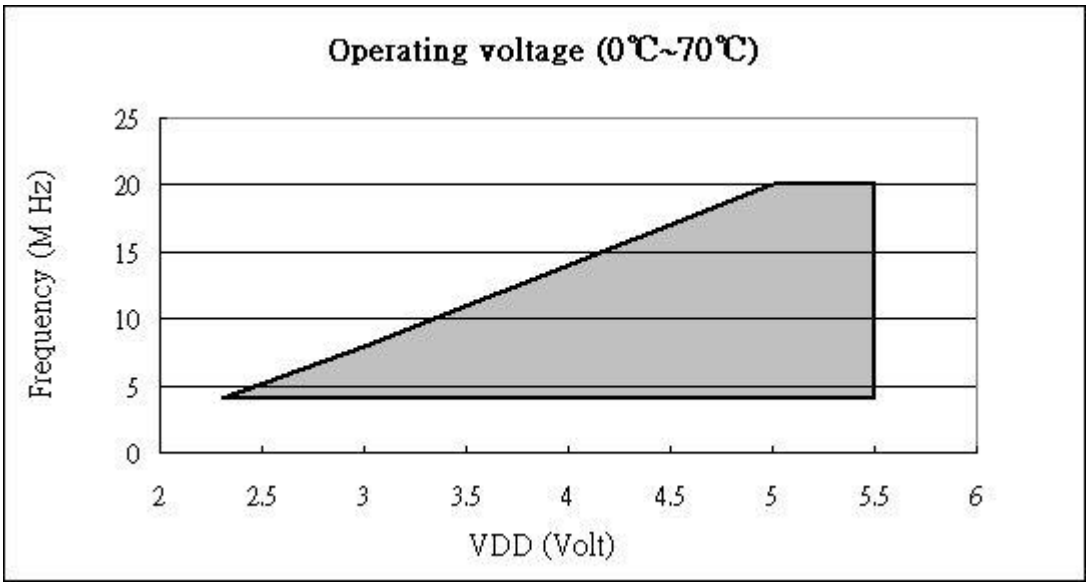


Fig. 49 Operating voltage under temperature range of 0℃ to 70℃

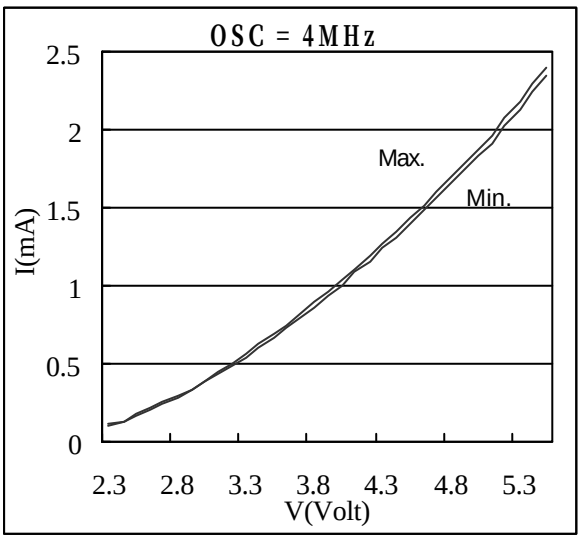


Fig. 50 V-I curve in operating mode, operating frequency is 4MHz

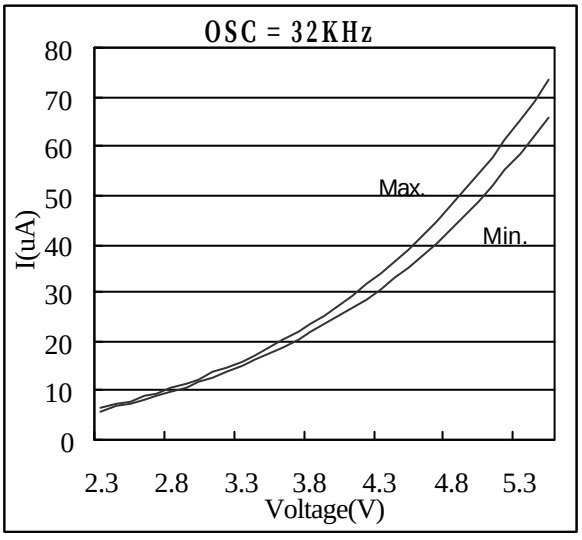


Fig. 51 V-I curve in operating mode, operating frequency is 32K Hz

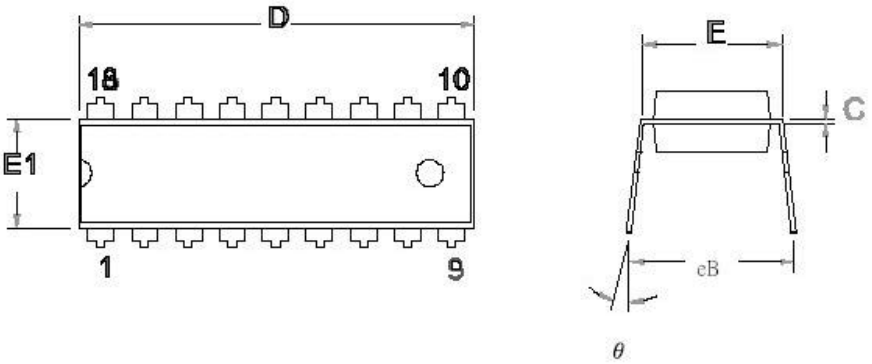
APPENDIX

Package Types

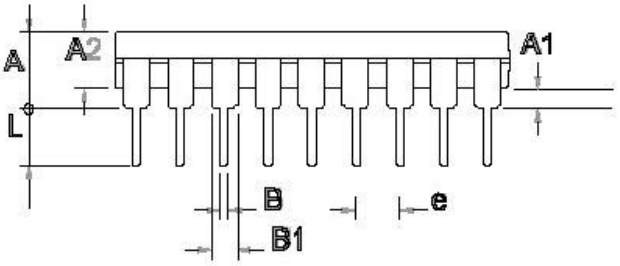
OTP MCU	Package Type	Pin Count	Package Size
EM78P257AP	DIP	18	300mil
EM78P257AM	SOP	18	300mil
EM78P257AKM	SSOP	20	209mil
EM78P257BP	DIP	20	300mil
EM78P257BM	SOP	20	300mil

Package Information

18-Lead Plastic Dual in line (PDIP) – 300 mil

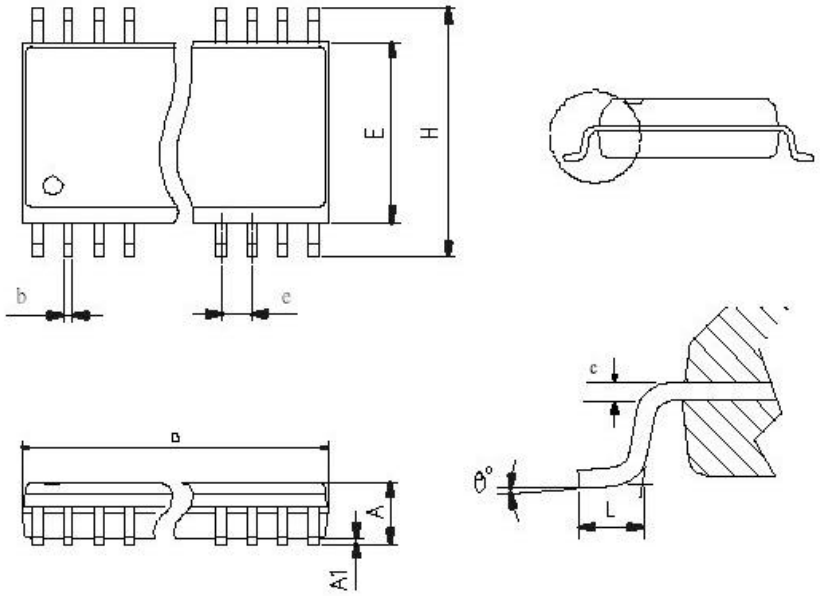


Symbal	Min	Normal	Max
A			4.450
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	22.610	22.860	23.110
E1	6.220	6.438	6.655
E	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ	0		15



TITLE: PDIP-18L 300MIL PACKAGE OUTLINE DIMENSION	
File : D18	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

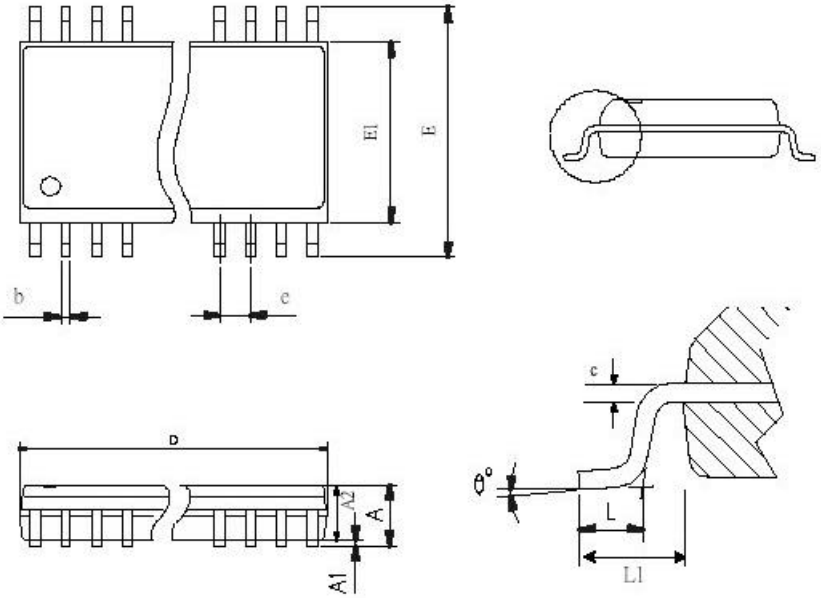
18-Lead Plastic Small Outline (SOP) – 300 mil



Symbal	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b	0.406(TYP)		
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	11.350		11.750
L	0.406	0.838	1.270
e	1.27(TYP)		
θ°	0		8

TITLE: SOP-18L(300MIL) PACKAGE OUTLINE DIMENSION	
File : SO18	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

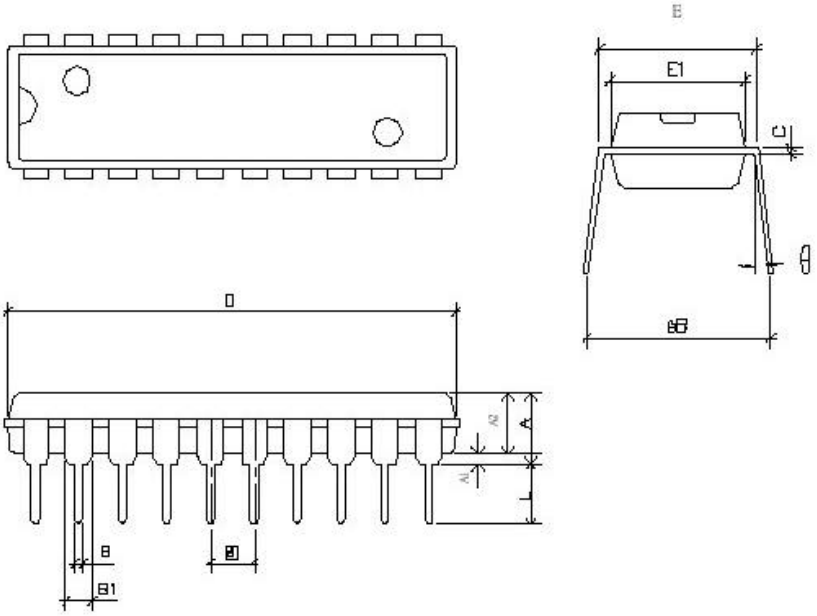
20- Lead Plastic Shrink Small Outline (SSOP) – 209 mil



Symbol	Min	Normal	Max
A			2.130
A1	0.050		0.250
A2	1.620	1.750	1.880
b	0.220		0.380
c	0.090		0.200
E	7.400	7.800	8.200
E1	5.000	5.300	5.600
D	6.900	7.200	7.500
L	0.650	0.750	0.850
L1	1.250(REF)		
e	0.650(TYP)		
θ°	0	4	8

TITLE: SSOP-20L(209MIL) OUTLINE PACKAGE PACKA OUTLINE DIMENSION	
File : SSOP20	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

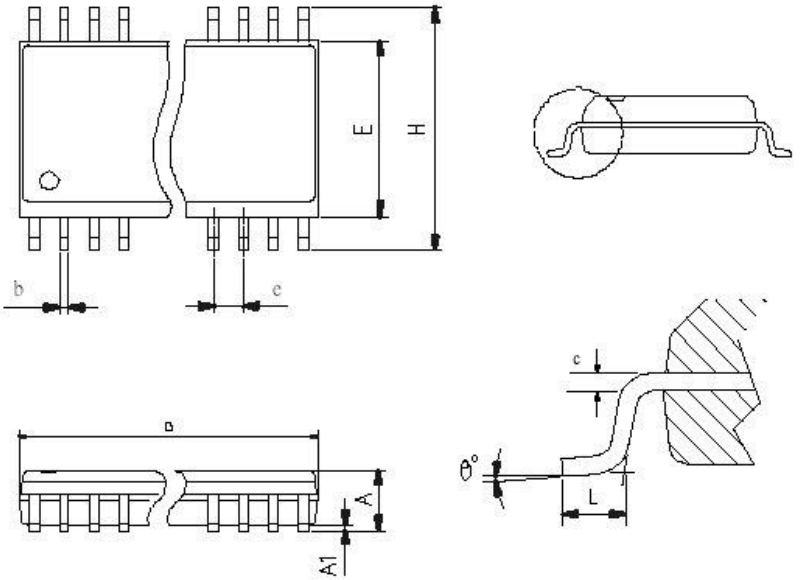
20-Lead Plastic Dual in line (PDIP) – 300 mil



Symbal	Min	Normal	Max
A			4.450
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	25.883	26.060	26.237
E1	6.220	6.438	6.655
E	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ	0		15

TITLE: PDIP-20L 300MIL PACKAGE OUTLINE DIMENSION	
File : D20	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

20-Lead Plastic Small Outline (SOP) – 300 mil



Symbal	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b	0.406(TYP)		
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	12.600		12.900
L	0.630	0.838	1.100
e	1.27(TYP)		
θ°	0		8

TITLE: SOP-20L(300MIL) PACKAGE OUTLINE DIMENSION	
File : SO20	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

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