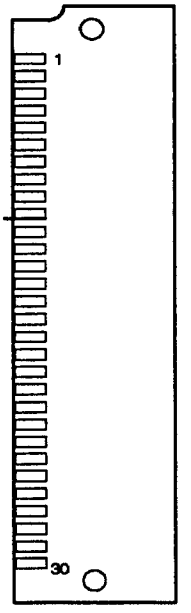
DALLAS SEMICONDUCTOR

DS2217
Nonvolatile SRAM Stik 128K x 9

FEATURES

- Data retention in the absence of V_{CC}
- Directly replaces volatile SRAM
- Employs popular JEDEC standard 30-position SIMM connection scheme
- Nonvolatile circuitry transparent to and independent from host system
- No additional components
- 10 years of data retention
- Organized as 128K bytes
- Available in 120ns, 150ns, and 200ns read access times
- Full ± 10% operating range
- Read cycle time equals write cycle time
- Unlimited write cycles
- Automatic write protection circuitry safeguards against data loss
- Wide operating temperature range of 0°C to 70°C

PIN DESCRIPTION



30-Pin SIP Stik

PIN NAMES (\ Denotes Condition Low)

V_{CC}	-+5 volt supply
GND	-Ground
A_0-A_{16}	-Address Inputs
DQ_0-DQ_7	-Data Input/Output
CE\	-Chip Enable
OE\	-Output Enable
WE\	-Write Enable

DESCRIPTION

The DS2217 Nonvolatile SRAM Stik 128K x 9 is a self-contained, 1,048,576-bit nonvolatile static RAM organized as 131,072 words by 8 bits. The nonvolatile memory contains all necessary control circuitry and energy sources to maintain data integrity in the absence of power for more than 10 years. The DS2217 conforms to the popular 30-position SIMM pinout and requires no additional circuitry.

OPERATION

The DS2217 SRAM Stik is used like any standard static RAM. All the nonvolatile circuitry resides transparently to the user. Decoding from upper order address lines is also integrated into the nonvolatile controller and is transparent to SRAM operation. Connection to the DS2217 is made with an industry standard, 30-position SIMM socket (AMP part number 643930-1). These SIMM sockets are also available in double-row and low-profile angled variations.

READ MODE

The DS2217 is executing a read cycle whenever WE\ (write enable) is inactive (high) and CE\ (chip enable) is active (low). The unique address specified by the 17 address inputs (A0-A16) defines which byte of data is to be accessed. Valid data will be available to the eight data I/O pins within t_{ACC} (access time) after the last address input signal is stable, providing that CE\ and OE\ (output enable) access times are satisfied. If OE\ and CE\ times are not satisfied, then data access must be measured from the later occurring signal (CE\ or OE\) and the limiting parameter is either t_{CO} for CE\ or t_{OE} for OE\ rather than address access. Read cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is inhibited and all accesses are ignored.

WRITE MODE

The DS2217 is in the write mode whenever both WE\ and CE\ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of CE\ or WE\ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE\ or WE\. All address inputs must be kept valid throughout the write cycle. WE\ must return to the high state for a minimum recovery time (t_{WR}) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE\ and OE\ active) then WE\ will disable the outputs in t_{ODW} from its falling edge. Write cycles can occur only when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is write-protected.

DATA RETENTION MODE

The nonvolatile Stik provides full functional capability for V_{CC} greater than 4.5 volts and guarantees write protection for V_{CC} less than 4.5 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS2217 constantly monitors V_{CC}. Should the supply voltage decay, the RAM is automatically write-protected below 4.5 volts. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects a lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects the external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

The DS2217 checks battery status to warn of potential data loss. Each time that V_{CC} power is restored to the DS2217, the battery is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering data. If the next read cycle fails to verify the written data, the contents of the memory are questionable.

In many applications, data integrity is paramount. Therefore, the SRAM Stik provides battery redundancy. The DS2217 has an internal isolation switch that provides for the connection of two batteries. During battery backup time, the battery with the highest voltage is selected for use. If one battery fails, the other automatically takes over. The switch between batteries is transparent to the user. A battery status warning will occur only if both batteries are less than 2.0 volts.

IMAGE UNAVAILABLE

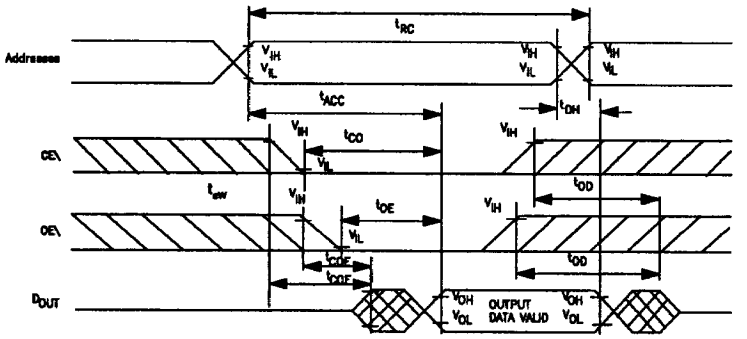
AC ELECTRICAL CHARACTERISTICS (0°C to +70°C, V_{CC}=5.0V ± 10%)

		DS2217-120		DS2217-150		DS2217-200			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read Cycle Time	t_{RC}	120		150		200		ns	
Access Time	t_{ACC}		120		150		200	ns	
CE\ to Output Valid	t_{OE}		60		70		100	ns	
OE\ to Output Valid	t_{CO}		120		150		200	ns	
OE\ or CE\ to Output Active	t_{COE}	5		5		5		ns	5
Output High Z from Deselection	t_{OD}		40		70		100	ns	
Output Hold from Address Change	t_{OH}	5		5		5		ns	5
Write Cycle Time	t_{WC}	120		150		200		ns	
Write Pulse Width	t_{WP}	90		100		150		ns	3
Address Setup Time	t_{aW}	0		0		0		ns	
Write Recovery Time	t_{WR}	20		20		20		ns	
Output High Z from WE\	t_{ODW}		40		70		80	ns	5
Output Active from WE\	t_{OEW}	5		5		5		ns	5
Data Setup Time	t_{DS}	50		60		80		ns	4
Data Hold Time	t_{DH}	20		20		20		ns	4

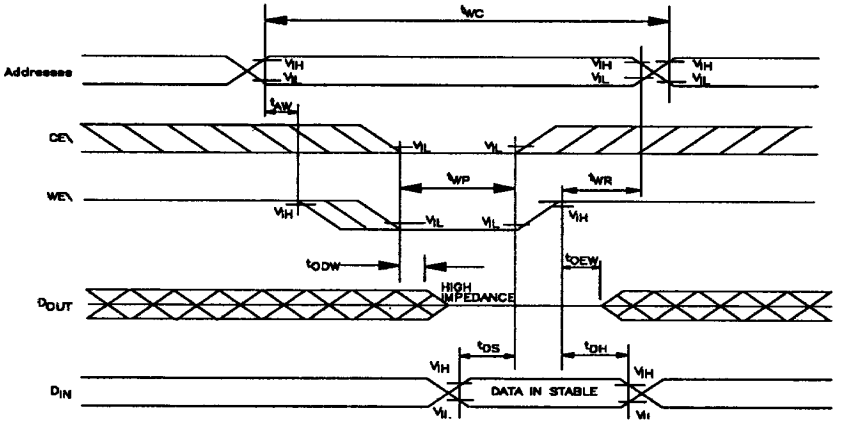
AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0-3.0 V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

READ CYCLE(1)



WRITE CYCLE 1(2),(6),(7)



WRITE CYCLE 2(2),(8)

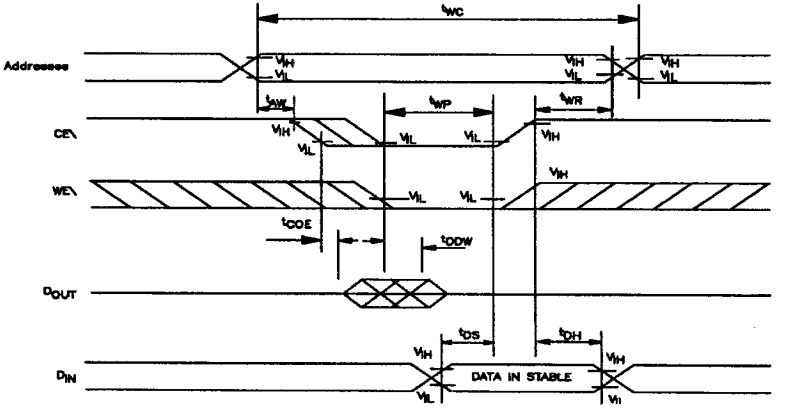


IMAGE UNAVAILABLE

NOTES:

1. WE\ is high for a read cycle.
2. OE\ = V_{IH} or V_{IL}. If OE\ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of CE\ and WE\. t_{WP} is measured from the latter of CE\ or WE\ going low to the earlier of CE\ or WE\ going high.
4. t_{DH}, t_{DS} are measured from the earlier of CE\ or WE\ going high.
5. These parameters are sampled with a 5pF load and are not 100% tested.
6. If the CE\ low transition occurs simultaneously with or later than the WE\ low transition in a Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the CE\ high transition occurs prior to or simultaneously with the WE\ high transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
8. If the WE\ is low or the WE\ low transition occurs prior to or simultaneously with the CE\ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS2217 is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.