PRODUCT SUMMARY

CX805-30 Baseband Processor for Multiband GSM and GPRS Applications

Applications

- GSM handsets and modules (850/900/1800/1900 MHz)
- GPRS handsets and modules (850/900/1800/1900 MHz)
- Bluetooth®-enabled wireless headset modules

Features

- 0.25µ CMOS process technology
- ARM7 TDMI core
- Skyworks DSP core with all memory on-chip
- GPRS class 10 and circuit-switched data (14.4 kbps) services
- Half-rate, full-rate, and enhanced full-rate speech coders
- Voice features such as voice recognition, conversation record, and voice memo
- Hardware accelerator for GPRS encryption algorithms (GEA 1 and 2)
- Integrated Real-Time Clock (RTC)
- Interface to handset MMI peripherals such as keypad, liquid crystal display (LCD), and annunciator
- Interfaces to Skyworks IA and PMIC devices
- Interface to Subscriber Identity Module (SIM)
- Addresses up to 16 MB of external memory (flash or SRAM)
- Application Interfaces:
  - Serial/RS-232
  - Infra-red Data Adapter (IrDA)
- Low power operation. 3 V I/Os and an on-chip supplied 2.5 V core
- Eight Chip Select (CS) signals for external memory
- 16-bit data bus, 24-bit address bus

NEW

Skyworks offers this part as a lead (Pb)-free "environmentally friendly" package that is RoHS compliant (European Parliament for the Restriction of Hazardous Substances).

Description

The Skyworks CX805-30 Baseband Processors (BPs) are highly integrated, dual core processors optimized for use in Global System for Mobile communications (GSM) and General Packet Radio Service (GPRS) cellular handset applications. The CX805-30 is the baseband portion of the Skyworks GSM/GPRS System Solution.

Both the Digital Signal Processor (DSP) core and the ARM7 THUMB™ Reduced Instruction Set Computing (RISC) architecture are well suited to meet the needs of low power, high performance embedded systems such as cellular phones. The BP operates over a range of 2.7 V to 3.3 V.

The baseband processing tasks are divided between the DSP and ARM7 processor cores. The DSP core executes the physical layer (layer 1) processing functions, and the ARM microcontroller core executes the Layer 2 and Layer 3 protocol software and Man-Machine Interface (MMI) functions. The two cores communicate through a dedicated block of dual port memory. Each of the functional blocks in the device can be individually powered down to ensure minimum current consumption in the idle or standby mode.

The CX805-30 family of devices is available in several package options:

- 12 x 12 mm, 0.8 mm pitch, 160-pin FPBGA
  - CX80501-31: supports up to Class 8 GPRS operation
  - CX80502-33/-35: supports up to Class 10 GPRS operation
- 10 x 10 mm, 0.5 mm pitch, 180-pin FPBGA
  - CX80501-32: supports up to Class 8 GPRS operation
  - CX80502-34/-36: supports up to Class 10 GPRS operation
  - CX80503-34: supports up to Class 10 GPRS operation and features optimized ROM code
- Lead-free 10 x 10 mm, 0.5 mm pitch, 180-pin FPBGA
  - CX80502-38: supports up to Class 10 GPRS operation
  - CX80503-38: supports up to Class 10 GPRS operation and features optimized ROM code

Figure 1 provides a block diagram of the CX805-30 device in a typical application. Package dimensions are provided in Figure 2 for the 12 x 12 devices and Figure 3 for the 10 x 10 devices.

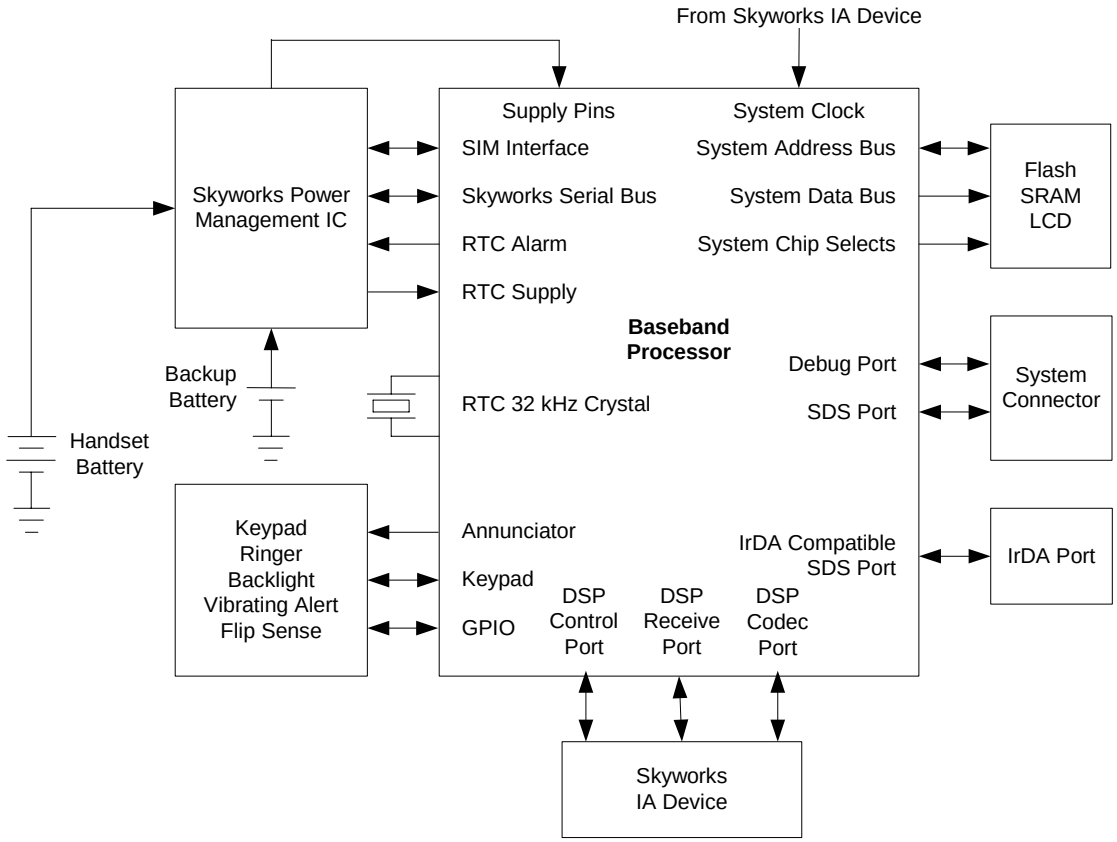
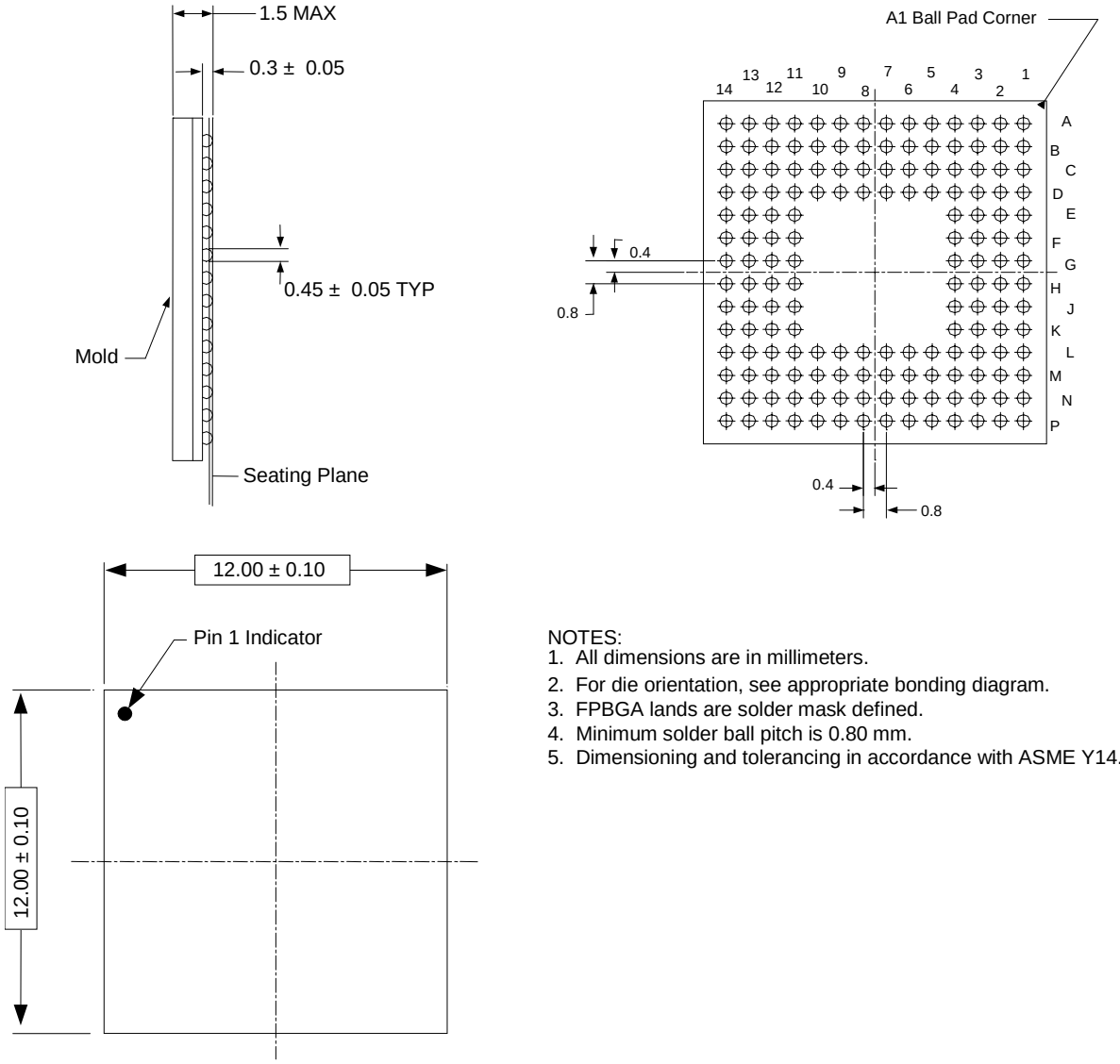


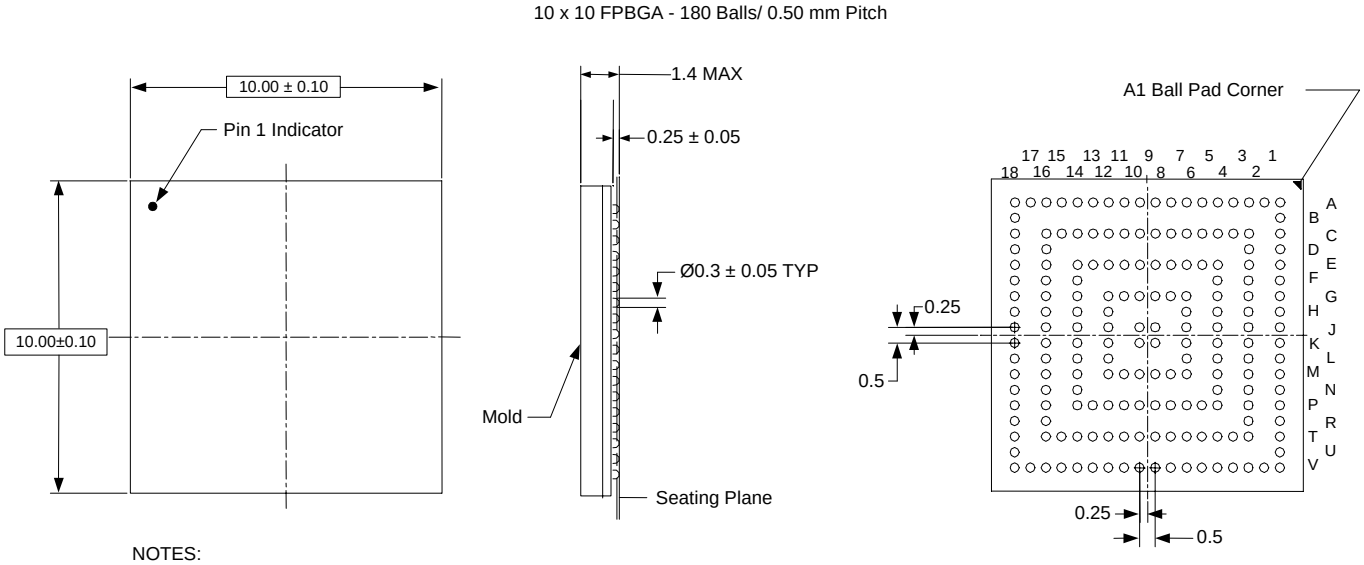
Figure 1. Block Diagram of the CX805-30 in a Typical Application

12 x 12 FPBGA - 160 Balls/ 0.80 mm Ball Pitch



NOTES:
1. All dimensions are in millimeters.
2. For die orientation, see appropriate bonding diagram.
3. FPBGA lands are solder mask defined.
4. Minimum solder ball pitch is 0.80 mm.
5. Dimensioning and tolerancing in accordance with ASME Y14.5M-1994

Figure 2. 160-pin FPBGA Package Dimensions



NOTES:
1. All dimensions are in millimeter
2. For die orientation see appropriate bonding diagram
3. FPBGA Lands are solder mask defined
4. Minimum solder pitch is 0.50 mm
5. Dimensioning and tolerancing in accordance with ASME Y14.5 M - 1994

Figure 3. 180-pin FPBGA and Lead-free 180-pin Lead-free FPBGA Package Dimensions