NEC

MOS INTEGRATED CIRCUIT

μPD43256B-X

256K-BIT CMOS STATIC RAM
32K-WORD BY 8-BIT
EXTENDED TEMPERATURE OPERATION

Description

The μPD43256B-X is a high speed, low power, and 262,144 bits (32,768 words by 8 bits) CMOS static RAM.

The μPD43256B-X is an extended-operating-temperature version of the μPD43256B (X version : T_A = –25 to +85 °C). And A and B versions are low voltage operations. Battery backup is available.

The μPD43256B-X is packed in 28-pin plastic TSOP (I) (8 x 13.4 mm).

Features

- 32,768 words by 8 bits organization
- Fast access time: 70, 85, 100, 120, 150 ns (MAX.)
- Operating ambient temperature: T_A = –25 to +85 °C
- Low voltage operation (A version: V_{CC} = 3.0 to 5.5 V, B version: V_{CC} = 2.7 to 5.5 V)
- Low V_{CC} data retention: 2.0 V (MIN.)
- /OE input for easy application

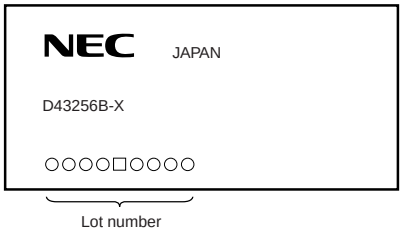
	Part number	Access time ns (MAX.)	Operating supply voltage V	Operating ambient temperature °C	Supply current		
					At operating mA (MAX.)	At standby μA (MAX.)	At data retention μA (MAX.) Note1
★	μPD43256B-xxX	70, 85	4.5 to 5.5	–25 to +85	45	50	2
	μPD43256B-AxxX	85 Note2, 100, 120 Note2	3.0 to 5.5				
	μPD43256B-BxxX Note2	100, 120 Note2, 150 Note2	2.7 to 5.5		40		

Notes 1. $T_A \leq 40$ °C, V_{CC} = 3.0 V

2. 100 s (MAX.) (V_{CC} = 4.5 to 5.5 V)

Version X

This Data sheet can be applied to the version X. Each version is identified with its lot number. Letter X in the fifth character position in a lot number signifies version X.



The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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The mark ★ shows major revised points.

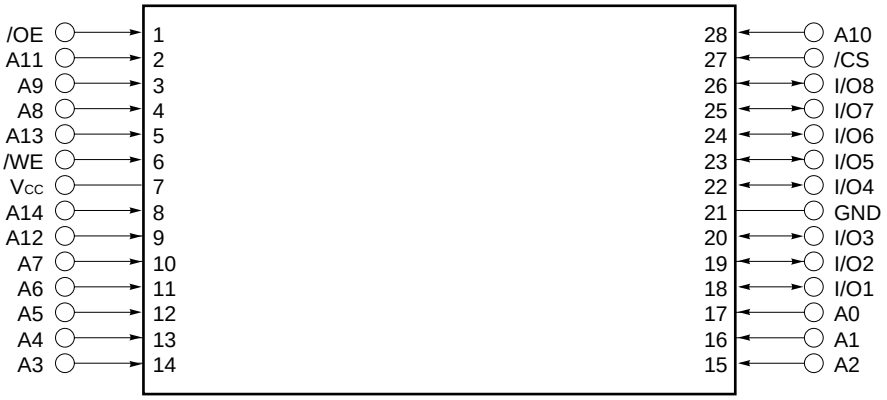
★ Ordering Information

Part number	Package	Access time ns (MAX.)	Operating supply voltage V	Operating ambient temperature °C	Remark
μPD43256BGW-70X-9JL	28-PIN PLASTIC TSOP(I)	70	4.5 to 5.5	–25 to +85	
μPD43256BGW-85X-9JL	(8x13.4) (Normal bent)	85			
μPD43256BGW-A85X-9JL		85	3.0 to 5.5		A version
μPD43256BGW-A10X-9JL		100			
μPD43256BGW-A12X-9JL		120			
μPD43256BGW-B10X-9JL		100	2.7 to 5.5		B version
μPD43256BGW-B12X-9JL		120			
μPD43256BGW-B15X-9JL		150			
μPD43256BGW-70X-9KL	28-PIN PLASTIC TSOP(I)	70	4.5 to 5.5		
μPD43256BGW-85X-9KL	(8x13.4) (Reverse bent)	85			
μPD43256BGW-A85X-9KL		85	3.0 to 5.5		A version
μPD43256BGW-A10X-9KL		100			
μPD43256BGW-A12X-9KL		120			
μPD43256BGW-B10X-9KL		100	2.7 to 5.5		B version
μPD43256BGW-B12X-9KL		120			
μPD43256BGW-B15X-9KL		150			

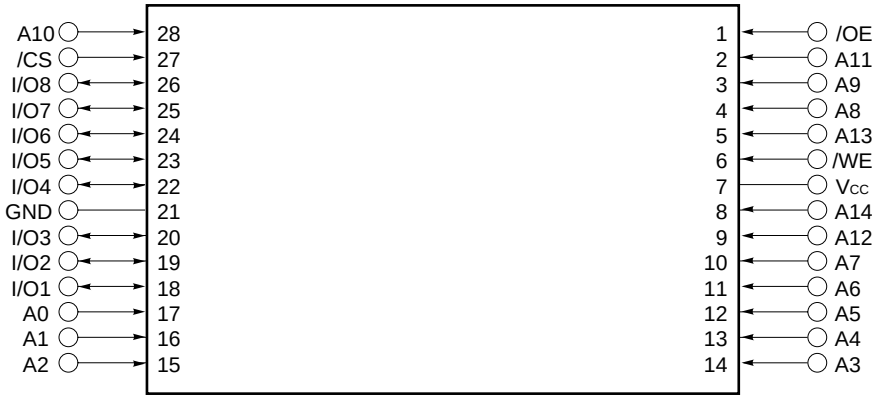
★ Pin Configurations (Marking Side)

/xxx indicates active low signal.

28-PIN PLASTIC TSOP(I) (8x13.4) (Normal bent)
[μPD43256BGW-xxX-9JL]
[μPD43256BGW-AxxX-9JL]
[μPD43256BGW-BxxX-9JL]



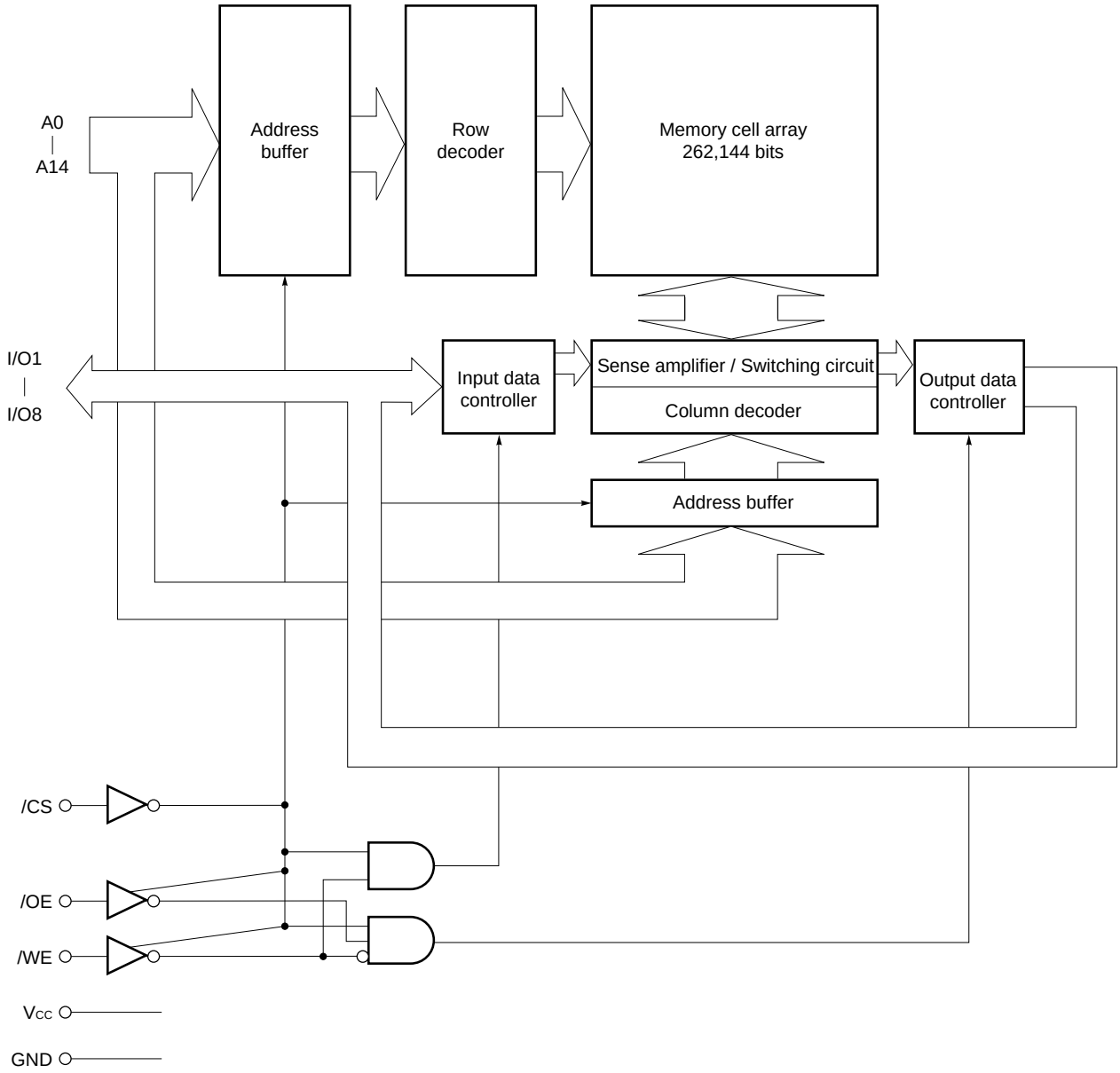
28-PIN PLASTIC TSOP(I) (8x13.4) (Reverse bent)
[μPD43256BGW-xxX-9KL]
[μPD43256BGW-AxxX-9KL]
[μPD43256BGW-BxxX-9KL]



A0 - A14	:	Address inputs
I/O1 - I/O8	:	Data inputs / outputs
/CS	:	Chip Select
/WE	:	Write Enable
/OE	:	Output Enable
Vcc	:	Power supply
GND	:	Ground

Remark Refer to **Package Drawings** for the 1-pin index mark.

Block Diagram



Truth Table

/CS	/OE	/WE	Mode	I/O	Supply current
H	×	×	Not selected	High impedance	I_{SB}
L	H	H	Output disable		I_{CCA}
L	×	L	Write	D_{IN}	
L	L	H	Read	D_{OUT}	

Remark × : V_{IH} or V_{IL}

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		–0.5 Note to +7.0	V
Input / Output voltage	V_T		–0.5 Note to V_{CC} + 0.5	V
Operating ambient temperature	T_A		–25 to +85	°C
Storage temperature	T_{stg}		–55 to +125	°C

Note –3.0 V (MIN.) (Pulse width : 50 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	μPD43256B-xxX		μPD43256B-AxxX		μPD43256B-BxxX		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Supply voltage	V_{CC}		4.5	5.5	3.0	5.5	2.7	5.5	V
High level input voltage	V_{IH}		2.4	V_{CC}+0.5	2.4	V_{CC}+0.5	2.4	V_{CC}+0.5	V
Low level input voltage	V_{IL}		–0.3 Note	+0.6	–0.3 Note	+0.4	–0.3 Note	+0.4	V
Operating ambient temperature	T_A		–25	+85	–25	+85	–25	+85	°C

Note –3.0 V (MIN.) (Pulse width: 50 ns)

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			5	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			8	pF

Remarks 1. V_{IN} : Input voltage

$V_{I/O}$: Input / Output voltage

2. These parameters are periodically sampled and not 100% tested.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted) (1/2)

	Parameter	Symbol	Test condition	μPD43256B-xxX			Unit
				MIN.	TYP.	MAX.	
	Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}	–1.0		+1.0	μA
	I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, /OE = V_{IH} or /CS = V_{IH} or /WE = V_{IL}	–1.0		+1.0	μA
★	Operating supply current	I_{CCA1}	/CS = V_{IL}, Minimum cycle time, $I_{I/O}$ = 0 mA			45	mA
		I_{CCA2}	/CS = V_{IL}, $I_{I/O}$ = 0 mA			15	
		I_{CCA3}	/CS ≤ 0.2 V, Cycle = 1 MHz, $I_{I/O}$ = 0 mA, V_{IL} ≤ 0.2 V, V_{IH} ≥ V_{CC} – 0.2 V			15	
	Standby supply current	I_{SB}	/CS = V_{IH}			3	mA
		I_{SB1}	/CS ≥ V_{CC} – 0.2 V		1.0	50	μA
	High level output voltage	V_{OH1}	I_{OH} = –1.0 mA	2.4			V
		V_{OH2}	I_{OH} = –0.1 mA	V_{CC}–0.5			
	Low level output voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V

Remarks 1. V_{IN} : Input voltage

$V_{I/O}$: Input / Output voltage

2. These DC characteristics are in common regardless of package types.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted) (2/2)

Parameter	Symbol	Test condition		μPD43256B-AxxX			μPD43256B-BxxX			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}		–1.0		+1.0	–1.0		+1.0	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, /OE = V_{IH} or /CS = V_{IH} or /WE = V_{IL}		–1.0		+1.0	–1.0		+1.0	μA
Operating supply current	I_{CCA1}	/CS = V_{IL}, Minimum cycle time, $I_{I/O}$ = 0 mA	μPD43256B-A85X			45			–	mA
			μPD43256B-A10X			40			–	
			μPD43256B-A12X			40			–	
			μPD43256B-B10X			–			40	
			μPD43256B-B12X			–			40	
			μPD43256B-B15X			–			40	
			V_{CC} ≤ 3.3 V			–			25	
	I_{CCA2}	/CS = V_{IL}, $I_{I/O}$ = 0 mA				15			15	
			V_{CC} ≤ 3.3 V			–			10	
	I_{CCA3}	/CS ≤ 0.2 V, Cycle = 1 MHz, $I_{I/O}$ = 0 mA,				15			15	
		V_{IL} ≤ 0.2 V, V_{IH} ≥ V_{CC} – 0.2 V	V_{CC} ≤ 3.3 V			–			10	
Standby supply current	I_{SB}	/CS = V_{IH}				3			3	mA
			V_{CC} ≤ 3.3 V			–			2	
	I_{SB1}	/CS ≥ V_{CC} – 0.2 V			1.0	50		1.0	50	μA
			V_{CC} ≤ 3.3 V			–			25	
High level output voltage	V_{OH1}	I_{OH} = –1.0 mA, V_{CC} ≥ 4.5 V		2.4			2.4			V
		I_{OH} = –0.5 mA, V_{CC} < 4.5 V		2.4			2.4			
	V_{OH2}	I_{OH} = –0.02 mA		V_{CC}– 0.1			V_{CC}– 0.1			
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA, V_{CC} ≥ 4.5 V				0.4			0.4	V
		I_{OL} = 1.0 mA, V_{CC} < 4.5 V				0.4			0.4	
	V_{OL1}	I_{OL} = 0.02 mA				0.1			0.1	

Remarks 1. V_{IN} : Input voltage

$V_{I/O}$: Input / Output voltage

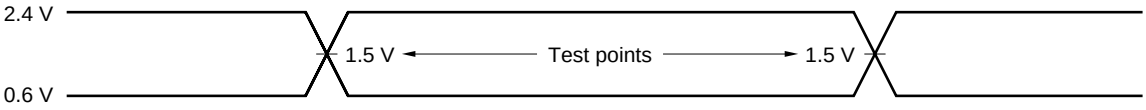
2. These DC characteristics are in common regardless of package types.

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

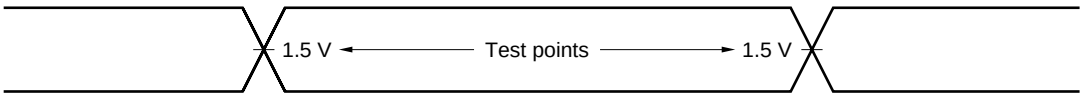
AC Test Conditions

[μPD43256B-70X, μPD43256B-85X]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



Output Load

AC characteristics should be measured with the following output load conditions.

Figure 1

(t_{AA}, t_{ACS}, t_{OE}, t_{OH})

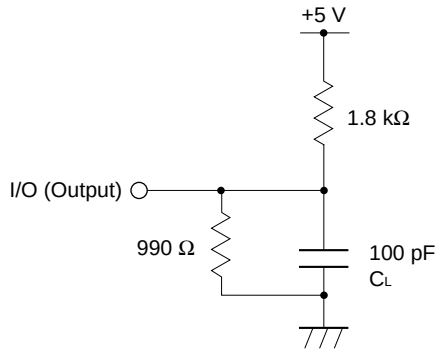
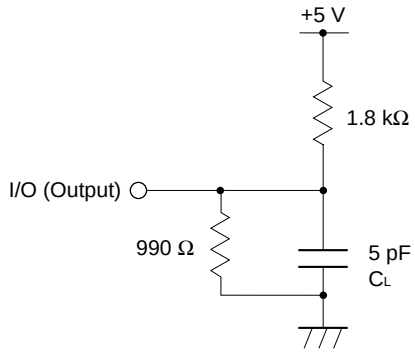


Figure 2

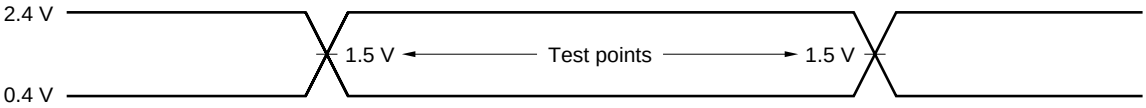
(t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ}, t_{OW})



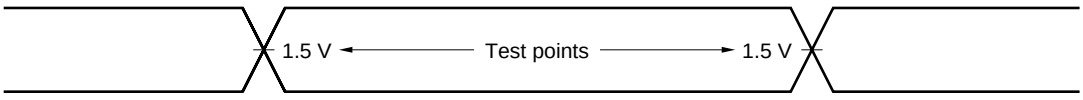
Remark C_L includes capacitance of the probe and jig, and stray capacitance.

[μPD43256B-A85X, μPD43256B-A10X, μPD43256B-A12X, μPD43256B-B10X, μPD43256B-B12X, μPD43256B-B15X]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



★ **Output Load**

AC characteristics should be measured with the following output load conditions.

t_{AA}, t_{ACS}, t_{OE}, t_{OH}	t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ}, t_{OW}
1TTL + 50 pF	1TTL + 5 pF

Read Cycle (1/2)

★

Parameter	Symbol	$V_{CC} \geq 4.5$ V						Unit	Condition
		μPD43256B-70X		μPD43256B-85X		μPD43256B-AxxX μPD43256B-BxxX			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	70		85		100		ns	
Address access time	t_{AA}		70		85		100	ns	**Note**
/CS access time	t_{ACS}		70		85		100	ns	
/OE access time	t_{OE}		35		40		50	ns	
Output hold from address change	t_{OH}	10		10		10		ns	
/CS to output in low impedance	t_{CLZ}	10		10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		5		ns	
/CS to output in high impedance	t_{CHZ}		30		30		35	ns	
/OE to output in high impedance	t_{OHZ}		30		30		35	ns	

Note See the **output load**.

Remark These AC characteristics are in common regardless of package types and L, LL versions.

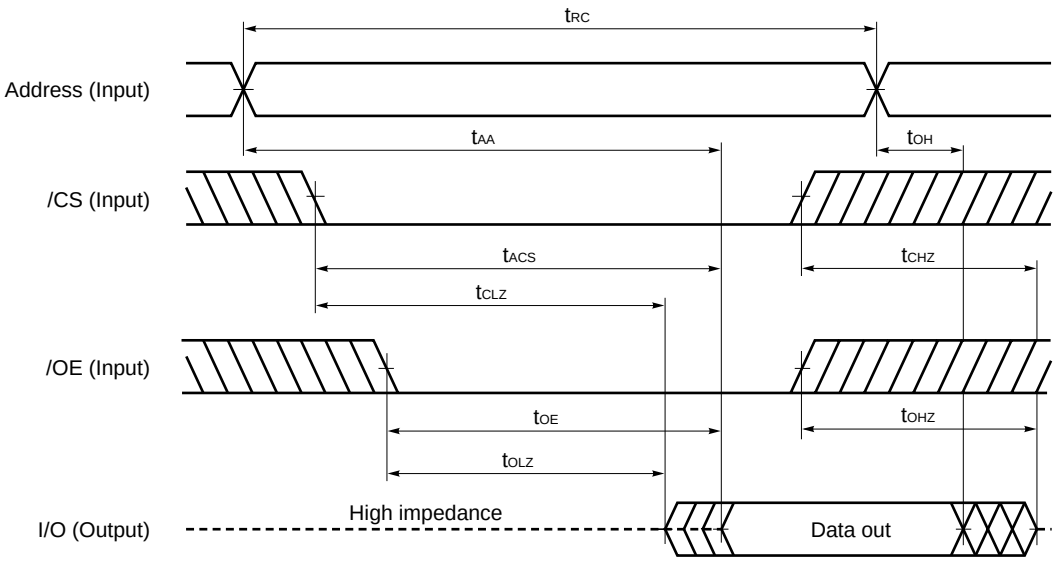
Read Cycle (2/2)

Parameter	Symbol	$V_{CC} \geq 3.0$ V						$V_{CC} \geq 2.7$ V						Unit	Condition
		μPD43256B-A85X		μPD43256B-A10X		μPD43256B-A12X		μPD43256B-B10X		μPD43256B-B12X		μPD43256B-B15X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	85		100		120		100		120		150		ns	
Address access time	t_{AA}		85		100		120		100		120		150	ns	**Note**
/CS access time	t_{ACS}		85		100		120		100		120		150	ns	
/OE access time	t_{OE}		50		60		60		60		60		70	ns	
Output hold from address change	t_{OH}	10		10		10		10		10		10		ns	
/CS to output in low impedance	t_{CLZ}	10		10		10		10		10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		5		5		5		5		ns	
/CS to output in high impedance	t_{CHZ}		35		35		40		35		40		50	ns	
/OE to output in high impedance	t_{OHZ}		35		35		40		35		40		50	ns	

Note See the **output load**.

Remark These AC characteristics are in common regardless of package types.

Read Cycle Timing Chart



Remark In read cycle, /WE should be fixed to high level.

Write Cycle (1/2)

★

Parameter	Symbol	$V_{CC} \geq 4.5$ V						Unit	Condition
		μPD43256B-70X		μPD43256B-85X		μPD43256B-AxxX μPD43256B-BxxX			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	70		85		100		ns	
/CS to end of write	t_{CW}	60		70		80		ns	
Address valid to end of write	t_{AW}	60		70		80		ns	
Write pulse width	t_{WP}	55		60		70		ns	
Data valid to end of write	t_{DW}	30		35		40		ns	
Data hold time	t_{DH}	5		5		5		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write recovery time	t_{WR}	0		0		0		ns	
/WE to output in high impedance	t_{WHZ}		30		30		35	ns	**Note**
Output active from end of write	t_{OW}	5		5		5		ns	

Note See the **output load**.

Remark These AC characteristics are in common regardless of package types and L, LL versions.

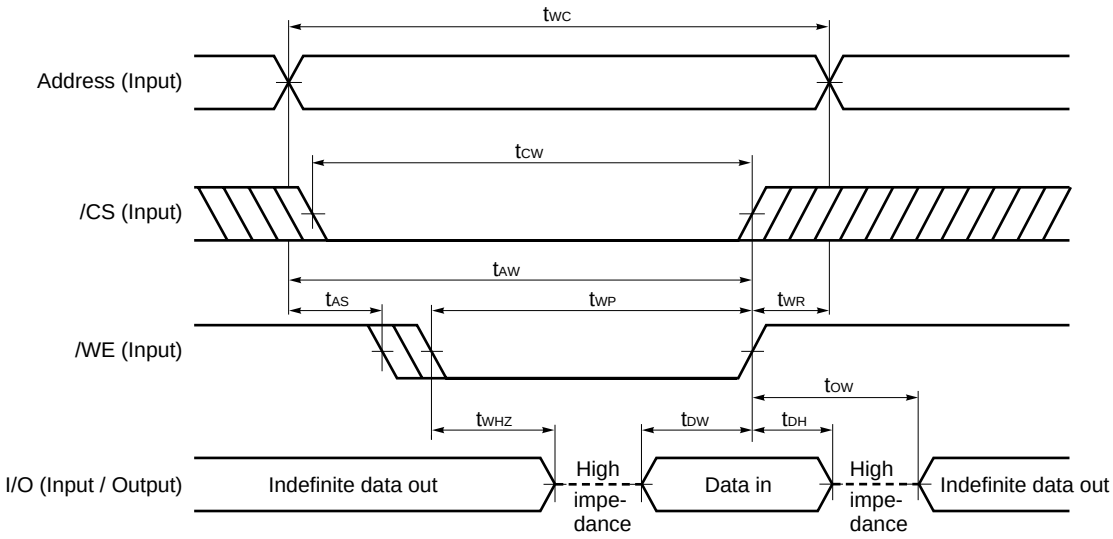
Write Cycle (2/2)

Parameter	Symbol	$V_{CC} \geq 3.0$ V						$V_{CC} \geq 2.7$ V						Unit	Condition
		μPD43256B-A85X		μPD43256B-A10X		μPD43256B-A12X		μPD43256B-B10X		μPD43256B-B12X		μPD43256B-B15X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	85		100		120		100		120		150		ns	
/CS to end of write	t_{CW}	70		70		90		70		90		100		ns	
Address valid to end of write	t_{AW}	70		70		90		70		90		100		ns	
Write pulse width	t_{WP}	60		60		80		60		80		90		ns	
Data valid to end of write	t_{DW}	60		60		70		60		70		80		ns	
Data hold time	t_{DH}	5		5		5		5		5		5		ns	
Address setup time	t_{AS}	0		0		0		0		0		0		ns	
Write recovery time	t_{WR}	0		0		0		0		0		0		ns	
/WE to output in high impedance	t_{WHZ}		35		35		40		35		40		40	ns	**Note**
Output active from end of write	t_{OW}	5		5		5		5		5		5		ns	

Note See the **output load**.

Remark These AC characteristics are in common regardless of package types.

Write Cycle Timing Chart 1 (/WE Controlled)



Cautions 1. /CS or /WE should be fixed to high level during address transition.

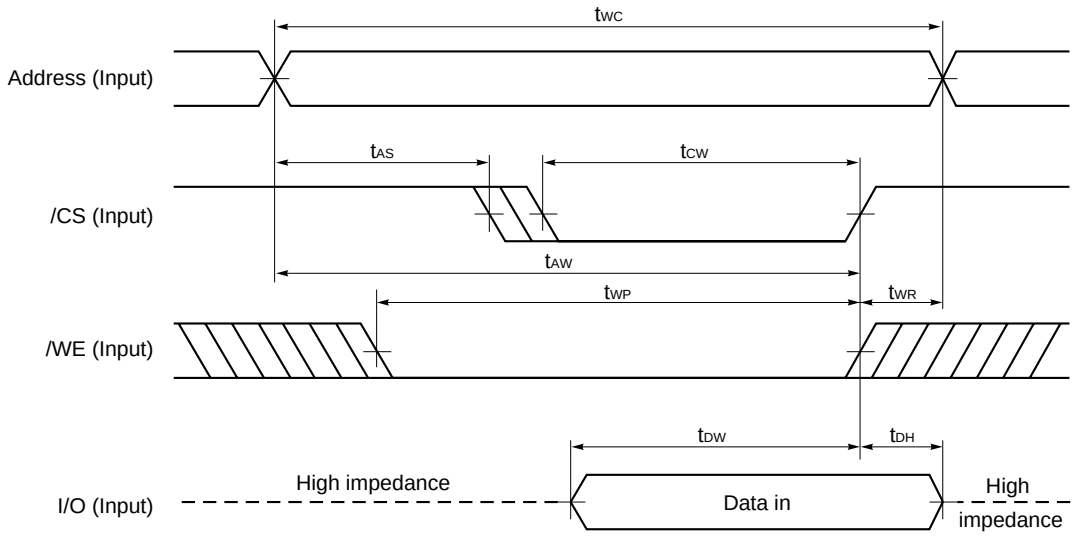
2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remarks 1. Write operation is done during the overlap time of a low level /CS and a low level /WE.

2. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

3. If /CS changes to low level at the same time or after the change of /WE to low level, the I/O pins will remain high impedance state.

Write Cycle Timing Chart 2 (/CS Controlled)



Cautions 1. /CS or /WE should be fixed to high level during address transition.

2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

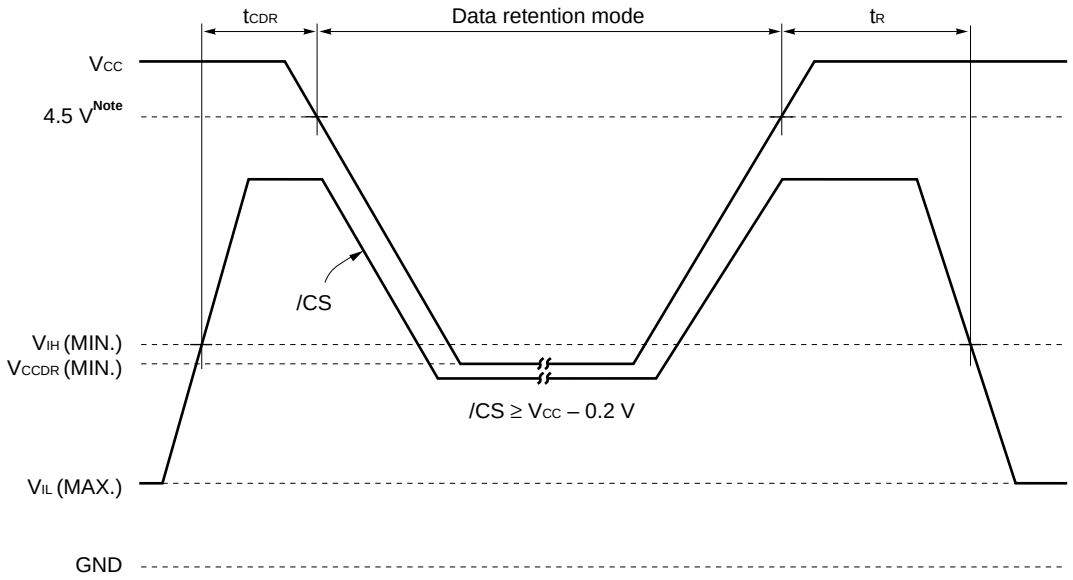
Remark Write operation is done during the overlap time of a low level /CS and a low level /WE.

Low V_{CC} Data Retention Characteristics (T_A = –25 to +85 °C)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{CCDR}	/CS ≥ V_{CC} – 0.2 V	2.0		5.5	V
Data retention supply current	I_{CCDR}	V_{CC} = 3.0 V, /CS ≥ V_{CC} – 0.2 V		0.5	20 Note	μA
Chip deselection to data retention mode	t_{CDR}		0			ns
Operation recovery time	t_R		5			ms

Note 2 μA (T_A ≤ 40 °C), 7 μA (T_A ≤ 70 °C)

Data Retention Timing Chart

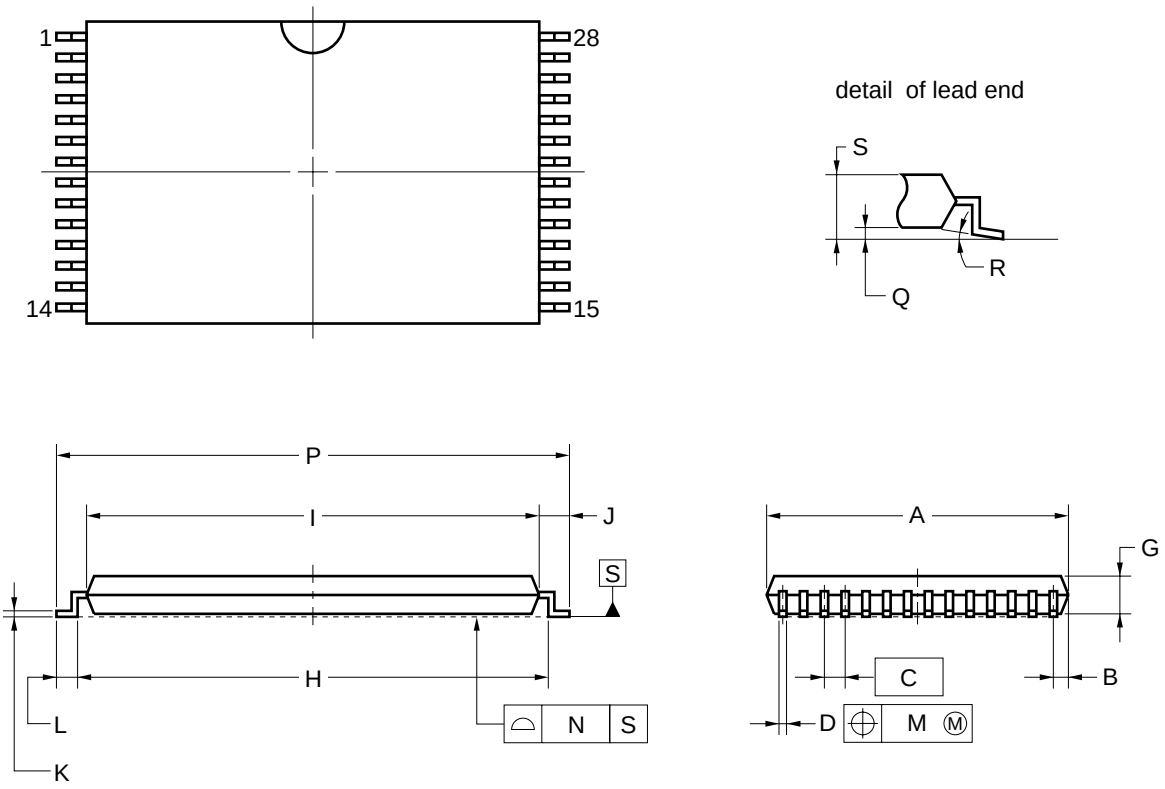


Note A version : 3.0 V, B version : 2.7 V

Remark The other pins (Address, /OE, /WE, I/O) can be in high impedance state.

★ **Package Drawings**

28-PIN PLASTIC TSOP(I) (8x13.4)



NOTES

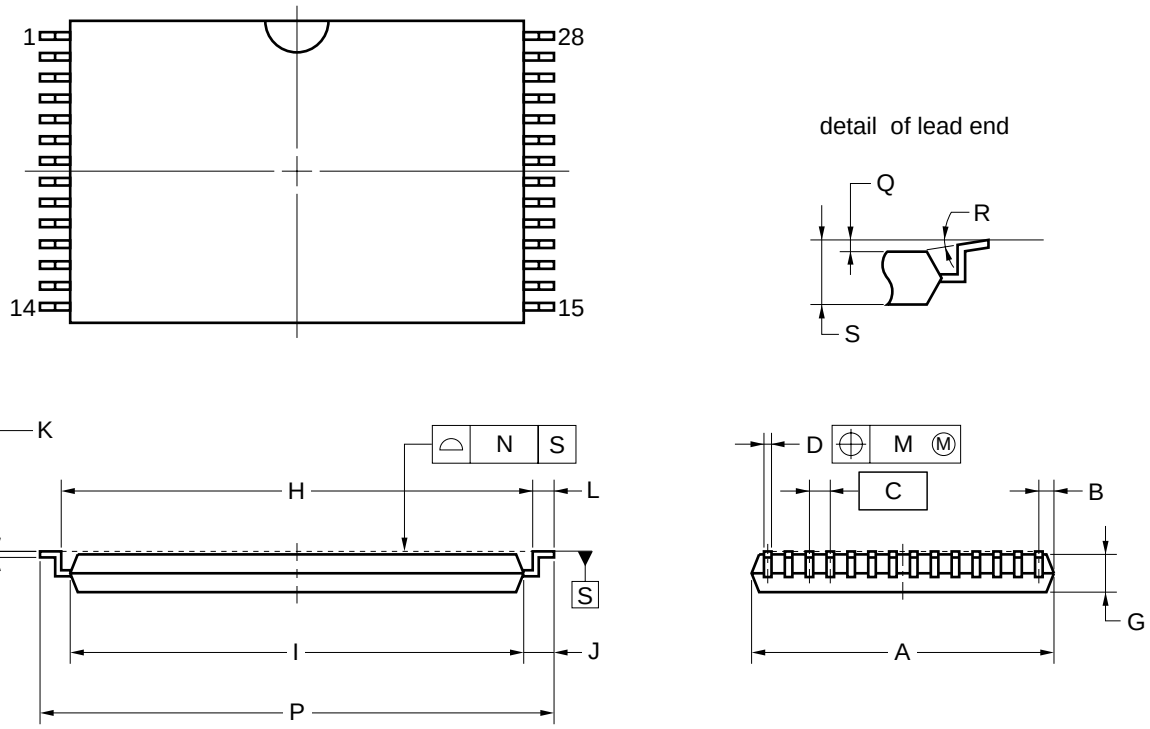
1. Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

2. "A" excludes mold flash. (Includes mold flash : 8.4mm MAX.)

ITEM	MILLIMETERS
A	8.0±0.1
B	0.6 MAX.
C	0.55 (T.P.)
D	$0.22^{+0.08}_{-0.07}$
G	1.0
H	12.4±0.2
I	11.8±0.1
J	0.8±0.2
K	$0.145^{+0.025}_{-0.015}$
L	0.5±0.1
M	0.08
N	0.10
P	13.4±0.2
Q	0.1±0.05
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.2 MAX.

P28GW-55-9JL-2

28-PIN PLASTIC TSOP(I) (8x13.4)



NOTE

1. Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 8.4mm MAX.)

ITEM	MILLIMETERS
A	8.0±0.1
B	0.6 MAX.
C	0.55 (T.P.)
D	$0.22^{+0.08}_{-0.07}$
G	1.0
H	12.4±0.2
I	11.8±0.1
J	0.8±0.2
K	$0.145^{+0.025}_{-0.015}$
L	0.5±0.1
M	0.08
N	0.10
P	13.4±0.2
Q	0.1±0.05
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.2 MAX.

P28GW-55-9KL-2

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD43256B-X.

Types of Surface Mount Device

μPD43256BGW-xxX-9JL: 28-PIN PLASTIC TSOP(I) (8x13.4) (Normal bent)

μPD43256BGW-xxX-9KL: 28-PIN PLASTIC TSOP(I) (8x13.4) (Reverse bent)

μPD43256BGW-AxxX-9JL: 28-PIN PLASTIC TSOP(I) (8x13.4) (Normal bent)

μPD43256BGW-AxxX-9KL: 28-PIN PLASTIC TSOP(I) (8x13.4) (Reverse bent)

μPD43256BGW-BxxX-9JL: 28-PIN PLASTIC TSOP(I) (8x13.4) (Normal bent)

μPD43256BGW-BxxX-9KL: 28-PIN PLASTIC TSOP(I) (8x13.4) (Reverse bent)

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.