

# 1

## PRODUCT OVERVIEW

### S3C8-SERIES MICROCONTROLLERS

Samsung's S3C8 series of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes. Important CPU features include:

- Efficient register-oriented architecture
- Selectable CPU clock sources
- Idle and Stop power-down mode release by interrupt
- Built-in basic timer with watchdog function

A sophisticated interrupt structure recognizes up to eight interrupt levels. Each level can have one or more interrupt sources and vectors. Fast interrupt processing (within a minimum six CPU clocks) can be assigned to specific interrupt levels.

### S3C8095/P8095 MICROCONTROLLER

The S3C8095/P8095 single-chip CMOS microcontroller is fabricated using a highly advanced CMOS process and is based on Samsung's newest CPU architecture.

The S3C8095 is the microcontroller which has 16-Kbytes mask-programmable ROM.

The S3P8095 is the microcontroller which has 16-Kbytes one-time-programmable EPROM.

Using a proven modular design approach, Samsung engineers developed the S3C8095/P8095 by integrating the following peripheral modules with the powerful SAM87 core:

- Four programmable I/O ports, including three 8-bit ports and one 2-bit port, for a total of 26 pins.
- Twelve bit-programmable pins for external interrupts.
- One 8-bit basic timer for oscillation stabilization and watchdog functions (system reset).

- One 8-bit timer/counter and one 16-bit timer/counter with selectable operating modes.
- One 8-bit counter with auto-reload function and one-shot or repeat control.

The S3C8095 is a versatile general-purpose microcontroller. It is currently available in a 32-pin SOP and SDIP package.



Figure 1-1. S3C8095 Microcontroller

## FEATURES

### CPU

- SAM87 CPU core

### Memory

- 16K-byte internal program memory (ROM)
- 317-byte internal register file

### Instruction Set

- 78 instructions
- IDLE and STOP instructions added for power-down modes

### Instruction Execution Time

- 750 ns at 8-MHz  $f_{OSC}$  (minimum)

### Interrupts

- Six interrupt levels and 18 interrupt sources
- 15 vectors (14 sources have a dedicated vector address and four sources share a single vector)
- Fast interrupt processing feature (for one selected interrupt level)

### I/O Ports

- Three 8-bit I/O ports (P0–P2) and one 2-bit port (P3) for a total of 26 bit-programmable pins
- Twelve input pins for external interrupts

### Timers and Timer/Counters

- One programmable 8-bit basic timer (BT) for oscillation stabilization control or watchdog timer (software reset) function
- One 8-bit timer/counter (Timer 0) with three operating modes; Interval, Capture and PWM
- One 16-bit timer/counter (Timer 1) with two operating modes; Interval and Capture

### Carrier Frequency Generator

- One 8-bit counter with auto-reload function and one-shot or repeat control (Counter A)

### Operating Temperature Range

- $-20^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

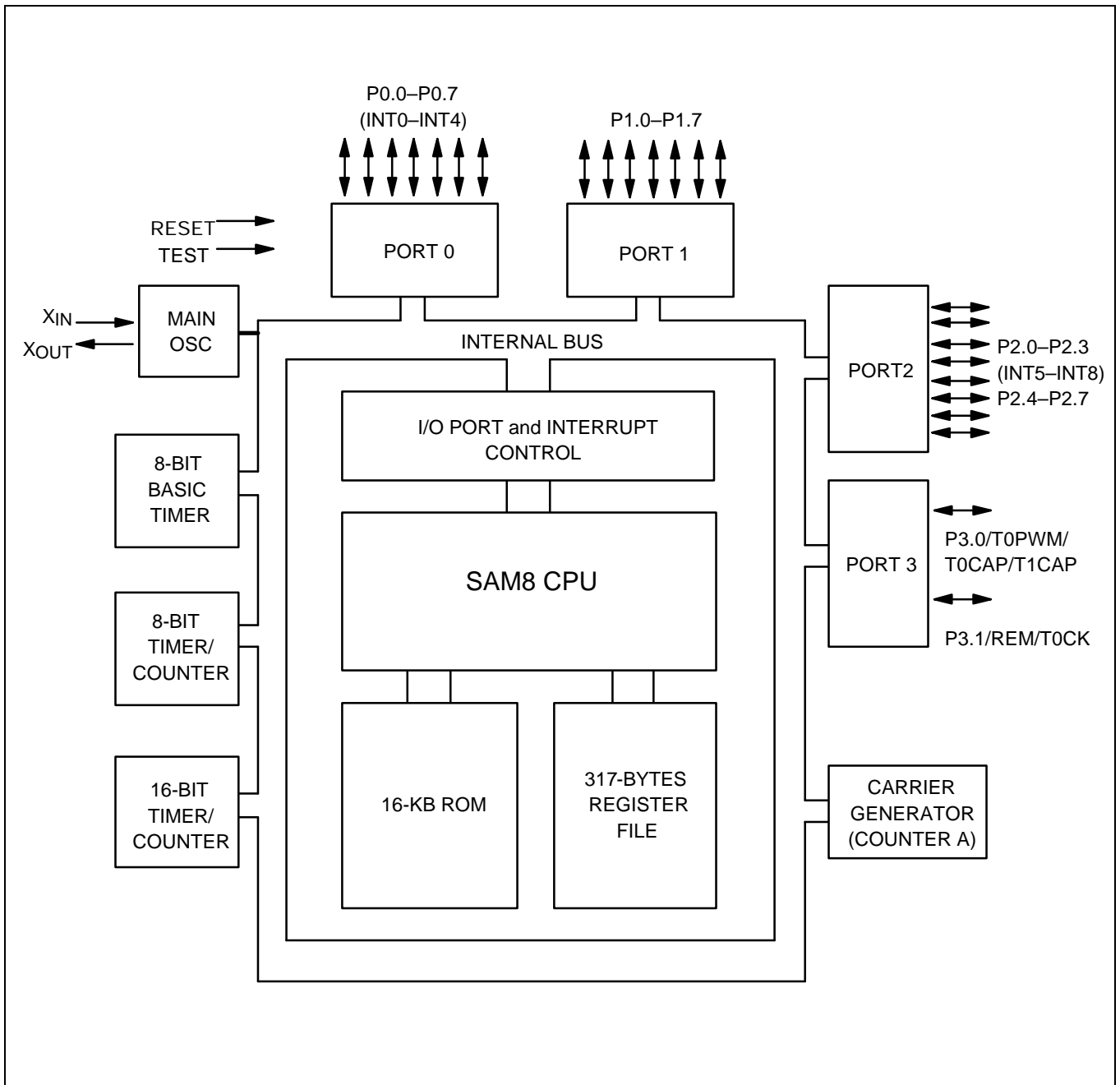
### Operating Voltage Range

- 2.0 V to 5.5 V at 4 MHz  $f_{OSC}$
- 2.4 V to 5.5 V at 8 MHz  $f_{OSC}$

### Package Type

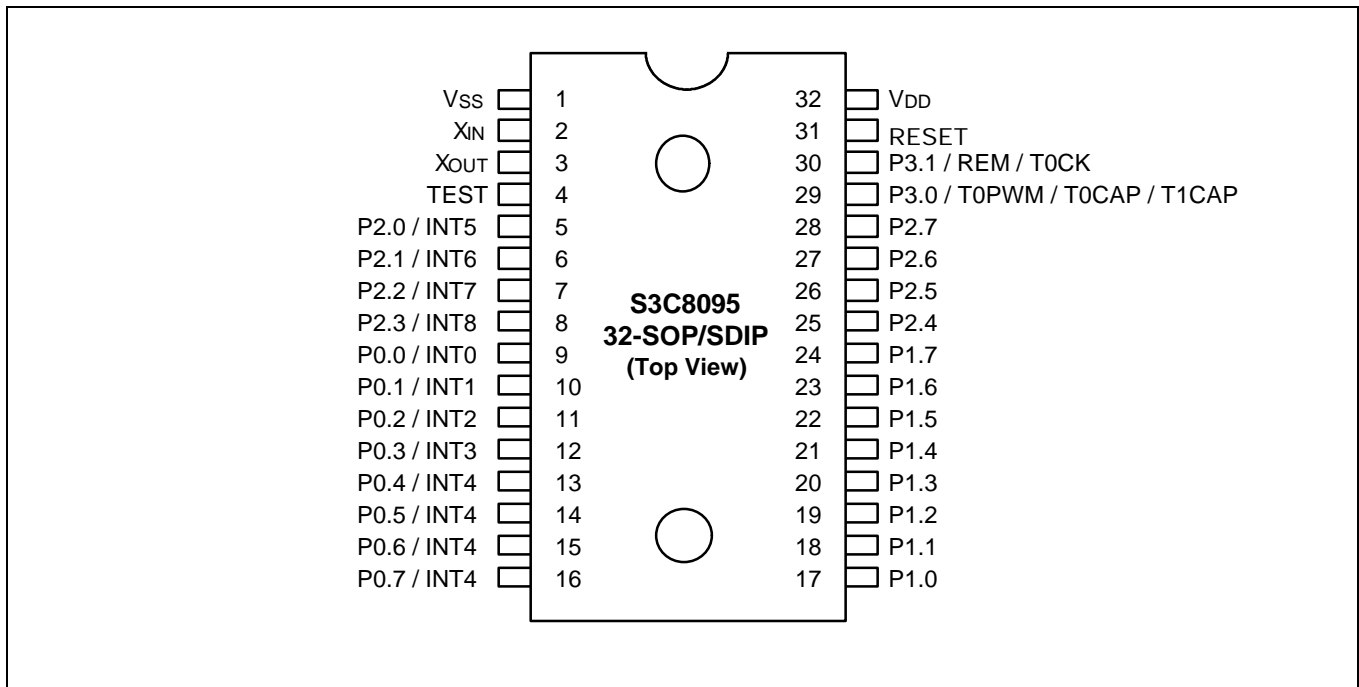
- 32-pin SOP
- 32-pin SDIP

**BLOCK DIAGRAM**



**Figure 1-2. Block Diagram**

**PIN ASSIGNMENTS**



**Figure 1-3. Pin Assignment Diagram (32-Pin SOP/SDIP Package)**

## PIN DESCRIPTIONS

Table 1-1. Pin Descriptions

Pin Names	Pin Type	Pin Description	Circuit Type	Pin No.	Shared Functions
P0.0–P0.7	I/O	I/O port with bit-programmable pins. Configurable to input or push-pull output mode. Pull-up resistors are assignable by software. Pins can be assigned individually as external interrupt inputs with noise filters, interrupt enable/ disable, and interrupt pending control.	1	9–16	INT0–INT4
P1.0–P1.7	I/O	I/O port with bit-programmable pins. Configurable to Schmitt trigger input mode or output mode. Pin circuits are either push-pull or n-channel open-drain type. Pull-up resistors are assignable by software.	3	17–24	–
P2.0–P2.3 P2.4–P2.7	I/O	General-purpose I/O port with bit-programmable pins. Configurable to Schmitt trigger input mode, push-pull output mode, or n-channel open-drain output mode. Pull-up resistors are assignable by software. Lower nibble pins, P2.3–P2.0, can be assigned as external interrupt inputs with noise filters, interrupt enable/disable, and interrupt pending control.	2 3	5–8, 25–28	INT5–INT8 –
P3.0 P3.1	I/O	2-bit I/O port with bit-programmable pins. Configurable to Schmitt trigger input mode, push-pull output mode, or n-channel open-drain output mode. Pull-up resistors are assignable by software. The two port 3 pins have high current drive capability.	4	29 30	T0PWM/ T0CAP/ T1CAP/ REM/T0CK
X <sub>IN</sub> , X <sub>OUT</sub>	–	System clock input and output pins	–	2, 3	–
RESET	I	System reset signal input pin with schmitt trigger circuit.	5	31	–
TEST	I	Test signal input pin (for factory use only; must be connected to V <sub>SS</sub> ).	–	4	–
V <sub>DD</sub>	–	Power supply input pin	–	32	–
V <sub>SS</sub>	–	Ground pin	–	1	–

PIN CIRCUITS

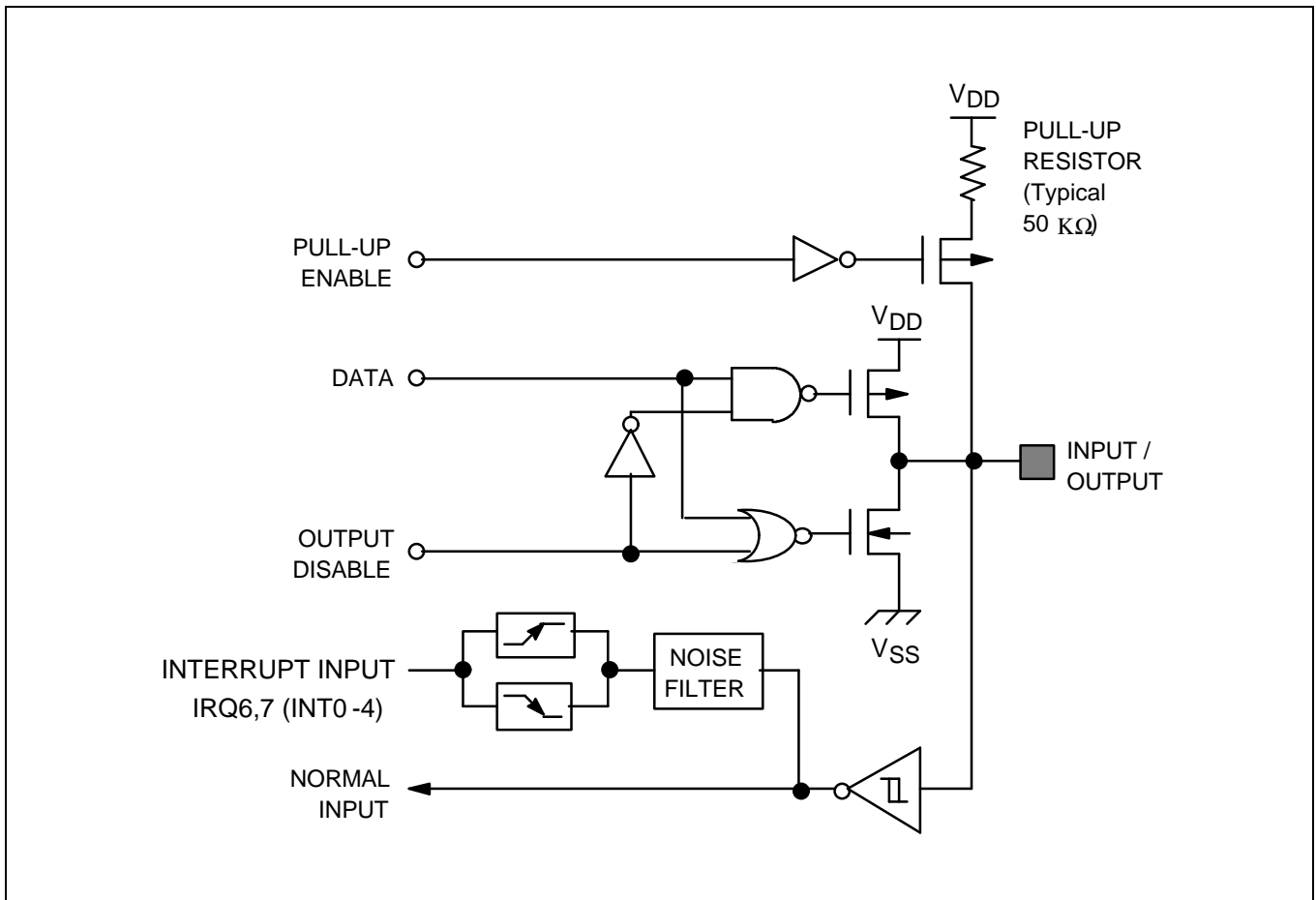


Figure 1-4. Pin Circuit Type 1 (Port 0)

PIN CIRCUITS (Cont.)

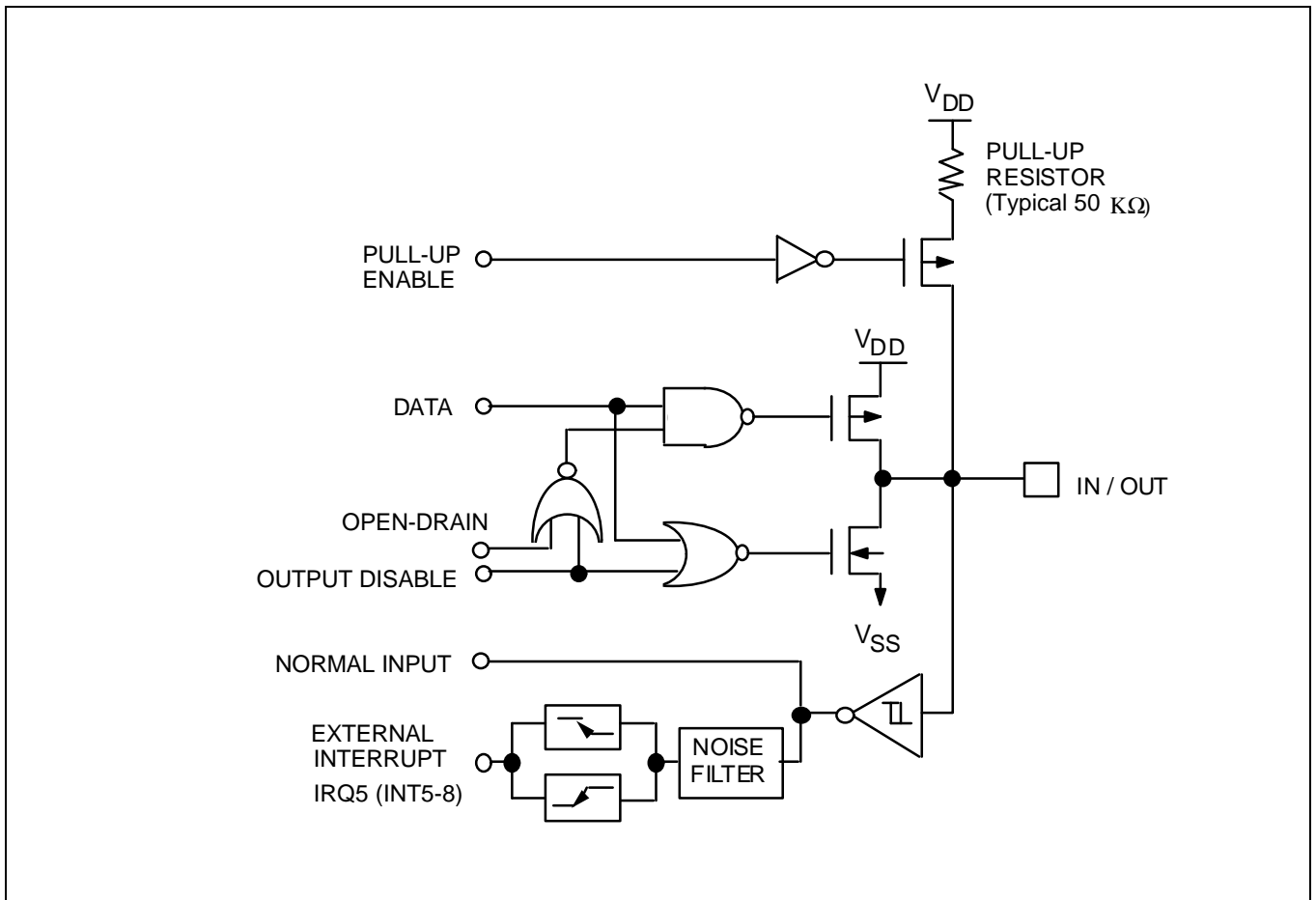


Figure 1-5. Pin Circuit Type 2 (Ports 2.0-2.3)

PIN CIRCUITS (Cont.)

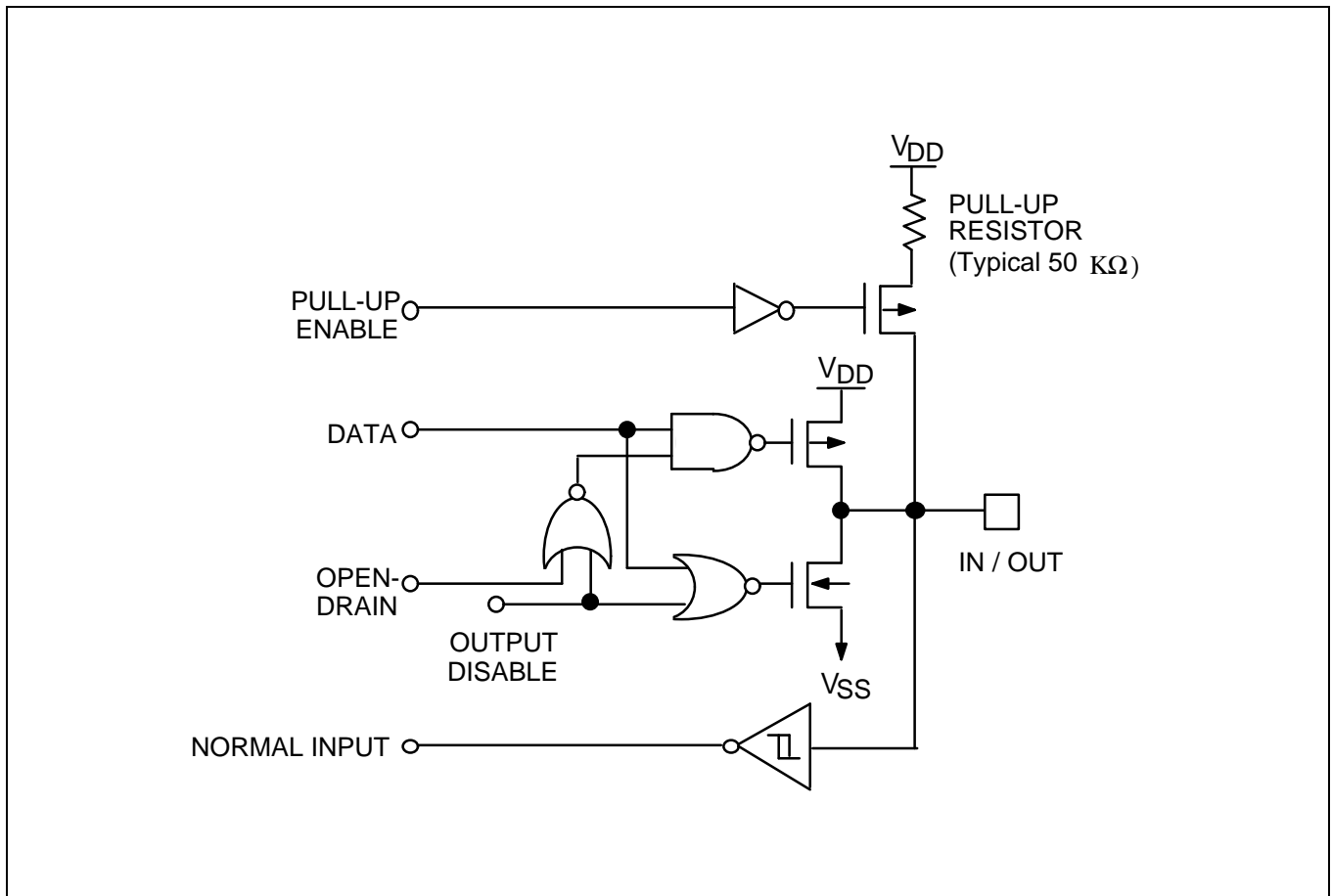


Figure 1-6. Pin Circuit Type 3 (Ports 1 and P2.4–P2.7)



PIN CIRCUITS (Cont.)

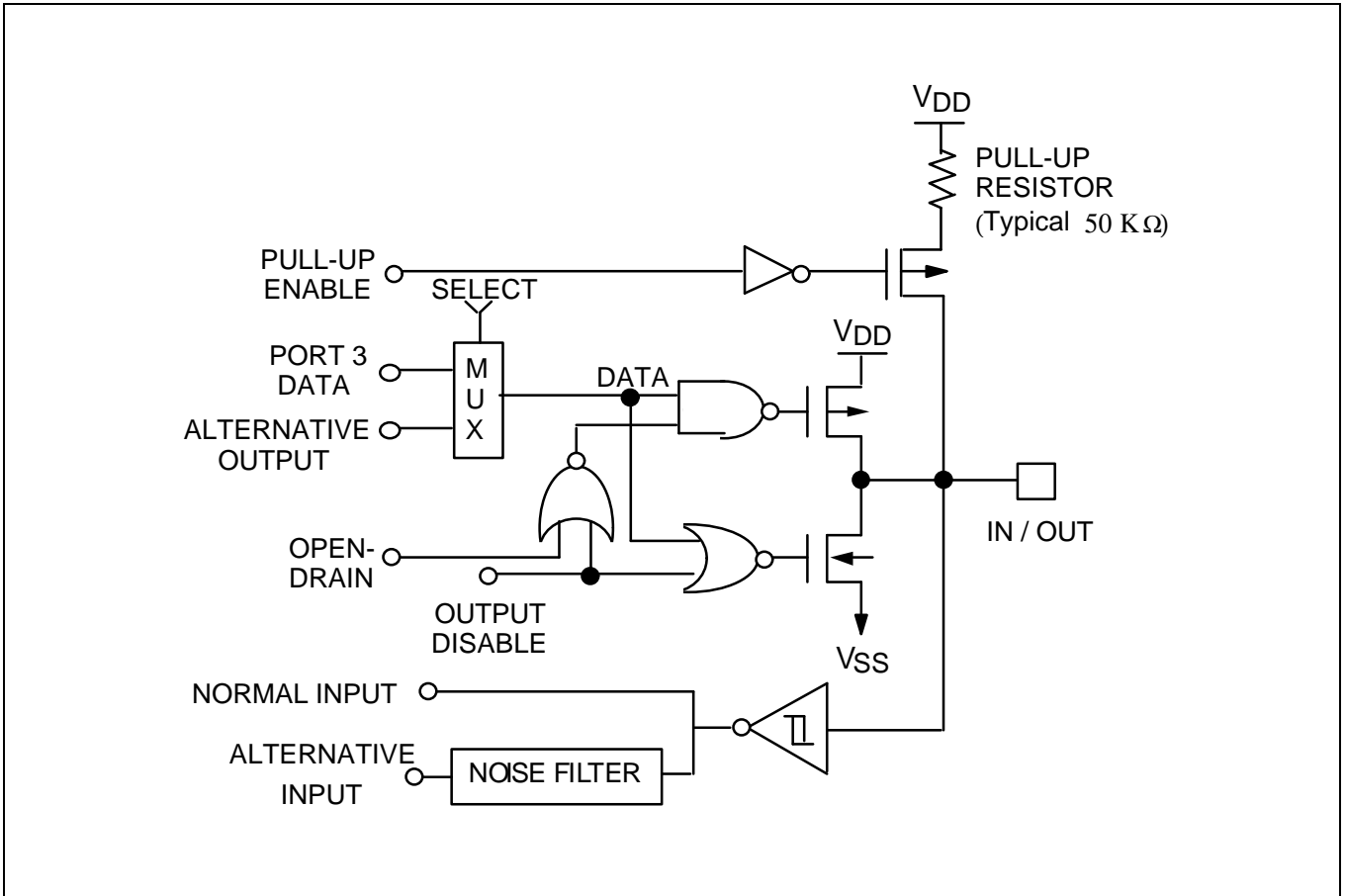


Figure 1-7. Pin Circuit Type 4 (Port 3)

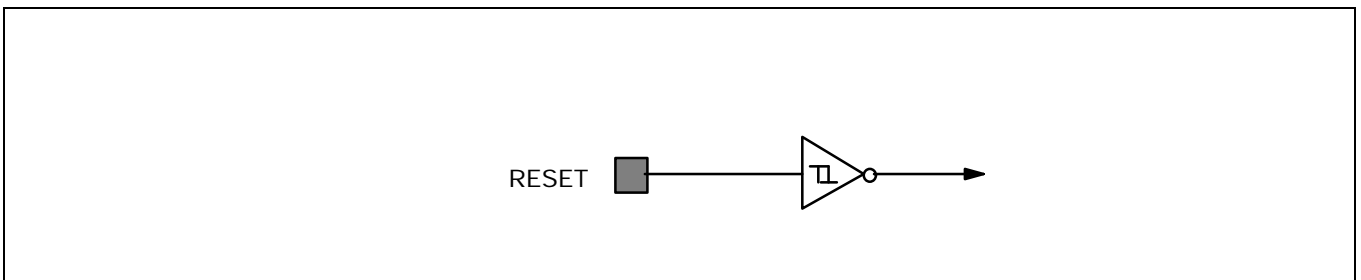


Figure 1-8. Pin Circuit Type 5 (RESET)

# 13

## S3P8095 OTP

### OVERVIEW

The S3P8095 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3C8095 microcontroller. It has an on-chip EPROM instead of masked ROM.

The S3P8095 is fully compatible with the S3C8095, both in function and in pin configuration. Because of its simple programming requirements, the S3P8095 is ideal for use as an evaluation chip for the S3C8095.

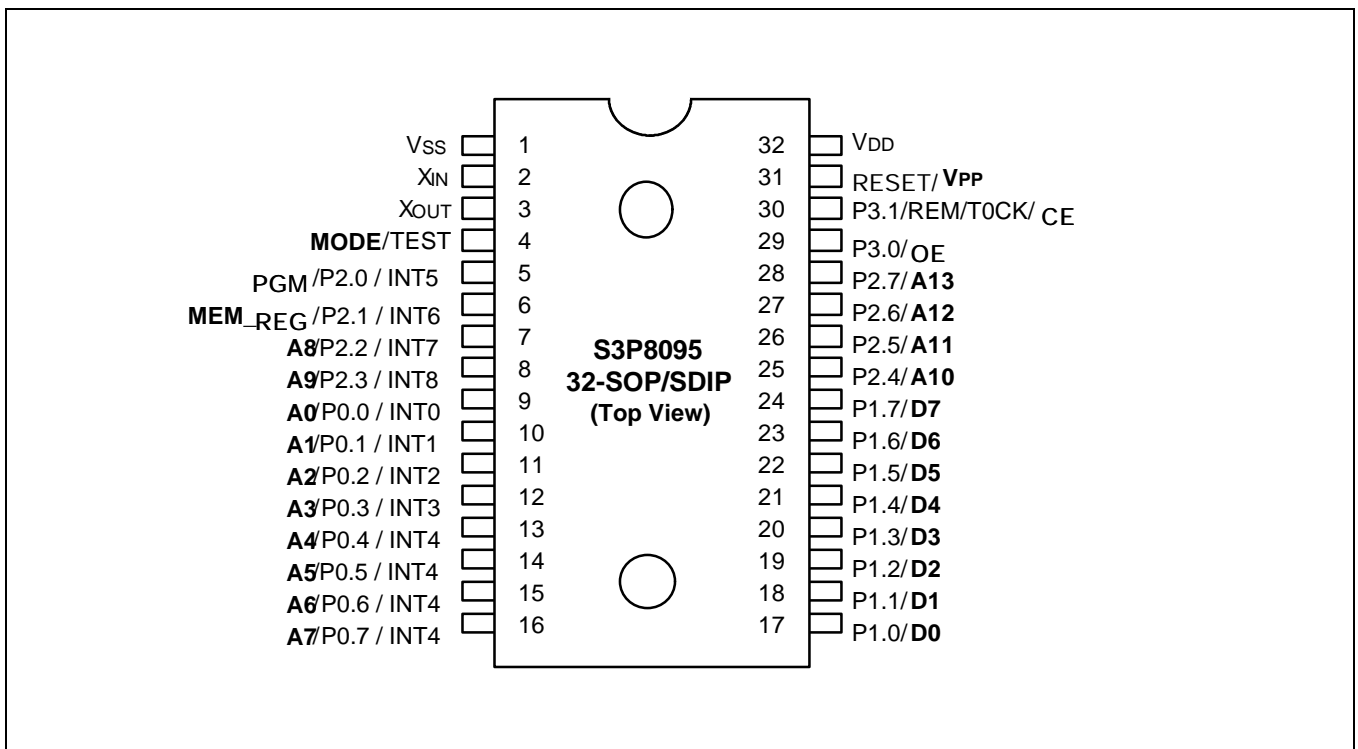


Figure 13-1. S3P8095 Pin Assignments

Table 13-1. Pin Descriptions used to read/write the EPROM

Pin Name	Pin No.	I/O	Function
A0 - A13	7 - 16, 25 - 28	O	Address lines to read/write EPROM
D0 - D7	17 - 24	I/O	8-bit data input/output lines to read/write EPROM
MODE	4	—	Select EPROM mode.
CE	30	I	Chip enable (Connect to V <sub>SS</sub> , when read/write EPROM)
OE	29	I	Output enable
PGM	5	I	EPROM Program enable
MEM_REG	6	I	Select Memory space of EPROM
V <sub>DD</sub>	32	—	Supply voltage (normally 5 V)
V <sub>PP</sub>	31	—	EPROM Program/Verify voltage (normally 12.5 V)
V <sub>SS</sub>	1	—	GROUND
X <sub>IN</sub>	2	—	System Clock input pin
X <sub>OUT</sub>	3	—	System Clock output pin

### CHARACTERISTICS OF EPROM OPERATION

When +12.5 V is supplied to V<sub>PP</sub> and MODE pins of the S3P8095, the EPROM programming mode is entered. The operating mode (read, write) is selected according to the input signals to the pins listed in Table 2 as below.

Table 13-2. Operating Mode Selection Criteria

V <sub>DD</sub>	MODE	V <sub>PP</sub>	PGM	MEM	OE	Mode
5 V	V <sub>PP</sub>	12.5 V	1	1	0	READ
			0	1	1	PROGRAM
			1	1	0	PROGRAM VERIFY

**NOTE:** "0" means Low level; "1" means High level.

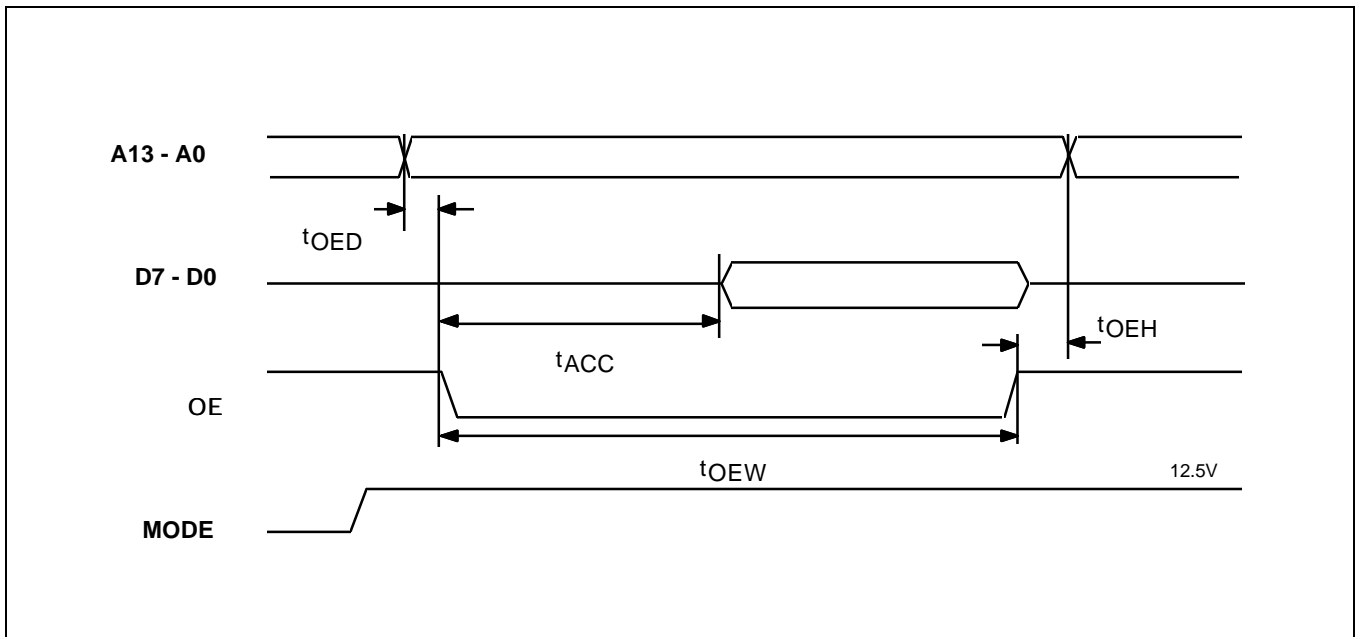


Figure 13-2. OTP Read Timing

Table 13-3. OTP Read characteristics

( $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$ ,  $V_{DD} = 5\text{V} \pm 5\%$ ,  $V_{PP} = 12.5\text{V} \pm 0.25\text{V}$ )

Parameter	Symbol	Min	Typ	Max	Units
Address to Output Delay	$t_{ACC}$	—	—	75	ns
OE to Address Delay	$t_{OED}$	0	—	—	
OE Pulse Width	$t_{OEW}$	75	—	—	
Output hold from OE whichever occurs first	$t_{OEH}$	0	—	—	

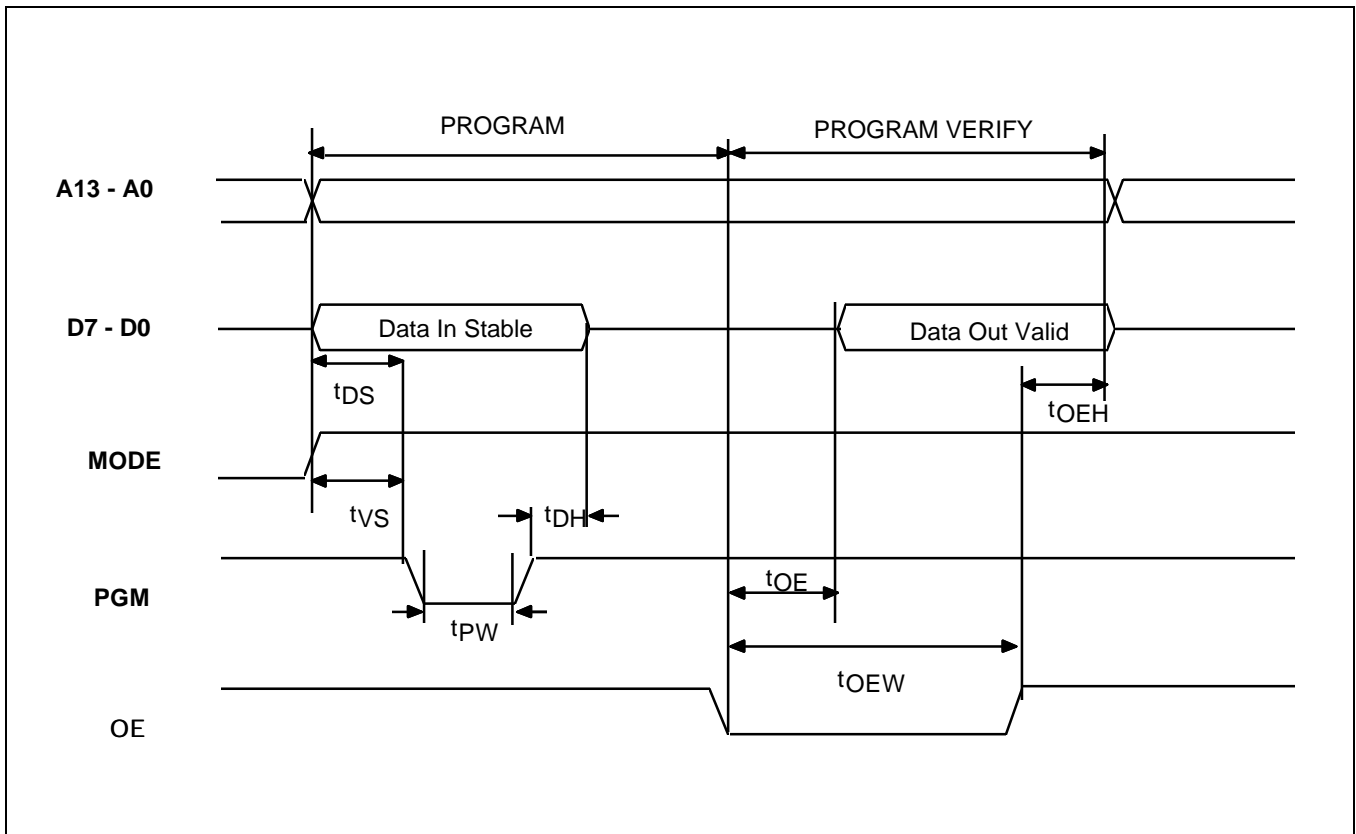


Figure 13-3. Program Memory Write Timing

Table 13-4. OTP Program/Program Verify Characteristics

( $T_A = 25\text{ }^\circ\text{C} \pm 5\text{ }^\circ\text{C}$ ,  $V_{DD} = 5\text{ V} \pm 5\%$ ,  $V_{PP} = 12.5\text{ V} \pm 0.25\text{V}$ )

Parameter	Symbol	Min	Typ	Max	Units
V <sub>PP</sub> Setup Time	$t_{VS}$	—	2	—	μs
Data Setup Time	$t_{DS}$	—	2	—	
Data Hold Time	$t_{DH}$	—	2	—	
PGM Pulse Width	$t_{PW}$	—	300	500	
Data Valid from OE	$t_{OE}$	75	—	—	ns
OE Pulse Width	$t_{OEW}$	75	—	—	
Output Enable to Output Float Delay	$t_{OEH}$	0	—	130	

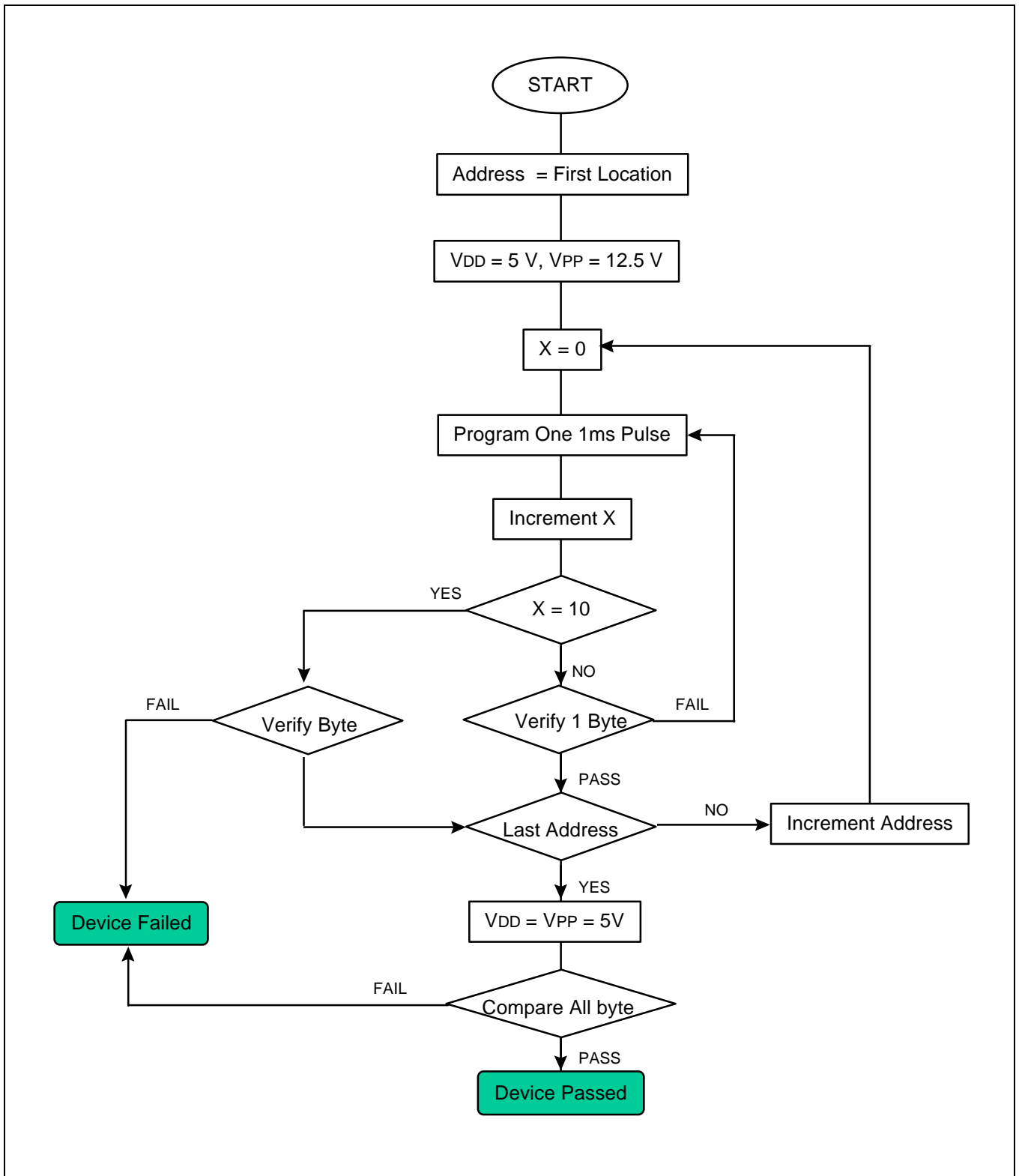


Figure 13-4. OTP Programming Algorithm

# 14 ELECTRICAL DATA

## OVERVIEW

In this section, S3C8095/P8095 electrical characteristics are presented in tables and graphs. The information is arranged in the following order:

- Absolute maximum ratings
- D.C. electrical characteristics
- Data retention supply voltage in Stop mode
- Stop mode release timing when initiated by an external interrupt
- Stop mode release timing when initiated by a Reset
- I/O capacitance
- A.C. electrical characteristics
- Input timing for external interrupts (port 0, P2.3–P2.0)
- Input timing for RESET
- Oscillation characteristics
- Oscillation stabilization time

Table 14-1. Absolute Maximum Ratings

 $(T_A = 25\text{ }^\circ\text{C})$ 

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	$V_{DD}$	–	– 0.3 to + 6.5	V
Input voltage	$V_{IN}$	–	– 0.3 to $V_{DD} + 0.3$	V
Output voltage	$V_O$	All output pins	– 0.3 to $V_{DD} + 0.3$	V
Output current High	$I_{OH}$	One I/O pin active	– 18	mA
		All I/O pins active	– 60	
Output current Low	$I_{OL}$	One I/O pin active	+ 30	mA
		Total pin current for ports 0, 1, and 2	+ 100	
		Total pin current for port 3	+ 20	
Operating temperature	$T_A$	–	– 20 to + 85	$^\circ\text{C}$
Storage temperature	$T_{STG}$	–	– 65 to + 150	$^\circ\text{C}$

Table 14-2. D.C. Electrical Characteristics

 $(T_A = -20\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $V_{DD} = 2.0\text{ V}$  to  $5.5\text{ V}$ )

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	$V_{DD}$	$f_{OSC} = 8\text{ MHz}$ (Instruction clock = 1.33 MHz)	2.4	—	5.5	V
		$f_{OSC} = 4\text{ MHz}$ (Instruction clock = 0.67 MHz)	2.0	—	5.5	
Input High voltage	$V_{IH1}$	All input pins except $V_{IH2}$ and $V_{IH3}$	$0.8 V_{DD}$	–	$V_{DD}$	V
	$V_{IH2}$	RESET	$0.95 V_{DD}$		$V_{DD}$	
	$V_{IH3}$	$X_{IN}$	$V_{DD} - 0.3$		$V_{DD}$	
Input Low voltage	$V_{IL1}$	All input pins except $V_{IL2}$ and $V_{IL3}$	0	–	$0.2 V_{DD}$	V
	$V_{IL2}$	RESET			$0.3 V_{DD}$	
	$V_{IL3}$	$X_{IN}$			0.3	
Output High voltage	$V_{OH1}$	$V_{DD} = 3.0\text{ V}$ $I_{OH} = -7\text{ mA}$ Port 3 only	$V_{DD} - 2.0$	–	–	V



Table 14-2. D.C. Electrical Characteristics (Continued)

(T<sub>A</sub> = -20 °C to +85 °C, V<sub>DD</sub> = 2.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output High voltage	V <sub>OH2</sub>	V <sub>DD</sub> = 3.0 V I <sub>OH</sub> = -200 μA All output pins except port 3	V <sub>DD</sub> - 1.0	-	-	V
Output Low voltage	V <sub>OL1</sub>	V <sub>DD</sub> = 3.0 V I <sub>OL</sub> = 1.5 mA, port 3 only	-	0.3	0.6	
	V <sub>OL2</sub>	I <sub>OL</sub> = 1 mA Ports 0, 1 and 2		0.4	1.0	
Input High leakage current	I <sub>LIH1</sub>	V <sub>IN</sub> = V <sub>DD</sub> ; all input pins except X <sub>IN</sub> and X <sub>OUT</sub>	-	-	1	μA
	I <sub>LIH2</sub>	V <sub>IN</sub> = V <sub>DD</sub> , X <sub>IN</sub> and X <sub>OUT</sub>			20	
Input Low leakage current	I <sub>LIL1</sub>	V <sub>IN</sub> = 0 V; all input pins except X <sub>IN</sub> , X <sub>OUT</sub> , and RESET	-	-	-1	μA
	I <sub>LIL2</sub>	V <sub>IN</sub> = 0 V, X <sub>IN</sub> and X <sub>OUT</sub>			-20	
Output High leakage current	I <sub>LOH</sub>	V <sub>OUT</sub> = V <sub>DD</sub> All output pins	-	-	1	μA
Output Low leakage current	I <sub>LOL</sub>	V <sub>OUT</sub> = 0 V All output pins	-	-	-1	μA
Pull-up resistors	R <sub>L1</sub>	V <sub>IN</sub> = 0 V; T <sub>A</sub> = 25 °C V <sub>DD</sub> = 5.0 V ± 10 % Ports 0-3	30	50	100	KΩ
Supply current (See Note)	I <sub>DD1</sub>	Operating mode; V <sub>DD</sub> = 5.0 V ± 10 % 4-MHz crystal	-	4.5	9	mA
	I <sub>DD2</sub>	Idle mode; V <sub>DD</sub> = 5.0 V ± 10 % 4-MHz crystal		1.6	3	
	I <sub>DD3</sub>	Stop mode; V <sub>DD</sub> = 5.0 V ± 10 %		0.3	3	μA
		V <sub>DD</sub> = 3.6 V		0.1	1	

**NOTE:** Supply current does not include current drawn through internal pull-up resistors or external output current loads.

Table 14-3. Data Retention Supply Voltage in Stop Mode

( $T_A = -20\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	$V_{DDDR}$	—	1.0	—	5.5	V
Data retention supply current	$I_{DDDR}$	$V_{DDDR} = 1.0\text{ V}$ Stop mode	—	—	1	$\mu\text{A}$

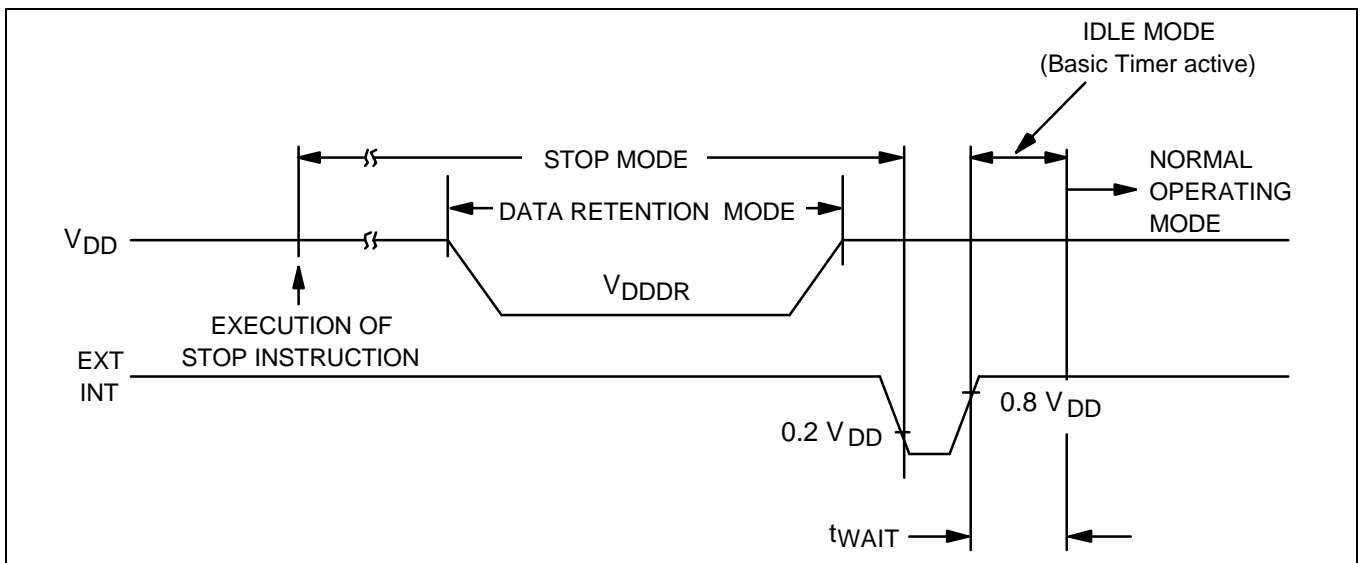


Figure 14-1. Stop Mode Release Timing When Initiated by an External Interrupt

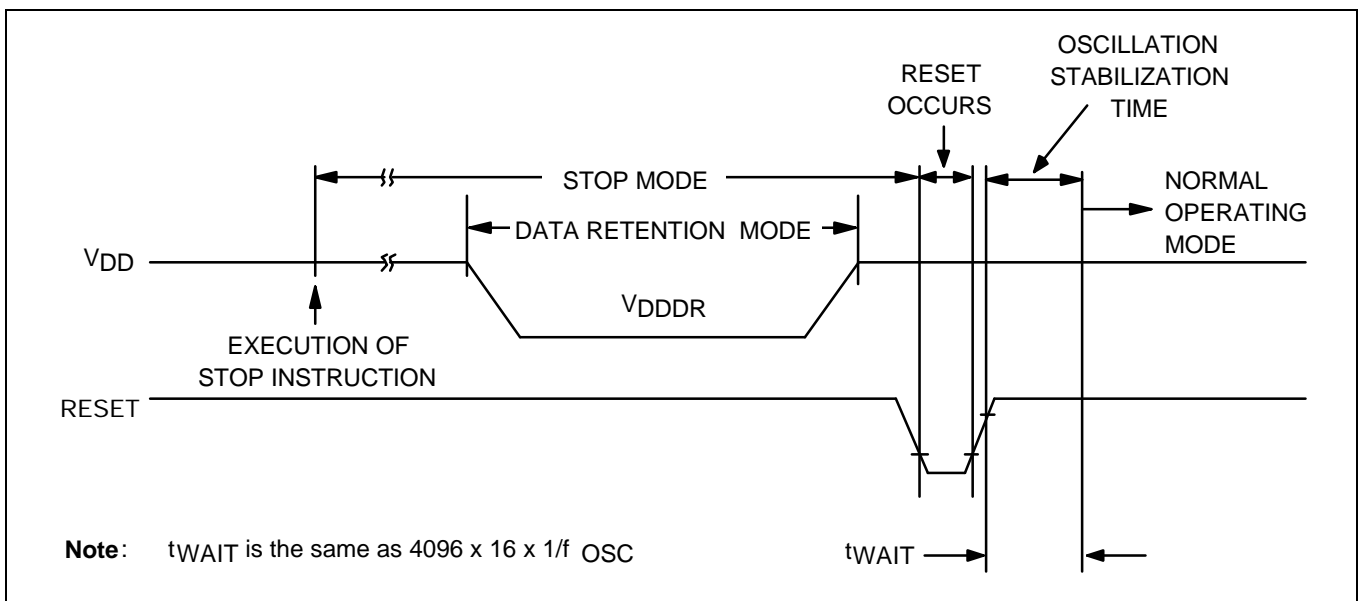


Figure 14-2. Stop Mode Release Timing When Initiated by a Reset

**Table 14-4. Input/Output Capacitance**

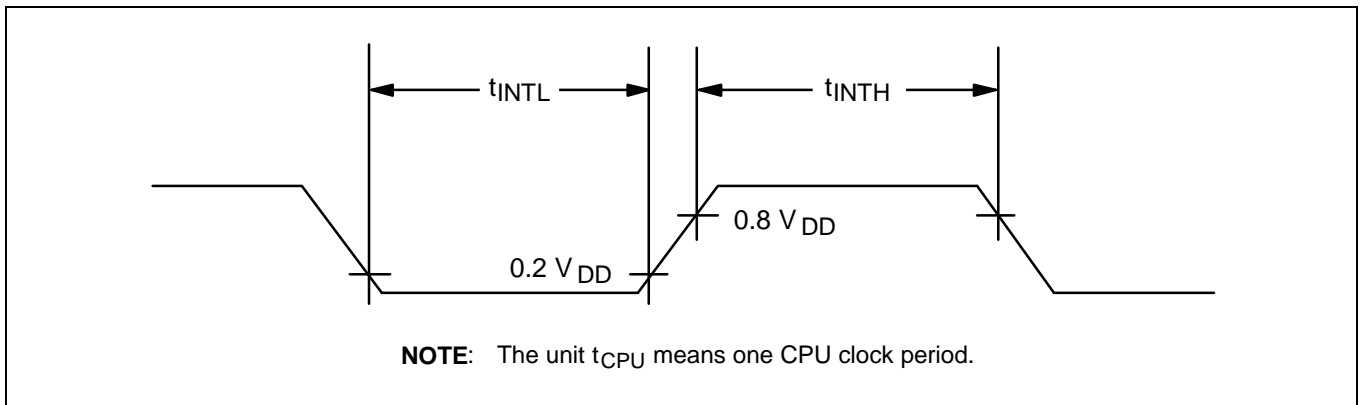
( $T_A = -20\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $V_{DD} = 0\text{ V}$ )

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	$C_{IN}$	f = 1 MHz; unmeasured pins are connected to $V_{SS}$	—	—	10	pF
Output capacitance	$C_{OUT}$					
I/O capacitance	$C_{IO}$					

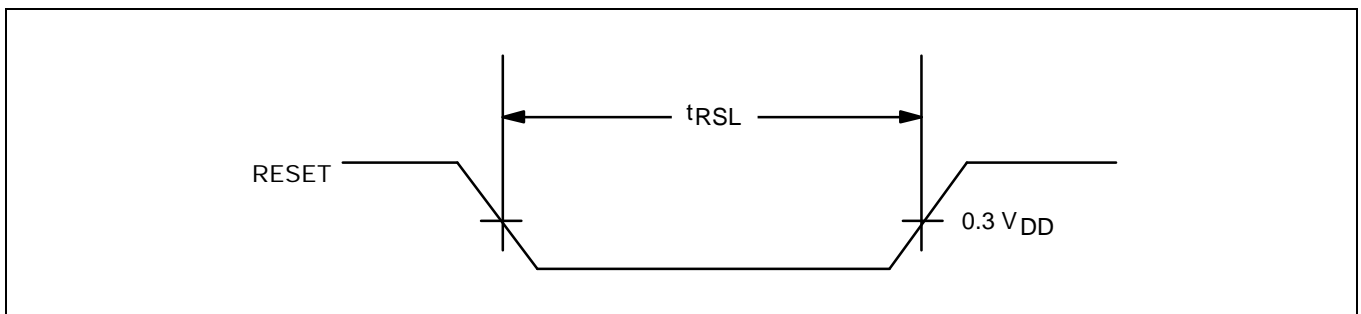
**Table 14-5. A.C. Electrical Characteristics**

( $T_A = -20\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Interrupt input, High, Low width	$t_{INTH}$ , $t_{INTL}$	P0.0–P0.7, P2.3–P2.0 $V_{DD} = 5\text{ V}$	200	300	—	ns
RESET input Low width	$t_{RSL}$	Input $V_{DD} = 5\text{ V}$	1000	—	—	



**Figure 14-3. Input Timing for External Interrupts (Port 0, P2.3–P2.0)**



**Figure 14-4. Input Timing for RESET**

Table 14-6. Oscillation Characteristics

 $(T_A = -20\text{ }^\circ\text{C} + 85\text{ }^\circ\text{C})$ 

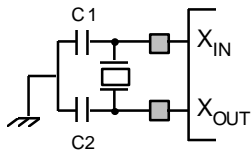
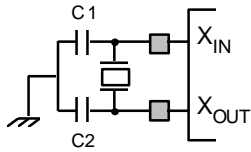
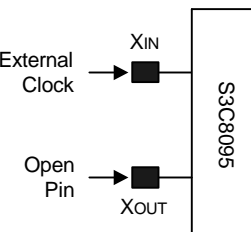
Oscillator	Clock Circuit	Conditions	Min	Typ	Max	Unit
Crystal		CPU clock oscillation frequency	0.4	—	8	MHz
Ceramic		CPU clock oscillation frequency	0.4	—	8	MHz
External clock		X <sub>IN</sub> input frequency	0.4	—	8	MHz

Table 14-7. Recommended Oscillator Constants

 $(T_A = -20\text{ }^\circ\text{C} + 85\text{ }^\circ\text{C}, V_{DD} = 4.5\text{ V to } 5.5\text{ V})$ 

Manufacturer	Product Name	Load Cap (pF)		Oscillator Voltage Range (V)		Remarks
		C1	C2	MIN	MAX	
TDK	FCR4.0MC5 (note)	—	—	2.0	5.5	On-chip C Leaded Type
	FCR4.0M5	33	33	2.0	5.5	Leaded Type
	CCR4.0MC3 (note)	—	—	2.0	5.5	On-chip C SMD Type
	FCR6.0MC5 (note)	—	—	2.0	5.5	On-chip C Leaded Type
	FCR6.0M5	33	33	2.0	5.5	Leaded Type
	CCR6.0MC3 (note)	—	—	2.0	5.5	On-chip C SMD Type
	FCR8.0MC5 (note)	—	—	2.0	5.5	On-chip C Leaded Type
	FCR8.0M5	33	33	2.0	5.5	Leaded Type
	CCR8.0MC5 (note)	—	—	2.0	5.5	On-chip C SMD Type

**NOTE:** On-chip C: 30 pF  $\pm$  20 % built in.

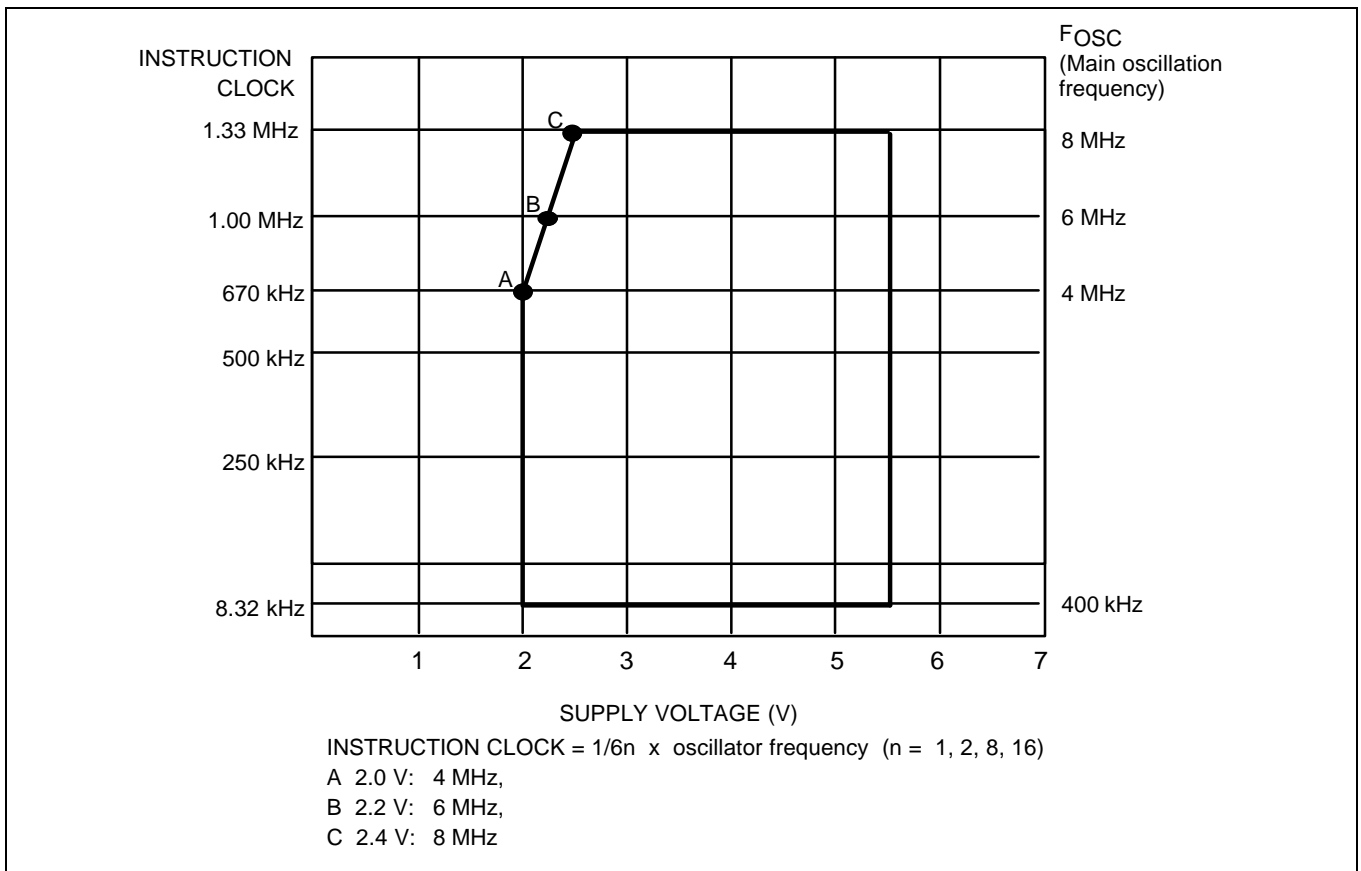
**Table 14-8. Oscillation Stabilization Time**

( $T_A = -20\text{ }^\circ\text{C} + 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 4.5\text{ V to } 5.5\text{ V}$ )

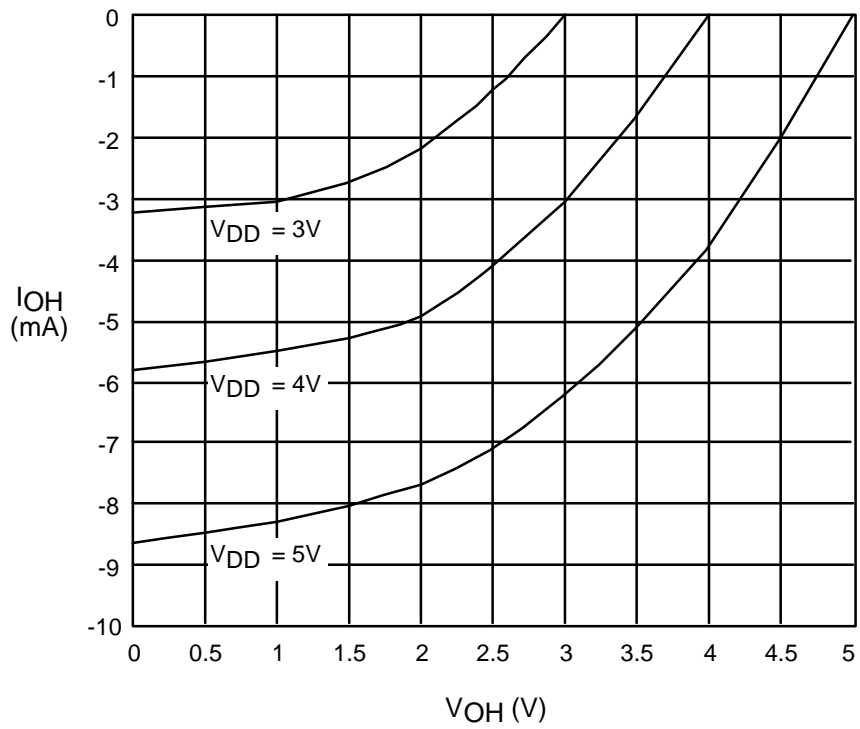
Oscillator	Test Condition	Min	Typ	Max	Unit
Main crystal	$f_{OSC} > 400\text{ kHz}$	—	—	20	ms
Main ceramic	Oscillation stabilization occurs when $V_{DD}$ is equal to the minimum oscillator voltage range.	—	—	10	ms
External clock (main system)	$X_{IN}$ input High and Low width ( $t_{XH}$ , $t_{XL}$ )	25	—	500	ns
Oscillator stabilization wait time	$t_{WAIT}$ when released by a reset <sup>(1)</sup>	—	$2^{16} / f_{OSC}$	—	ms
	$t_{WAIT}$ when released by an interrupt <sup>(2)</sup>	—	—	—	ms

**NOTES:**

- $f_{OSC}$  is the oscillator frequency.
- The duration of the oscillation stabilization time ( $t_{WAIT}$ ) when it is released by an interrupt is determined by the setting in the basic timer control register, BTCON.



**Figure 14-5. Operating Voltage Range**

Figure 14-6.  $I_{OH}$  vs.  $V_{OH}$  (Port 0)

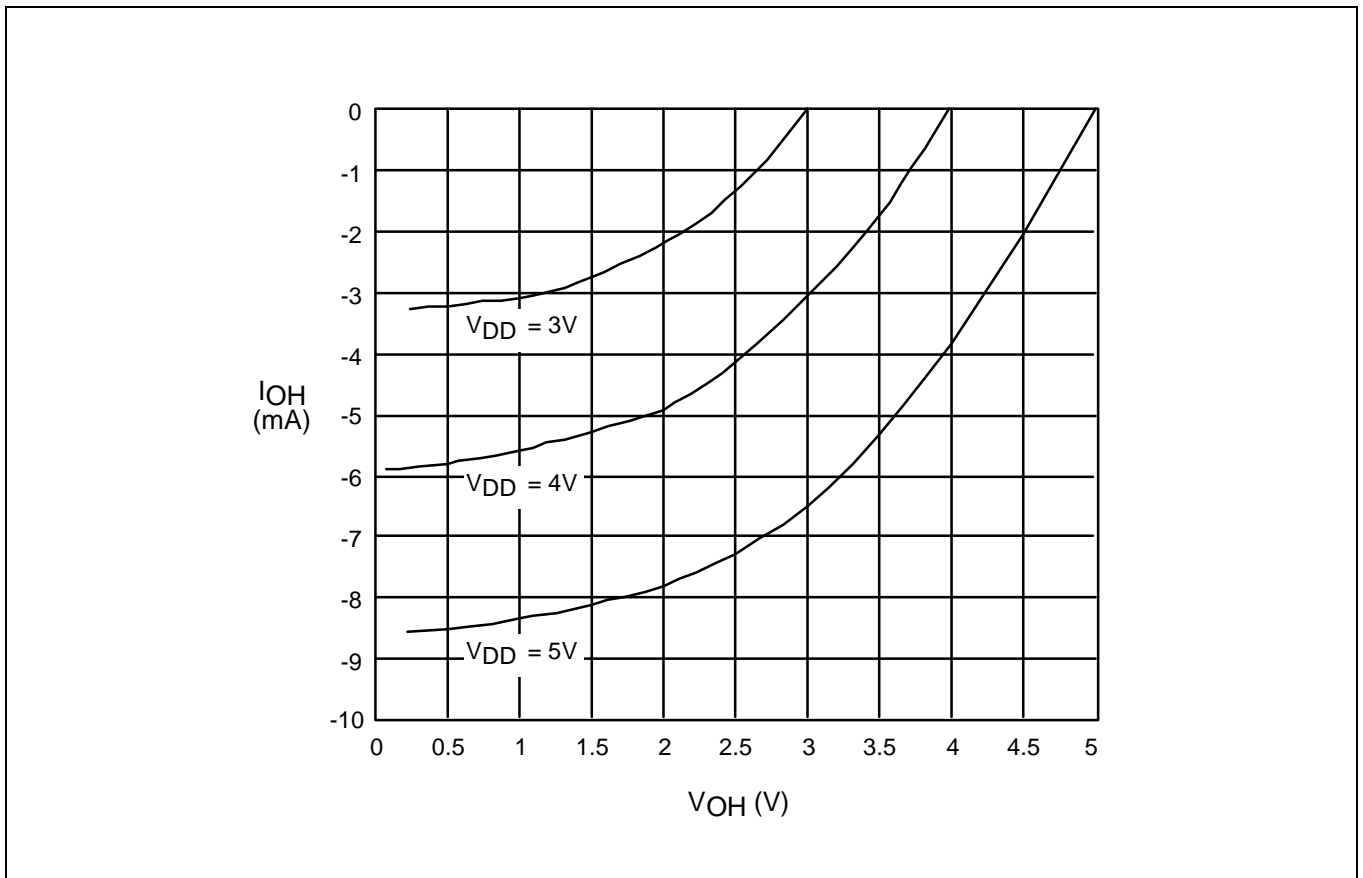
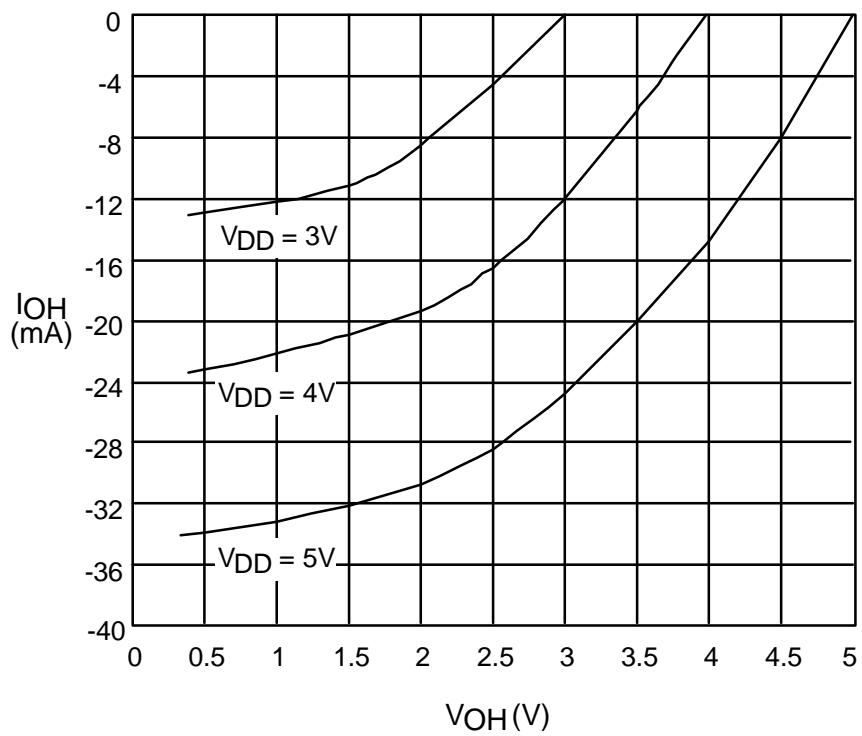


Figure 14-7.  $I_{OH}$  vs.  $V_{OH}$  (Port 2)

Figure 14-8.  $I_{OH}$  vs.  $V_{OH}$  (Port 3)



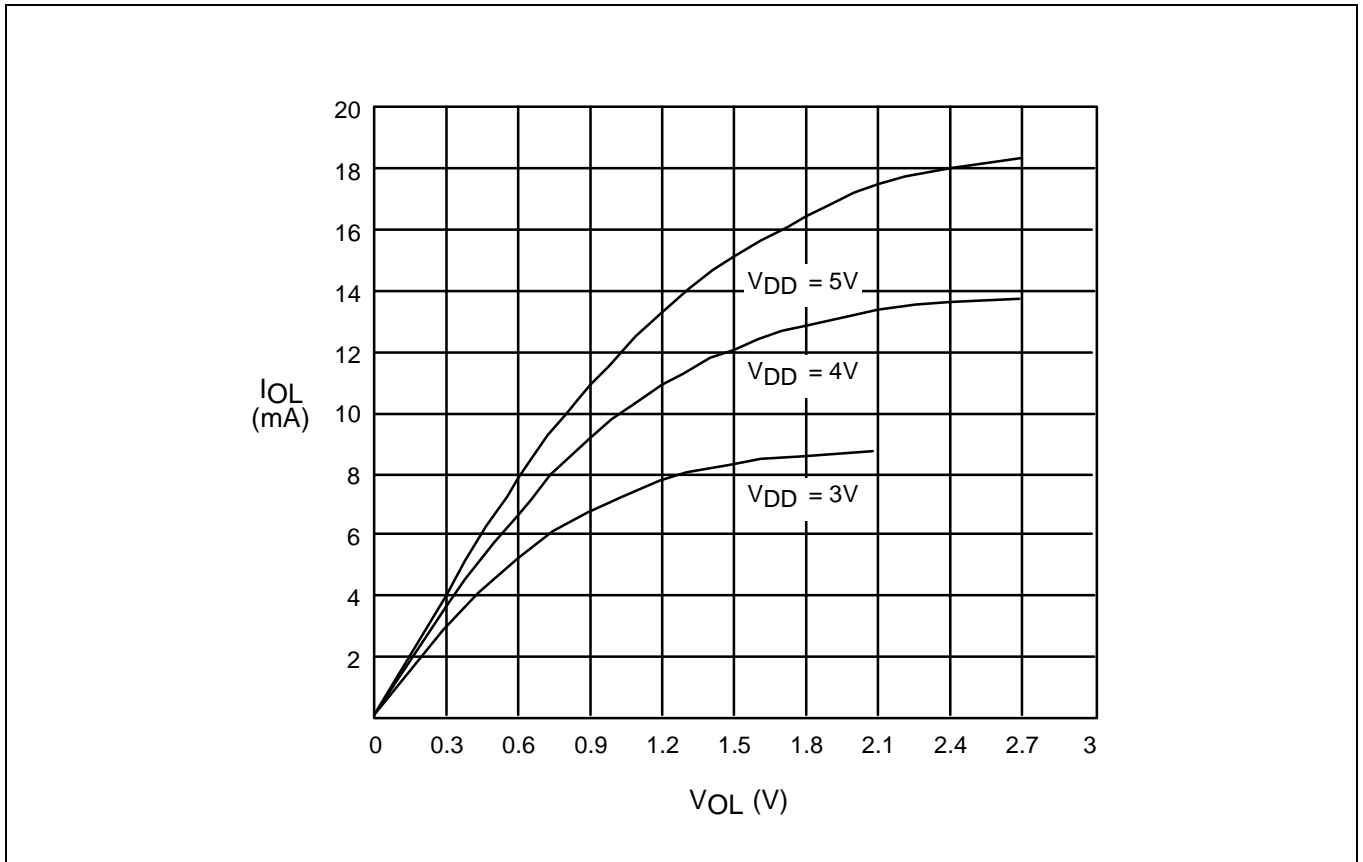
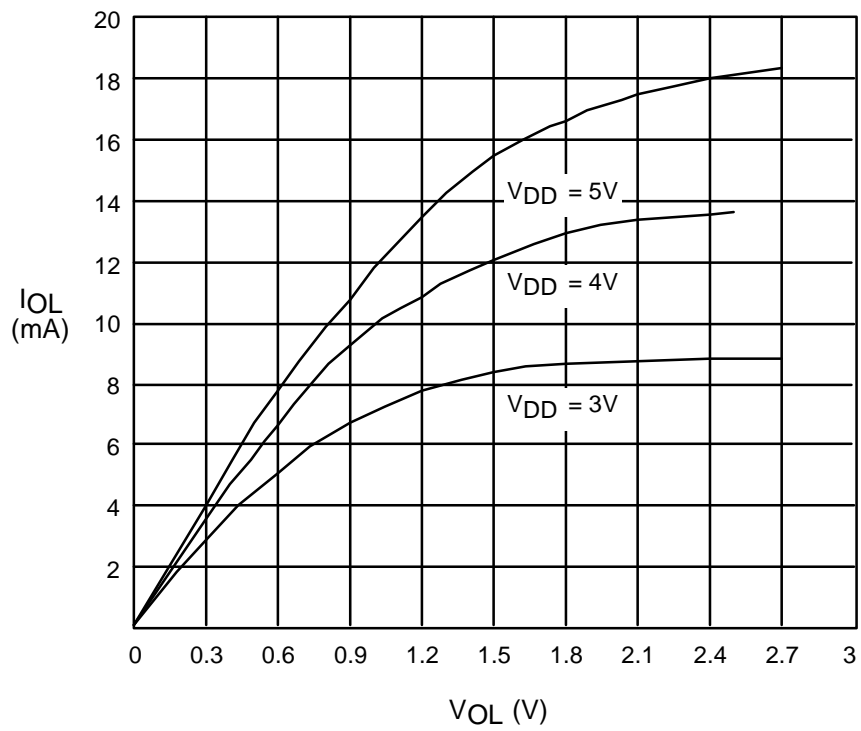
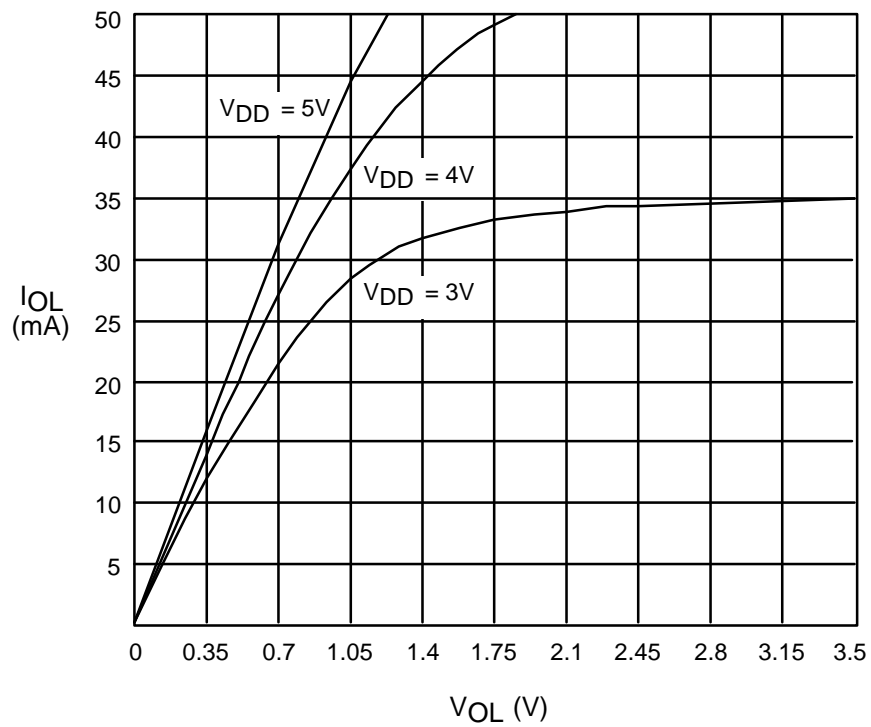


Figure 14-9. I<sub>OL</sub> vs. V<sub>OL</sub> (Port 0)

Figure 14-10.  $I_{OL}$  vs.  $V_{OL}$  (Port 2)

Figure 14-11.  $I_{OL}$  vs.  $V_{OL}$  (Port 3)

# 15 MECHANICAL DATA

## OVERVIEW

The S3C8095 microcontroller is currently available in a 32-pin SOP package.

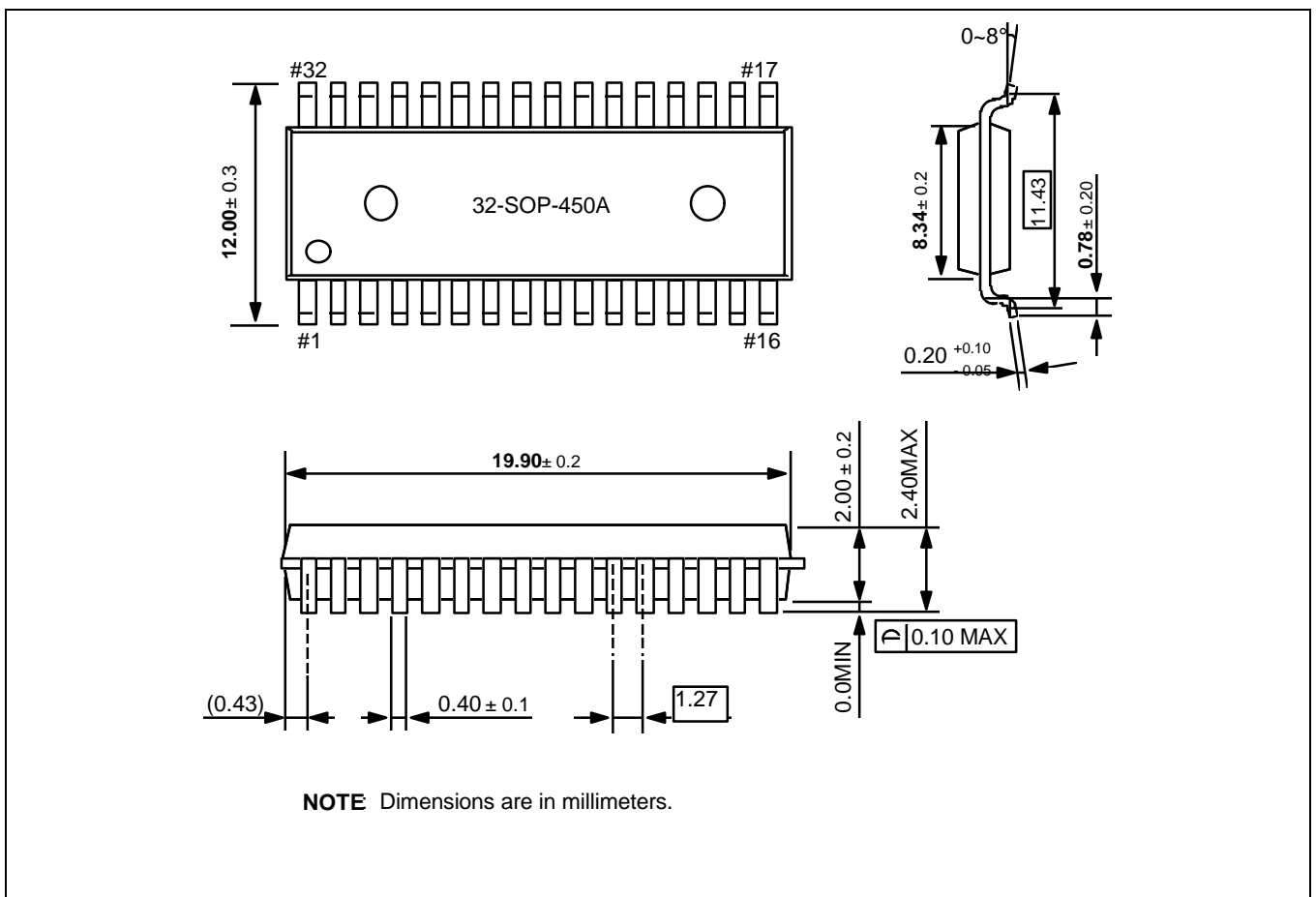


Figure 15-1. 32-Pin SOP Package Mechanical Data

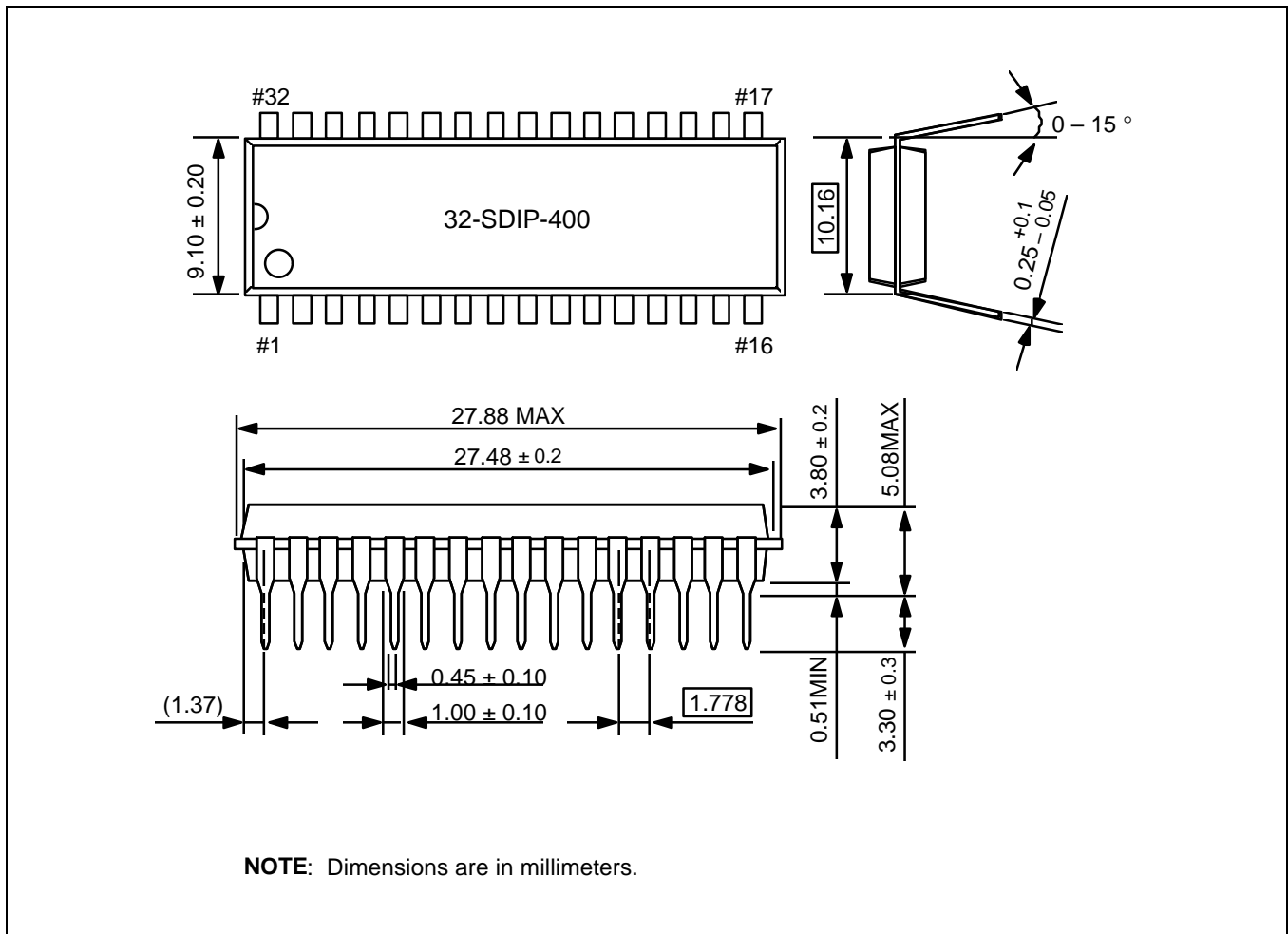


Figure 15-2. 32-Pin SDIP Package Mechanical Data