

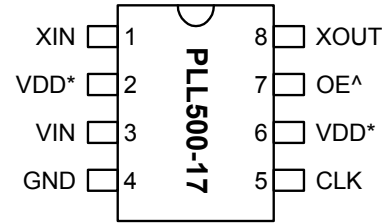
**Low Phase Noise VCXO (17MHz to 36MHz)**

**FEATURES**

- VCXO output for the 17MHz to 36MHz range
- Low phase noise (-130 dBc @ 10kHz offset at 35.328MHz).
- CMOS output with OE tri-state control.
- 17 to 36MHz fundamental crystal input.
- Integrated high linearity variable capacitors.
- 12mA drive capability at TTL output.
- +/- 150 ppm pull range, max 5% linearity.
- Low jitter (RMS): 2.5ps period jitter.
- 2.5 to 3.3V operation.
- Available in 8-Pin SOIC, 6-pin SOT23 packages, or DIE.

**BLOCK DIAGRAM**

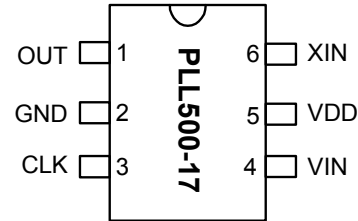
**PIN CONFIGURATION**



^: Denotes internal Pull-up  
\*: Only one VDD pin needs to be connected

**DESCRIPTION**

The PLL500-17 is a low cost, high performance and low phase noise VCXO for the 17 to 36MHz range, providing less than -130dBc at 10kHz offset at 35.328MHz. The very low jitter (2.5 ps RMS period jitter) makes this chip ideal for applications requiring voltage controlled frequency sources. Input crystal can range from 17 to 36MHz (fundamental resonant mode).

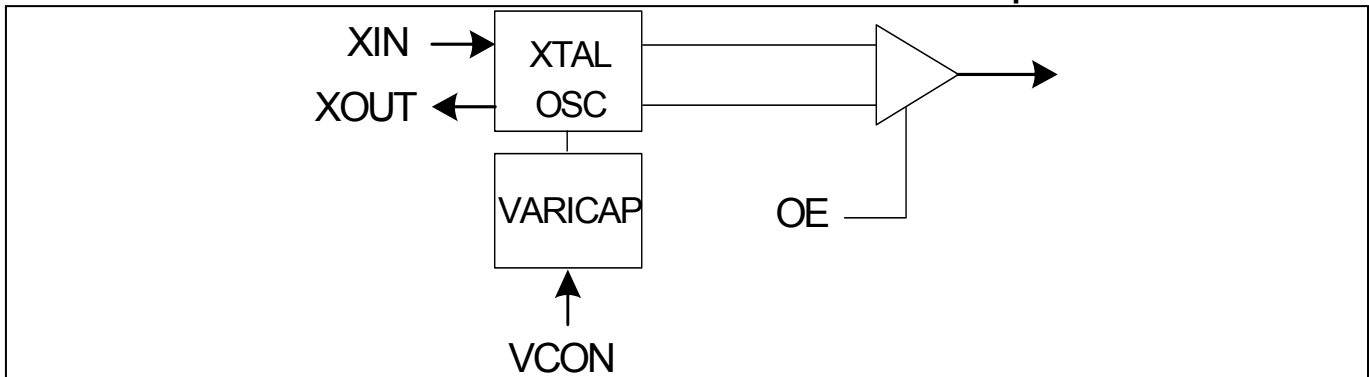


**8-pin SOIC**

**6-pin SOT**

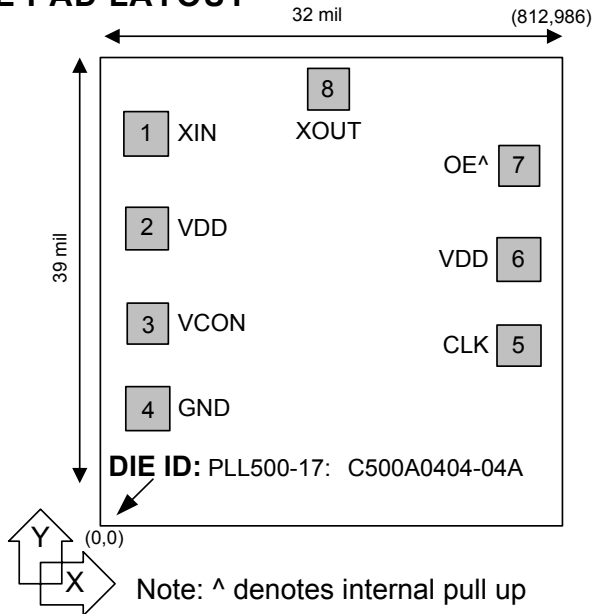
**FREQUENCY RANGE**

MULTIPLIER	FREQUENCY	OUTPUT BUFFER
No PLL	17 – 36 MHz	CMOS



## Low Phase Noise VCXO (17MHz to 36MHz)

### DIE PAD LAYOUT



### DIE SPECIFICATIONS

Name	Value
Size	39 x 32 mil
Reverse side	GND
Pad dimensions	80 micron x 80 micron
Thickness	10 mil

### PIN ASSIGNMENT (8-pin SOIC package) AND PAD DESCRIPTION (8-pin SOIC package)

Name	Pin#	Die Pad Position		Type	Description
		X (μm)	Y (μm)		
XIN	1	94.183	768.599	I	Crystal input pin.
VDD	2	94.157	605.029	P	VDD power supply pin. Only one VDD pin is necessary.
VCON	3	94.183	331.756	I	Frequency control voltage input pin.
GND	4	94.193	140.379	P	Ground pin.
CLK	5	715.472	203.866	O	Output clock pin.
VDD	6	715.307	455.726	P	VDD power supply pin. Only one VDD pin is necessary.
OE	7	715.472	626.716	I	Output Enable input pin. Disables the output when low. Internal pull-up enables output by default if pin is not connected to low.
XOUT	8	476.906	888.881	I	Crystal output pin. Ref Clock input.

\* OE (Output Enable) pin is not available in SOT-26 package, the output will always be enabled by the build in pull-up resistor.

### PIN ASSIGNMENT AND DESCRIPTION (6-pin SOIC package)

Name	Pin#	Type	Description
XOUT	1	I	Crystal Output pin. Ref. Clock input.
GND	2	P	Ground pin.
CLK	3	O	Output clock pin.
VCON	4	I	Frequency control voltage input pin.
VDD	5	P	VDD power supply pin.
XIN	6	I	Crystal input pin.

**Low Phase Noise VCXO (17MHz to 36MHz)**
**ELECTRICAL SPECIFICATIONS**
**1. Absolute Maximum Ratings**

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	$V_{DD}$		4.6	V
Input Voltage, dc	$V_I$	-0.5	$V_{DD}+0.5$	V
Output Voltage, dc	$V_O$	-0.5	$V_{DD}+0.5$	V
Storage Temperature	$T_S$	-65	150	°C
Ambient Operating Temperature*	$T_A$	-40	85	°C
Junction Temperature	$T_J$		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

\* **Note:** Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

**2. AC Electrical Specifications**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Crystal Frequency			17		36	MHz
Output Clock Rise/Fall Time		0.8V ~ 2.0V with 10 pF load		1.15		ns
		0.3V ~ 3.0V with 15 pF load		3.7		
Output Clock Duty Cycle		Measured @ 1.4V	45	50	55	%
Short Circuit Current				±50		mA

**3. Voltage Control Crystal Oscillator**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time *	$T_{VCXOSTB}$	From power valid			10	ms
VCXO Tuning Range		$F_{XIN} = 12 - 25\text{MHz};$ $XTAL C_0/C_1 < 250$ $0V \leq VCON \leq 3.3V$		300		ppm
CLK output pullability		$VCON=1.65V, \pm 1.65V$	±150			ppm
VCXO Tuning Characteristic				100		ppm/V
Pull range linearity					5	%
Power Supply Rejection	PWSRR	Frequency change with $V_{DD}$ varied +/- 10%	-1		+1	ppm
VCON pin input impedance			2000			kΩ
VCON modulation BW		$0V \leq VCON \leq 3.3V, -3\text{dB}$	45			kHz

**Note:** Parameters denoted with an asterisk (\*) represent nominal characterization data and are not production tested to any specific limits.

**4. Jitter and Phase Noise Specifications**

## Low Phase Noise VCXO (17MHz to 36MHz)

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
RMS Period Jitter (1 sigma – 1000 samples)	With capacitive decoupling between VDD and GND.		2.5		ps
Phase Noise relative to carrier	36MHz @100Hz offset		-80		dBc/Hz
Phase Noise relative to carrier	36MHz @1kHz offset		-110		dBc/Hz
Phase Noise relative to carrier	36MHz @10kHz offset		-130		dBc/Hz
Phase Noise relative to carrier	36MHz @100kHz offset		-138		dBc/Hz
Phase Noise relative to carrier	36MHz @1MHz offset		-145		dBc/Hz

### 5. DC Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic, with Loaded Outputs	$I_{DD}$	$F_{XIN} = 36\text{MHz}$ Output load of 15pF		5	6	mA
Operating Voltage	$V_{DD}$		2.25		3.63	V
Output Low Voltage at CMOS level	$V_{OLC}$	$I_{OL} = +4\text{mA}$			0.4	V
Output High Voltage at CMOS level	$V_{OHC}$	$I_{OH} = -4\text{mA}$	$V_{DD} - 0.4$			V
Output drive current		For $V_{OL} < 0.4\text{V}$ or $V_{OH} > 2.4\text{V}$	8	9.5		mA
Short Circuit Current				$\pm 50$		mA
VCXO Control Voltage	VCON		0		$V_{DD}$	V

### 6. Crystal Specifications

PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	$F_{XIN}$	17		36	MHz
Crystal Loading Rating (VCON = 1.65V)	$C_L (xtal)$		8.5		pF
Maximum Sustainable Drive Level				200	$\mu\text{W}$
Operating Drive Level			50		$\mu\text{W}$
C0				5	pF
C0/C1				250	-
ESR	$R_s$			30	$\Omega$

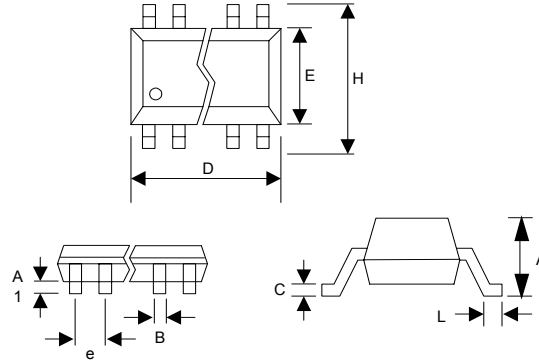
**Note:** The crystal must be such that it oscillates (parallel resonant) at nominal frequency when presented a C Load as specified above. If the crystal requires more load to be at nominal frequency, the additional load must be added externally. This however may reduce the pull range.

**Low Phase Noise VCXO (17MHz to 36MHz)**

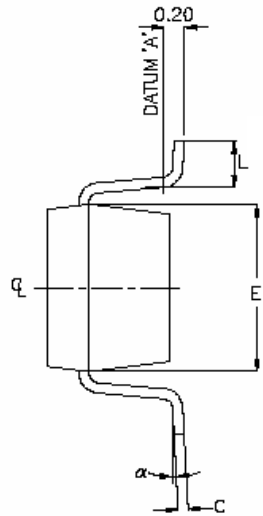
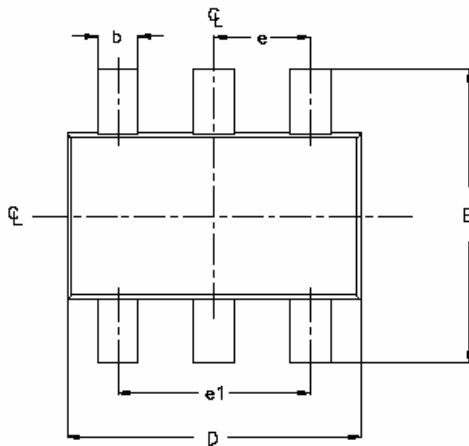
**PACKAGE INFORMATION**

8 PIN ( dimensions in mm )

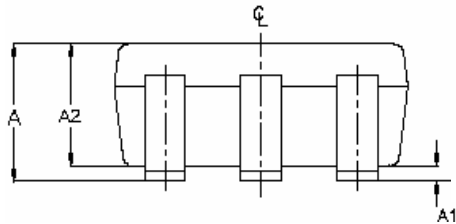
Narrow SOIC		
Symbol	Min.	Max.
A	1.47	1.73
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	4.95
E	3.80	4.00
H	5.80	6.20
L	0.38	1.27
e	1.27 BSC	



6-pin SOT (Dimensions in mm)



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.25	0.50
c	0.09	0.20
D	2.80	3.10
E	2.80	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95ref	
e1	1.90ref	
alpha	0°	10°



FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.

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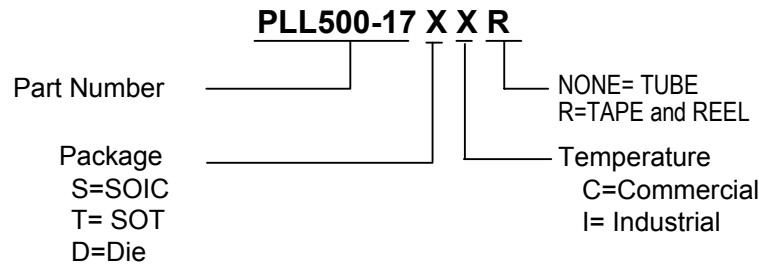
**ORDERING INFORMATION**

**For part ordering, please contact our Sales Department:**

47745 Fremont Blvd., Fremont, CA 94538, USA  
Tel: (510) 492-0990 Fax: (510) 492-0991

**PART NUMBER**

The order number for this device is a combination of the following:  
Device number, Package type and Operating temperature range



Part / Order Number	Marking	Package Option
PLL500-17DC	P500-17DC	Die (Waffle Pack)
PLL500-17SC	P500-17	8-Pin SOIC (Tube)
PLL500-17SC-R	P500-17	8-Pin SOIC (Tape and Reel)
PLL500-17SCL	P500-17L	8-Pin SOIC (Tube)
PLL500-17SCL-R	P500-17L	8-Pin SOIC (Tape and Reel)
PLL500-17TC	P500-17	6-Pin SOT (Tube)
PLL500-17TC-R	P500-17	6-Pin SOT (Tape and Reel)
PLL500-17TCL	P500-17L	6-Pin SOT (Tube)
PLL500-17TCL-R	P500-17L	6-Pin SOT (Tape and Reel)

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