MITSUBISHI 〈DIGITAL ASSP〉

M66335FP

FACSIMILE IMAGE DATA PROCESSOR

DESCRIPTION

The M66335 is a facsimile image processing controller to turn into binary signals analog signals which have been output through photoelectric conversion by the image sensor.

The image processing functions includes peak value detection, uniformity correction, resolution change, MTF compensation, γ correction, detection of background/character levels, error diffusion, separation of image zones, and designation of regions.

This controller contains not only the analog processing circuit, the A/D converter of a 7-bit flash type and image processing memory, but also the image sensor and the interface circuit to the CODEC (Coder and Decoder). Therefore, this LSI alone is capable of image processing.

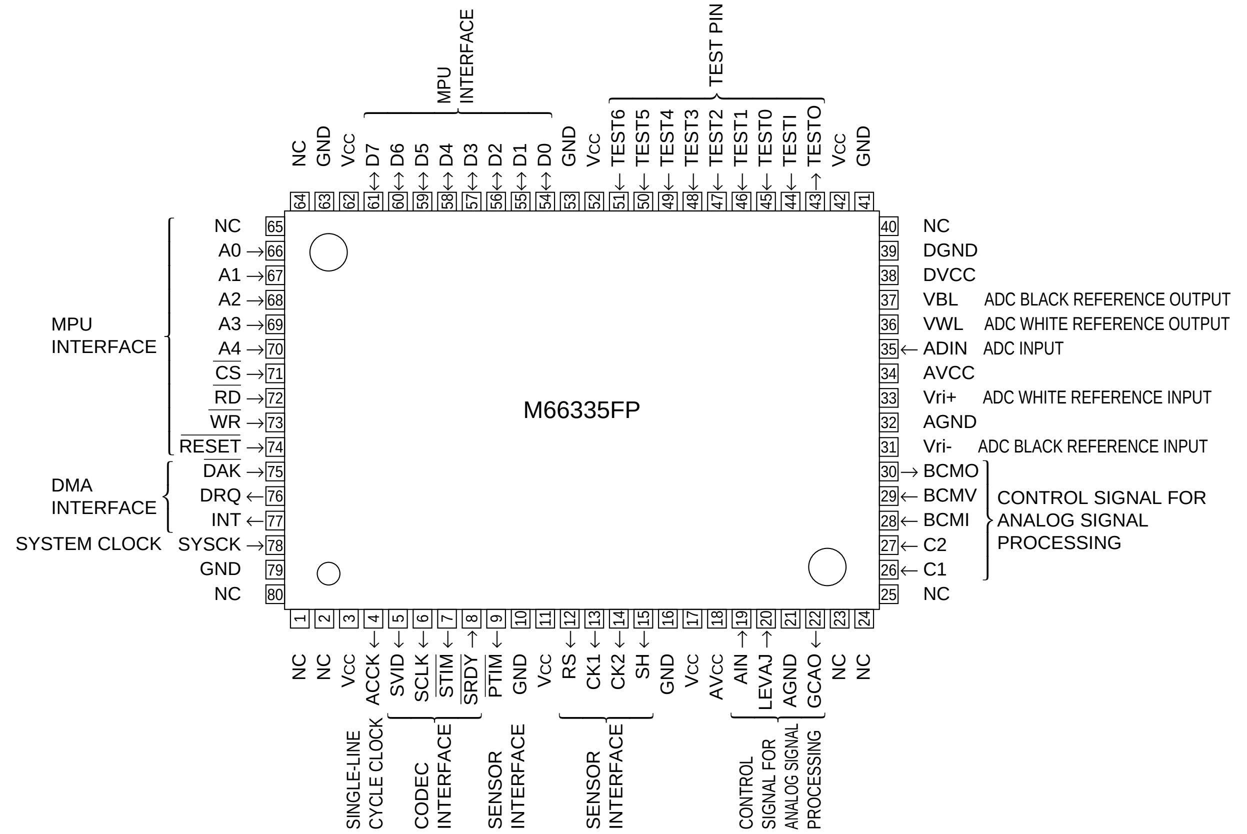
FEATURES

- High speed scan (max. 2 ms/line, typ. 5 ms/line)
- Compatibility with up to the B4 (8 pixels/mm, 16 pixels/mm) image sensor
- Generation of control signals for the image sensor (CCD, CIS)
  For CCD: SH, CK1, CK2, RS
  For the contact sensor (CIS): SH, CK1, CK2
- Built-in analog processing circuit (equivalent to the M64291)
  Sample and hold circuit
  Gain control circuit
  Black level clamping circuit
  Reference internal power supply for the A/D converter
- Built-in A/D converter of a 7-bit flash type
- Built-in image processing memories
  Uniformity correction memory, Line memory, Error memory, γ correction memory
- External output interface for converted binary data
  Serial output (→ M66330)
  DMA output
- External output interface for multivalued data
  DMA transfer of data compensated for uniformity
- Various image processing functions
  Uniformity correction
  Resolution change from 50% to 200% (by the 1% step)
  MTF compensation (2-dimensional processing, capable of correction for each character/photo)
  γ correction (capable of correction for each character/photo)
  Detection of background/character levels
  Change to pseudo-halftone
    - Error diffusion (64 tone steps through 6-bit processing)
    - Organized dither (64 tone steps through the 8 × 8 matrix)
  Image zone separation (2-dimensional processing)
- 5V single power supply

APPLICATION

Facsimile, word processor and image scanner

PIN CONFIGURATION (TOP VIEW)



Outline 80P6N–A

NC: No Connection

BLOCK DIAGRAM

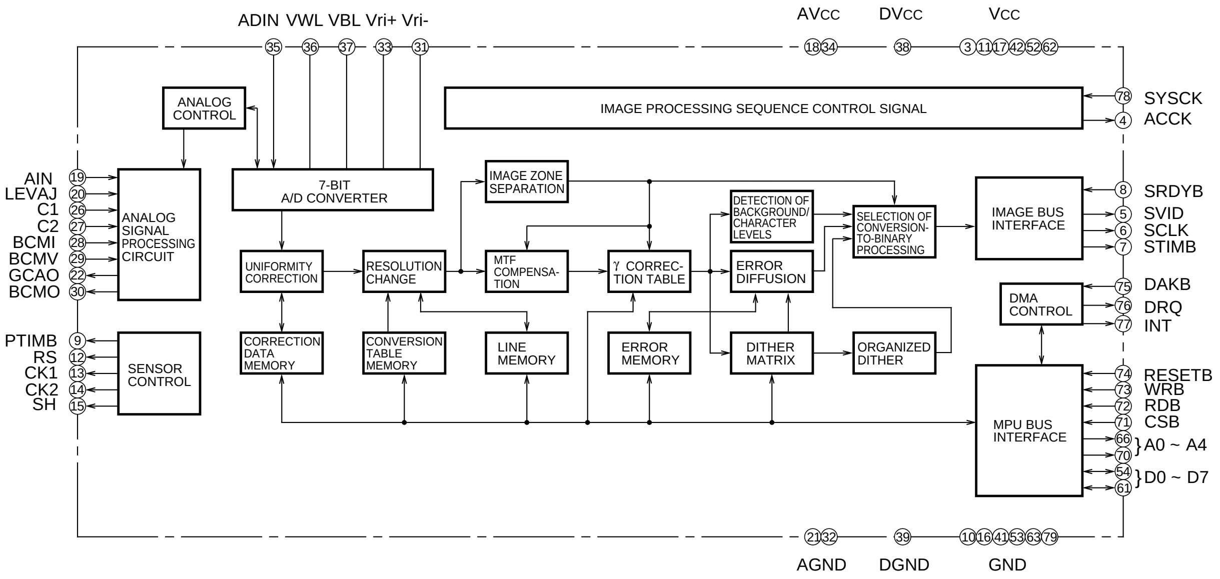


Table 1 Image processing functions

Image processing functions	Specifications	Remarks
Reading range	• A4, B4	
Resolution	• 8 pixels/mm, 16 pixels/mm (for the horizontal scanning direction)	
Reading speed	• Typ.: 5 ms/line; max.: 2 ms/line	• Controlled through the system clock.
Uniformity correction	• White correction, black correction • Correction range: 50%	• Correction memory is built in. • Readable from/writable in MPU
γ correction	• Logarithmic correction	• γ correction memory is built in. • Capable of correction for each character/photo.
MTF compensation	• Laplacian filter circuit through 2-dimensional processing	• Correction memory is built in. • Capable of correction for each character/photo.
Simple conversion to binary	• Floating slice system through the detection circuit for background/character levels	
Pseudo-halftone	• Error diffusion: 6-bit processing (for 64 tone steps) • Organized dither: 8 × 8 matrix (for 64 tone steps)	• Error buffer memory is built in. • 64W × 6 bits dither memory is built in.
Image zone separation	• 2-dimensional processing through luminance difference	
Image reduction	• Range of the reduction rate: 50% to 100% (by the 1% step)	• Capable of outputting the average line of a dropped line and the subsequent line instead of both lines
Image enlargement	• Range of the enlargement rate: 100% to 200% (by the 1% step)	• Capable of outputting the average line of a repeated line and the subsequent line instead of the repeated line
Image sensor control signal	• CIS image sensor (clock duty: 75%) • CCD image sensor	
Analog processing	• The sample/hold circuit, gain control amplifier, black level clamping circuit, and 7-bit A/D converter are built-in.	

DESCRIPTION OF DIGITAL PIN FUNCTIONS

Item	Pin name	Input/output	Function
Sensor interface	SH	Output	Outputs the shift pulse signal to transfer electric charges from the sensor’s photoconductor component to its transferring component for CCD and the start signal to start the sensor reading circuit for CIS.
	CK1	Output	Outputs the clock pulse signal to sequentially transfer out signaling electric charges from the sensor’s transferring component for CCD and the clock pulse signal for the shift register of the sensor reading circuit for CIS.
	CK2	Output	Reversed-phase pulses of CK1
	RS	Output	Outputs the reset pulse to return the voltage at the floating capacitor of the CCD sensor to the initial one.
	$\overline{\text{PTIM}}$	Output	Outputs the pulse motor control signal for the reading roller.
CODEC interface	$\overline{\text{SRDY}}$	Input	Transfer start ready signal for data from CODEC
	$\overline{\text{STIM}}$	Output	Defines the data transfer section to CODEC.
	SCLK	Output	Clock signal to transfer image data to CODEC
	SVID	Output	Outputs image data in serial to CODEC
DMA interface	DRQ	Output	DMA request signal to the external DMA controller to output in parallel image data through the MPU bus
	$\overline{\text{DAK}}$	Input	DMA acknowledge signal from the external DMA controller in response to the above DRQ signal
	INT	Output	Single-line termination interrupt
Clock	SYSCK	Input	System clock input pin
	ACCK	Output	Single-line cycle clock
MPU interface	$\overline{\text{RESET}}$	Input	Input of the system reset. The cycle counter, register, F/F, and latch are reset.
	$\overline{\text{CS}}$	Input	Chip select signal for MPU to access the M66335
	$\overline{\text{RD}}$	Input	Control signal for MPU to read data from the M66335
	$\overline{\text{WR}}$	Input	Control signal for MPU to write data to the M66335
	A0 ~ A4	Input	Address signal to access various registers inside the M66335
	D0 ~ D7	Input/Output	8 bit two way buffer
Others	VCC	—	Positive power supply pin
	GND	—	GND pin
	TESTI, 0~6	Input	Test input pin. Hold this at “L”.
	TESTO	Output	Test output pin. Set this open.

DESCRIPTION OF ANALOG PIN FUNCTIONS (Cont.)

Item	Pin name	Input/output	Function
Power supply	AVCC	—	Analog power supply pin (rated supply voltage: 5V)
	DVCC	—	Digital power supply pin (rated supply voltage: 5V)
GND	AGND	—	Analog ground pin
	DGND	—	Digital ground pin
Sensor signal input part	AIN	Input	Pin to input analog signals output from CCD or CIS (Signals from CCD are input through capacity coupling and those from CIS, with no clamping levels, are input directly.)
Gain control circuit	C1, C2	Input	Pin to control the frequency characteristic of the gain control circuit
	LEVAJ	Input	Pin to control the DC level of output signals of the gain control circuit. The output voltage, V_{GCAO}, is obtained by the following equation: $V_{GCAO} = V_{LEVAJ} + G_V \times V_{IN}$, where, V_{LEVAJ}: voltage at LEVAJ V_{IN}: input signal G_V: gain of the gain control circuit V_{IN} is the signal element corresponding to the signal level clamped through the input clamping circuit for CCD·CIS3 input or to the GND level for CIS1·CIS2 input.
	GCAO	Output	Signal output pin of the gain control circuit
Black level clamping circuit	BCMI	Input	Signal input pin to the black clamping circuit. Use this with capacity coupling with the GCAO pin.
	BCMV	Input	Pin to set the black level clamping voltage. Sets the black level of signals output from the BCMO pin for CCD signal processing.
	BCMO	Output	Signal output pin of the black level clamping circuit
A/D converter	Vri+	Input	Output of the circuit to generate the A/D full-scale point reference voltage (3.8V). Connected with VWL through the buffer inside the IC. To change the A/D reference voltage range, input a DC voltage from this pin.
	Vri–	Input	Output of the circuit to generate the A/D zero point reference voltage (1.8V). Connected with VBL through the buffer inside the IC. To change the A/D reference voltage range, input a DC voltage from this pin.
	ADIN	Input	Signal input pin to the A/D converting circuit. Use this by connecting with the BCMO pin for CCD or with the GCAO pin for CIS. Input signals in the voltage range (1.8V to 3.8V) set through VWL and VBL.
	VWL	Output	Output of the circuit generating the A/D full-scale reference voltage (3.8V). Connected inside the IC with the A/D converter.
	VBL	Output	Output of the circuit generating the A/D zero point reference voltage (1.8V). Connected inside the IC with the A/D converter.

(1) Operation mode

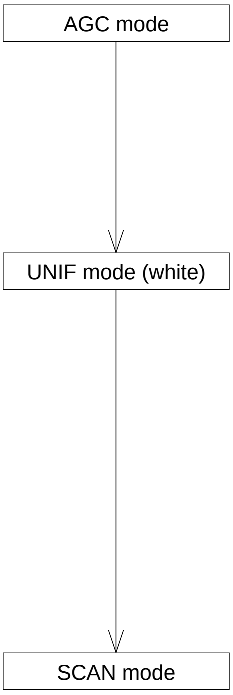
The M66335 has three basic operations.

- Peak value detection: Adjusting the peak value of analog signals output from the analog circuit to the white reference voltage (VWL) of the A/D converter built in the M66335.
- Generation of data for uniformity correction: Generating data on a white reference original sheet for uniformity correction by the sensor unit and writing them to the memory for correction built in the M66335.
- Read: Reading original sheets, performing image processing of the read image data, and outputting in serial or parallel the indicated converted binary data.

  The M66335 is capable of performing the DMA transfer of multivalued data (6-bit data=D7~D2, D1=D0=0) after correction about uniformities.

These three basic operations are performed in the following mode sequences for the CCD sensor and CIS sensor. The sensor is set through the register 00 (SENS).

For the CCD sensor

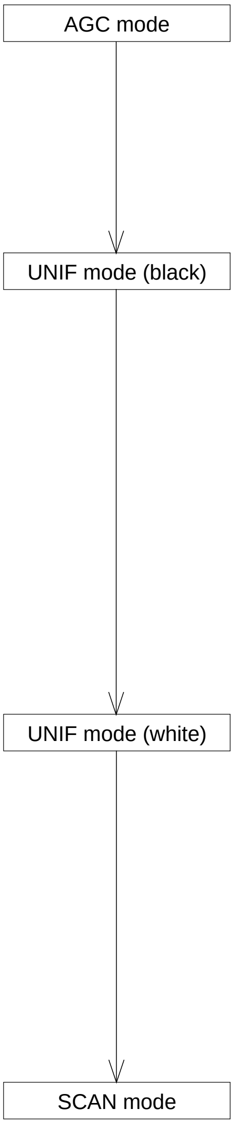


The peak value of the 16 line cycle is detected by setting the AGC command in the register 00 at “H”.
To escape this mode, set the AGC command at “L” after a 20 line cycle (or a cycle of 16 lines or more) passed since the start.

This operation mode is started by setting the UNIF command in the register 00 at “H” after setting UMODE: “H” (white correction) in the register 00 and UNIFM: “L” (only white correction) in the register 01. Starting by the UNIF command also makes the system generate data for non-uniformity correction for white correction (for the 8 line cycle).
To escape this mode, set the UNIF command at “L” after a 10 line cycle (or a cycle of 8 lines or more) passed since the start.

The read operation mode is started by setting the SCAN command in the register 00 at “H”. To escape this mode, set the SCAN command at “L”.

For the CIS sensor



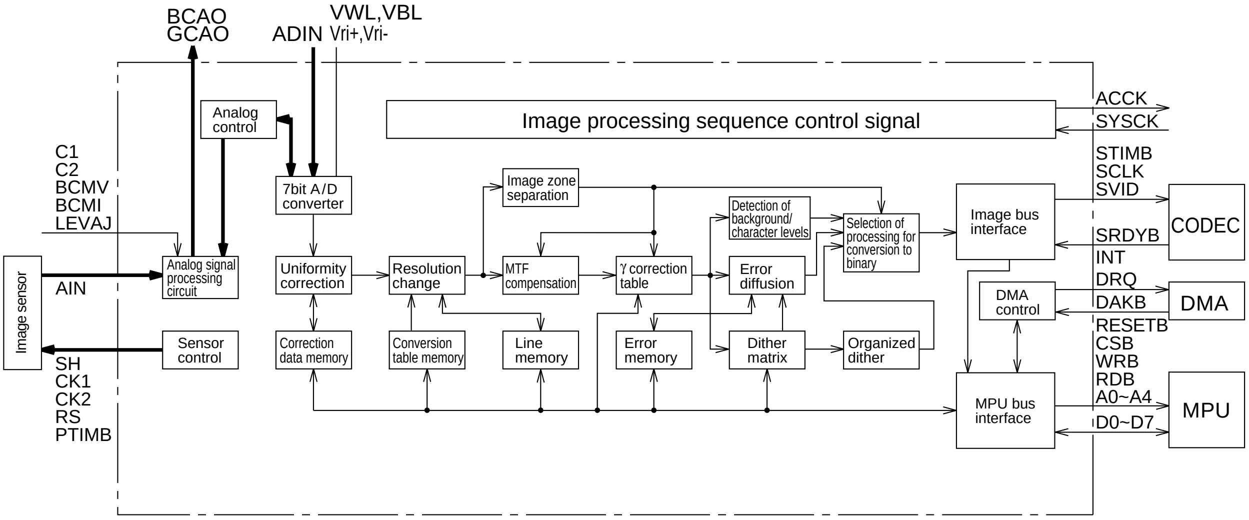
The peak value of the 16 line cycle is detected by setting the AGC command in the register 00 at “H”.
To escape this mode, set the AGC command at “L” after a 20 line cycle (or a cycle of 16 lines or more) passed since the start.

When this operation mode is started by the UNIF command after setting UMODE: “L” (black correction) in the register 00 and UNIFM: “H” (black and white correction) in the register 01, the system also generates black data for non-uniformity correction for black correction (for the 8 line cycle).
To escape this mode, set the UNIF command at “L” after a 10 line cycle (or a cycle of 8 lines or more) passed since the start.
In the case of only white correction, the setting is not necessary. Follow the instruction below.

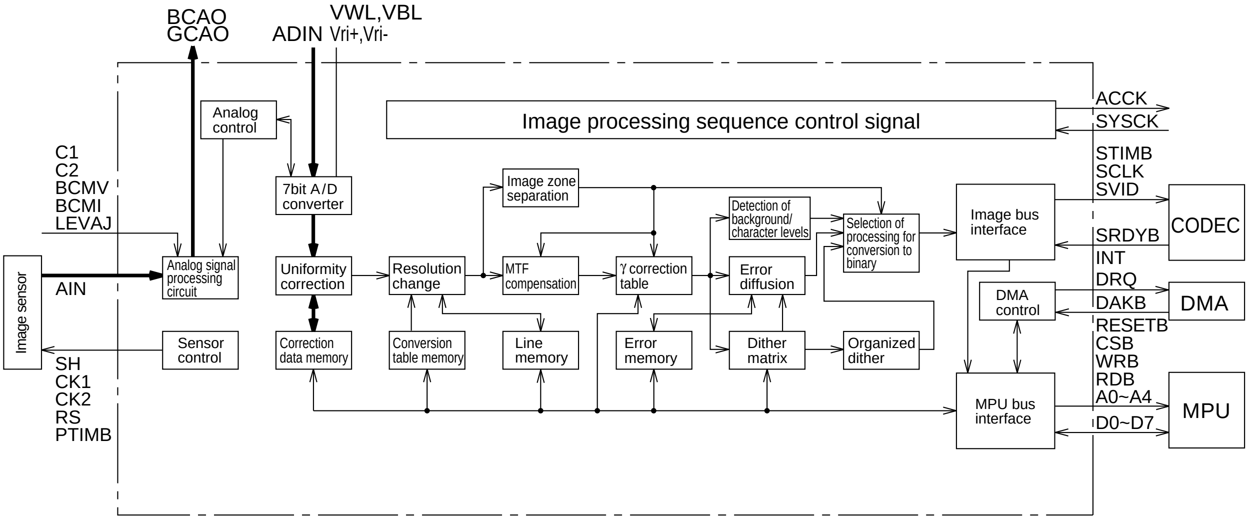
When this operation mode is started by the UNIF command in the register 00 after setting UMODE: “H” (white correction) in the register 00 and UNIFM: “L” (only white correction) in the register 01, the system also generates white data for non-uniformity correction for white correction (for the 8 line cycle).
To escape this mode, set the UNIF command at “L” after a 10 line cycle (or a cycle of 8 lines or more) passed since the start.

The reading operation is started by setting the SCAN command in the register 00 at “H”. To escape this mode, set the SCAN mode at “L”.
The signal operations and data flow in each basic operation are shown in the page 4-217 and 4-218, and the flowchart is in the page 4-260 and 4-261.

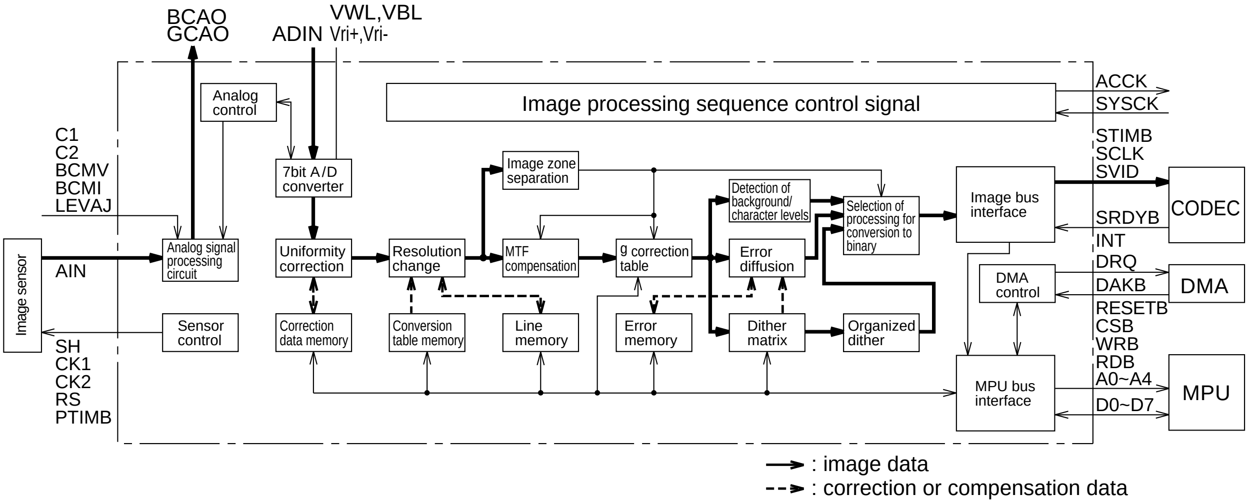
OPERATIONS OF SIGNALS IN THE PEAK VALUE DETECTION OPERATION



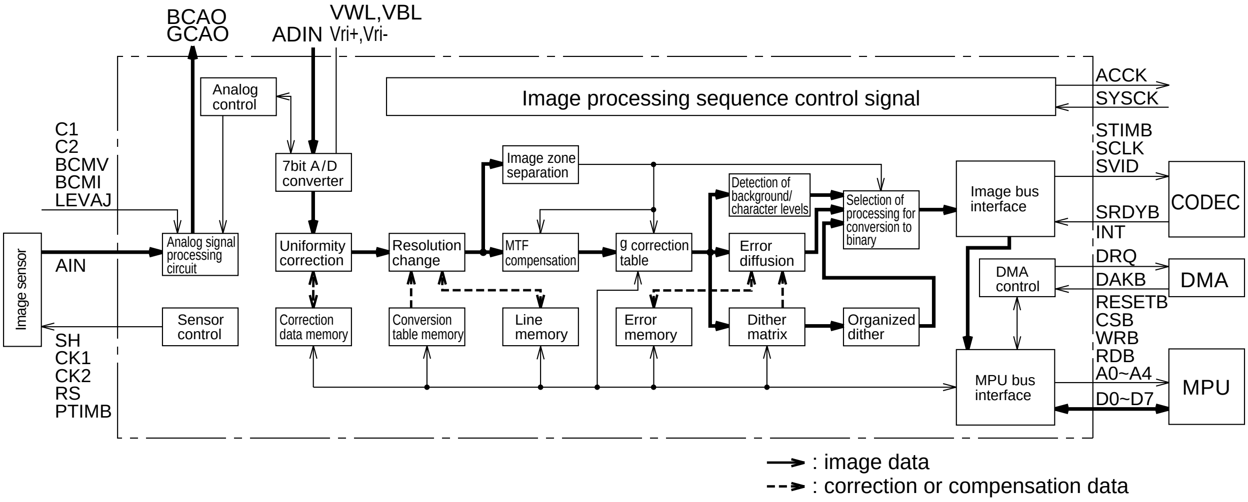
FLOW OF DATA IN THE CREATION OF DATA FOR UNIFORMITY CORRECTION



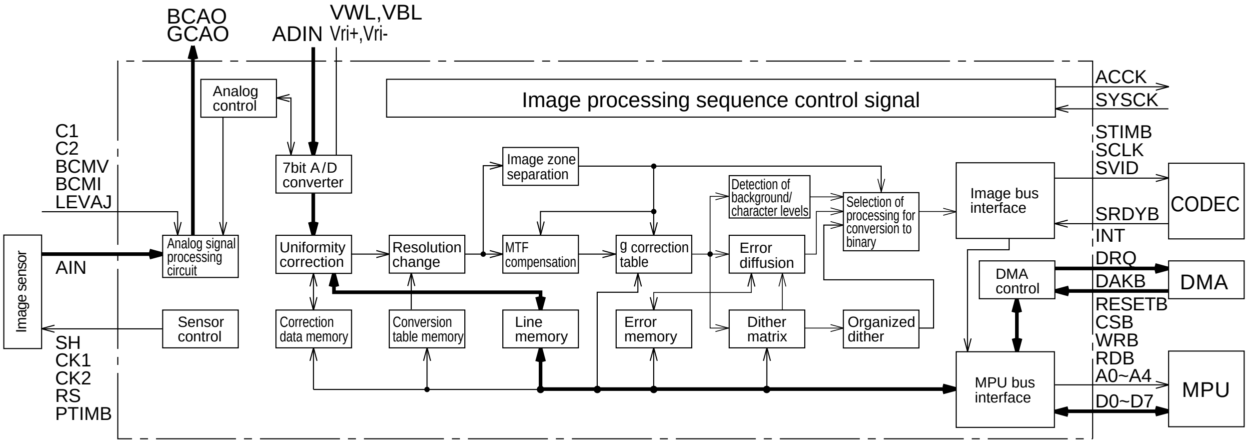
FLOW OF DATA IN THE READING OPERATION (FOR OUTPUT IN SERIAL: BINARY DATA)



FLOW OF DATA IN THE READING OPERATION (FOR OUTPUT IN PARALLEL: BINARY DATA)



FLOW OF SIGNALS IN THE READING OPERATION (FOR MULTIVATED DATA)



(2) Line cycle and reading sequence

The relationship between the line cycle and the reading sequence of the M66335 is shown in Fig. 1.

The relationship between the CODEC interface operations and the reading sequence is shown in Fig. 2 and that between the DMA interface operations and the reading sequence is shown in Fig. 3.

- Single-line cycle (1/ACCK):
  Defines the processing time per line of the M66335.
  The single-line cycle is decided by the line cycle counter value registers 03 and 04 (PRE_DATA), and the pixel transfer clock. The pixel transfer clock is 1/16 of SYSCK.
  1 line cycle (1/ACCK) [NS]
  = line cycle counter value × pixel transfer clock cycle [NS]
  = (PRE_DATA + 1) × pixel transfer clock cycle [NS]
  = (PRE_DATA + 1) × 16/SYSCK [NS]
  After loading the PRE_DATA value, the line cycle counter generates the addresses of the following gate signals while counting down with the pixel transfer clock.

- Sensor start pulse (SH):
  Image sensor start pulse. The point of the start pulse is decided by the uniformity correction range (UNIFG) and the value of the register 05.
  [ST_PL]
  The ST_PL value must be set according to the following formulas for each image sensor type.
  CCD: ST_PL = dummy pixels of the sensor + 2
  CIS: ST_PL = 2

- Uniformity correction range (UNIFG):
  Defines the range where uniformity correction is performed. This range corresponds to the width of the sensor (B4 to A4).
  For the relationship between the sensor width and the uniformity correction range, see Table 2.

- AGC range (AGCG):
  Defines the range where peak value detection is performed. This range corresponds to the sensor width (B4 to A4).
  Auto gain control is performed for the whole width of the sensor (solid line) in the AGC mode and for the narrower width (dashed line) than the sensor width in the SCAN mode.
  For the relationship between the sensor width and the AGC range, see Table 2.

- Original sheet reading width:
  Defines the reading width for original sheets.
  For original sheet widths narrower than the sensor width, the reading range (dashed line) is set, using the sensor center as the base center point. Therefore, the points for the original sheet should be based on the sensor center.
  For the relationship between the sensor width and the original sheet reading width, see Table 3.

- Pulse motor control signal ($\overline{\text{PTIM}}$):
  Generates control signals for the pulse motor for the reading roller.

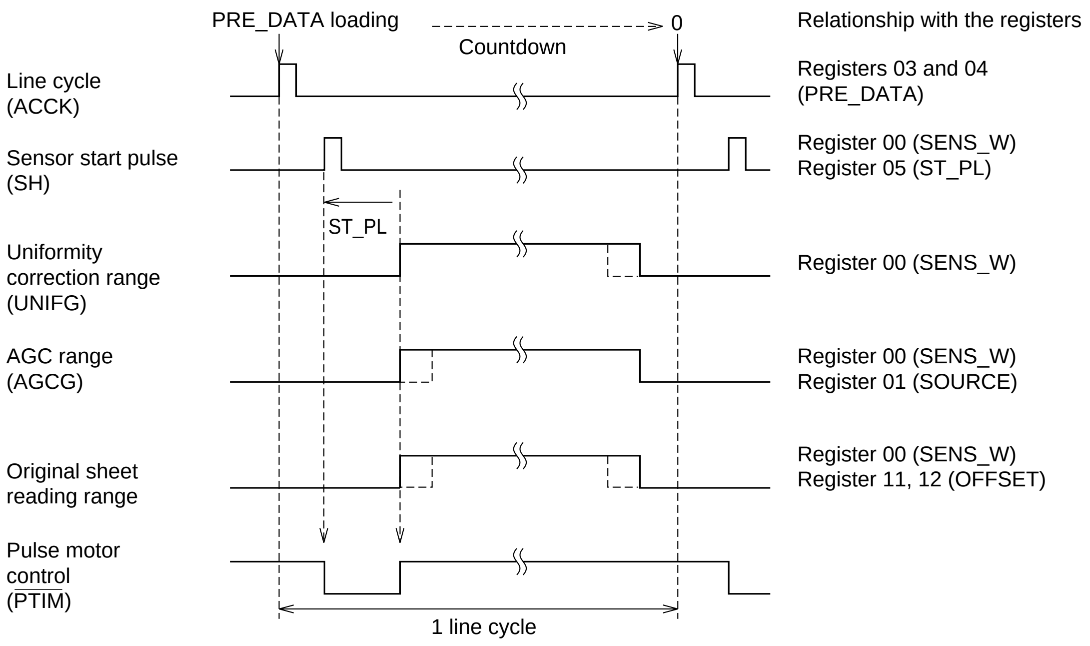
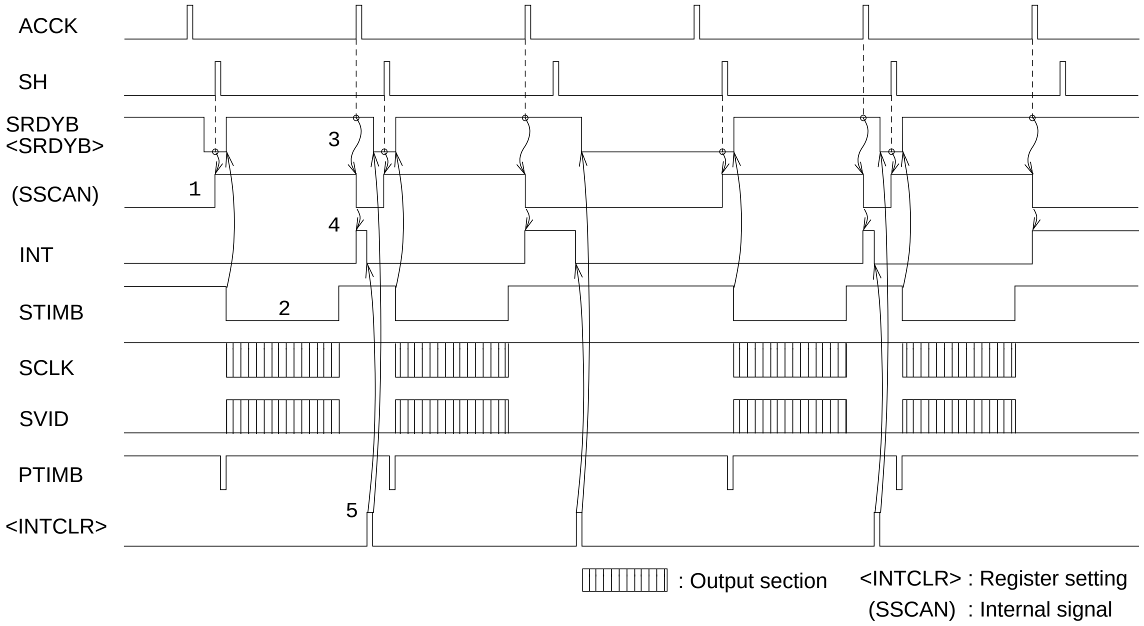
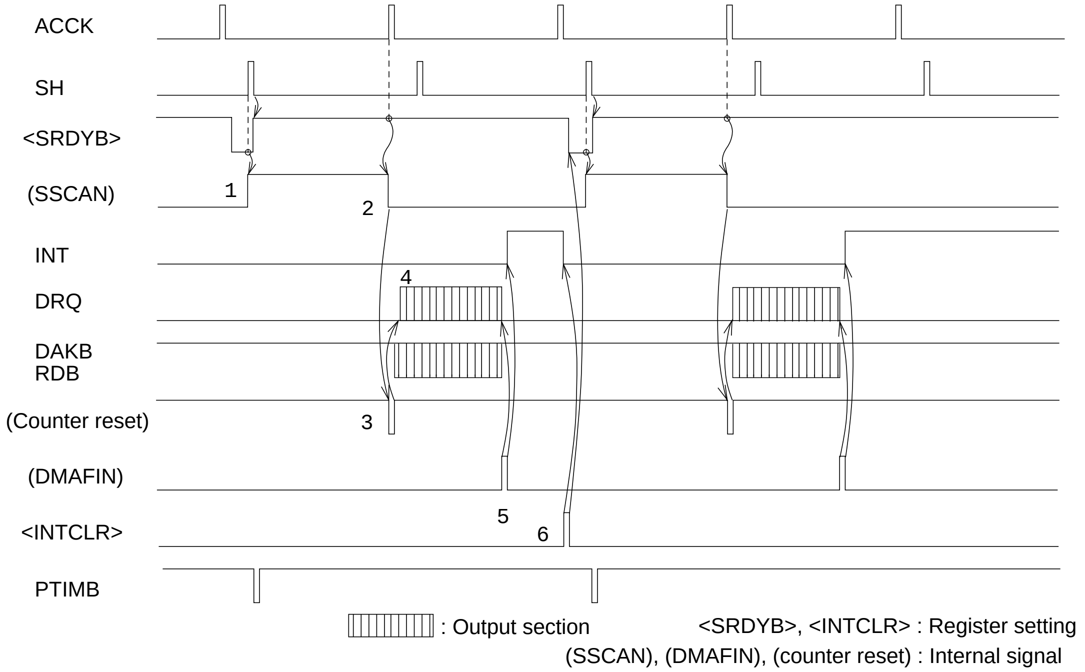


Fig. 1 Line cycle and the reading sequence



1 SRDYB : ‘L’ is taken in with a ↑ flow of SH, when scanning is started and PTIMB is output. (SSCAN : ‘H’)
2 During the period that STIMB is ‘L’, converted binary data are output.
3 SRDYB : ‘H’ is taken in with a ↑ flow of ACCK, when the reading of one line ends. (SSCAN : ‘L’)
4 INT is asserted with a ↓ flow of SSCAN. (INT : ‘H’)
5 When CPU is ready for reading the next line, INTCLR is generated and INT is negated, and then SRDYB is set ‘L’.

Fig. 2 CODEC interface operations and the reading sequence (Binary data output : sirial output)



1 SRDYB : ‘L’ is taken in with a ↑ flow of SH, when scanning is started and PTIMB is output. (SSCAN : ‘H’)
2 SRDYB : ‘H’ is taken in with a ↑ flow of ACCK, when the reading of one line ends. (SSCAN : ‘L’)
3 The internal counter reset signal is generated with a ↓ flow of SSCAN, and DRQ is asserted with a ↑ flow of SSCAN.
4 After the internal counter is reset, DMA transfer is started. (The internal counter is counted up by one each time a pixel is transferred.)
5 When the value of the internal counter reaches the output pixel number, DMAFIN shifts to ‘H’, and DRQ is negated with a ↑ flow form DMAFIN and INT is asserted with a ↓ flow of DMAFIN.
6 When CPU is ready for reading the next line, INTCLR is generated and INT is negated, and then SRDYB is set ‘L’.

Fig. 3 DMA interface operations and the reading sequence (Multivated data output)

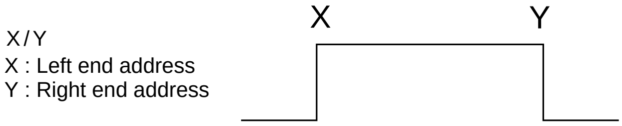
Table 2 Gate signal ranges for the sensor widths

Sensor width Gate signal		Resolution	B4	A4
Uniformity correction range (UNIFG)		200dpi	2103/55	1943/215
		400dpi	4207/111	3887/431
AGC range (AGCG)	AGC mode	200dpi	2103/55	1943/215
		400dpi	4207/111	3887/431
	SCAN mode	200dpi	2018/130	1584/564
		400dpi	4037/261	3169/1129

Table 3 Original sheet reading widths according to the original sheet widths for the sensor widths

Sensor width Original sheet width	Resolution	B4	A4
B4	200dpi	2102/54	——
	400dpi	4206/110	
A4	200dpi	2102/54	1942/214
	400dpi	4206/110	3886/430

When original sheets narrower than the sensor width, cut out the original sheet width with the registers 11 to 14. (OFFSET, OUTLENGTH): (Region designation function)



(3) Image processing function

The M66335 converts image signals input from the image sensor into binary data. This includes the simple conversion of characters and the change of images with various densities into pseudo-halftone.

Before the conversion, distortions and characteristic degradations which signals from the image sensor almost always have must be corrected or compensated.

Image zone separation must also be performed to realize optimal conversion-to-binary of the image for the possible shortest transmission time.

Functions required for image processing are as follows.

- Peak value detection
- Uniformity correction
- Resolution change (enlargement, reduction and averaging)
- MTF compensation
- γ correction
- Background/character level detection (simple conversion to binary)
- Change to pseudo-halftone
  - Organized dither
  - Error diffusion
- Image zone separation
- Designation of regions

` Peak value detection

Because the A/D converter of the M66335 uses the input dynamic range at 2 Vp-p, the reference voltages (V_{WL}, V_{BL}) corresponding to the peak value are fixed. The peak value of analog signals output from the analog processing circuit must be detected before those signals are input to the A/D converter in order to adjust the analog signal peak value to the full-scale value of the converter.

The peak value detection is performed by reading white data from the sensor in the AGC mode selected from its three modes (AGC, UNIF and SCAN) of the M66335.

As shown in Fig. 4, preprocessing of peak value detection to increase the gain at the gain control is performed for a 8 line cycle and gain control processing to decrease the gain when the A/D converter overflows is performed for another 8 line cycle after the start command (register 00: AGC) in the AGC mode.

As a result, the gain changes as shown in Fig. 5.

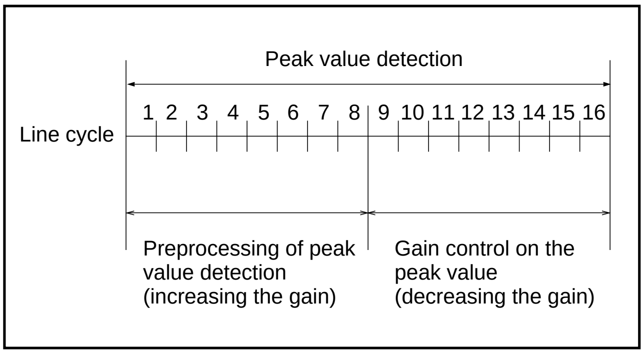


Fig. 4 Peak value detection

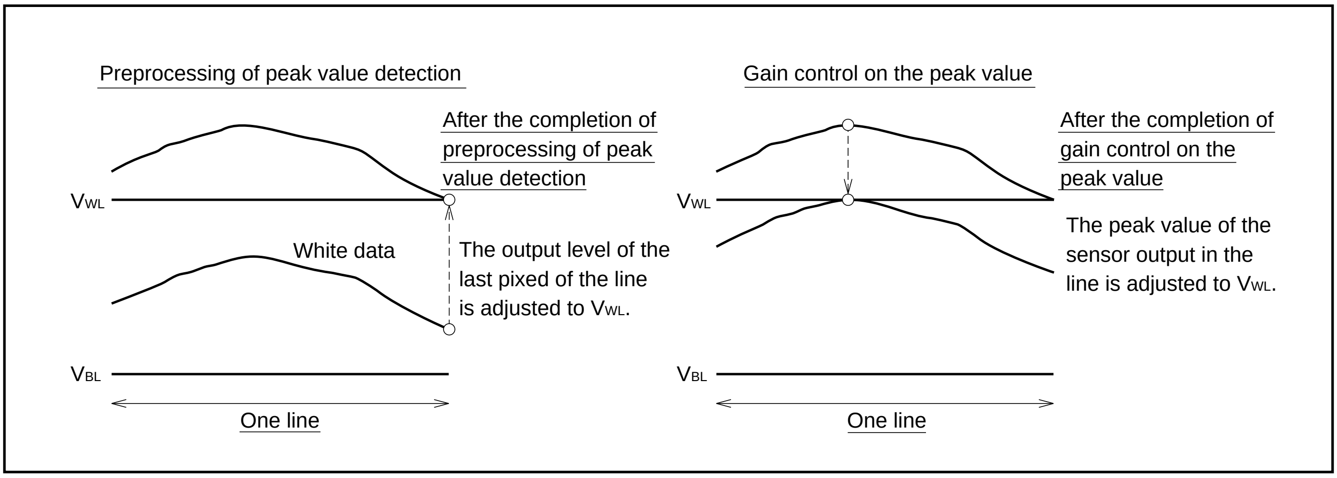


Fig. 5 Changes of the gain in peak value detection

` Uniformity correction

Uniformity correction is to correct shading distortion due to less light at each end of the light source and faded light around the lens, or high frequency distortion due to characteristic variations pixel by pixel in the image sensor.

As shown in Fig. 7, the M66335 makes blocks each of two pixels, creates a set of uniformity correction data for each block, and write them to the built-in correction memory (SRAM: 1024 word × 6 bits) in the UNIF mode selected from its three modes (AGC, UNIF and SCAN).

The correction data created each for two pixels are read from the built-in correction memory to correct the input image data consecutively in the SCAN mode. With the register 01 (UNIFS) set at “1”, the uniformity is not implemented.

With the register 02 (RES) set at “1”, uniformity correction is performed on a block for 4 pixels.

For uniformity correction, white correction or the combination of black correction and white correction can be selected according to the types of image sensors as shown in Table 4.

This is set in the register 00 (SENS, UMODE) and register 01 (UNIFM).

To perform both black correction and white correction, the black correction must be done first.

The M66335 implements the correction in the correction range of 50% as shown in Fig. 7. If a set of white correction data is beyond the correction range of 50%, the correction are not exactly performed as shown in Fig. 7. Therefore, ensure that input signals are within the range.

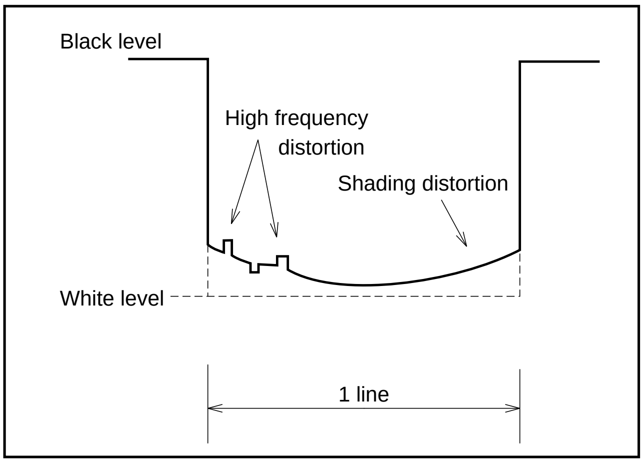


Fig. 6 Waveform of white data output from the image sensor

Table 4 Uniformity correction due to the image sensor

Image sensor	Correction	Register		
		Type of the sensor Register 00 (SENS)	Creation of uniformity correction data Register 00 (UMODE)	Selection of correction mode Register 01 (UNIFM)
CCD	White correction	0	1	0
CIS	White correction	1	1	0
	Black correction White correction	1	Period of black correction : 0 Period of white correction : 1	1

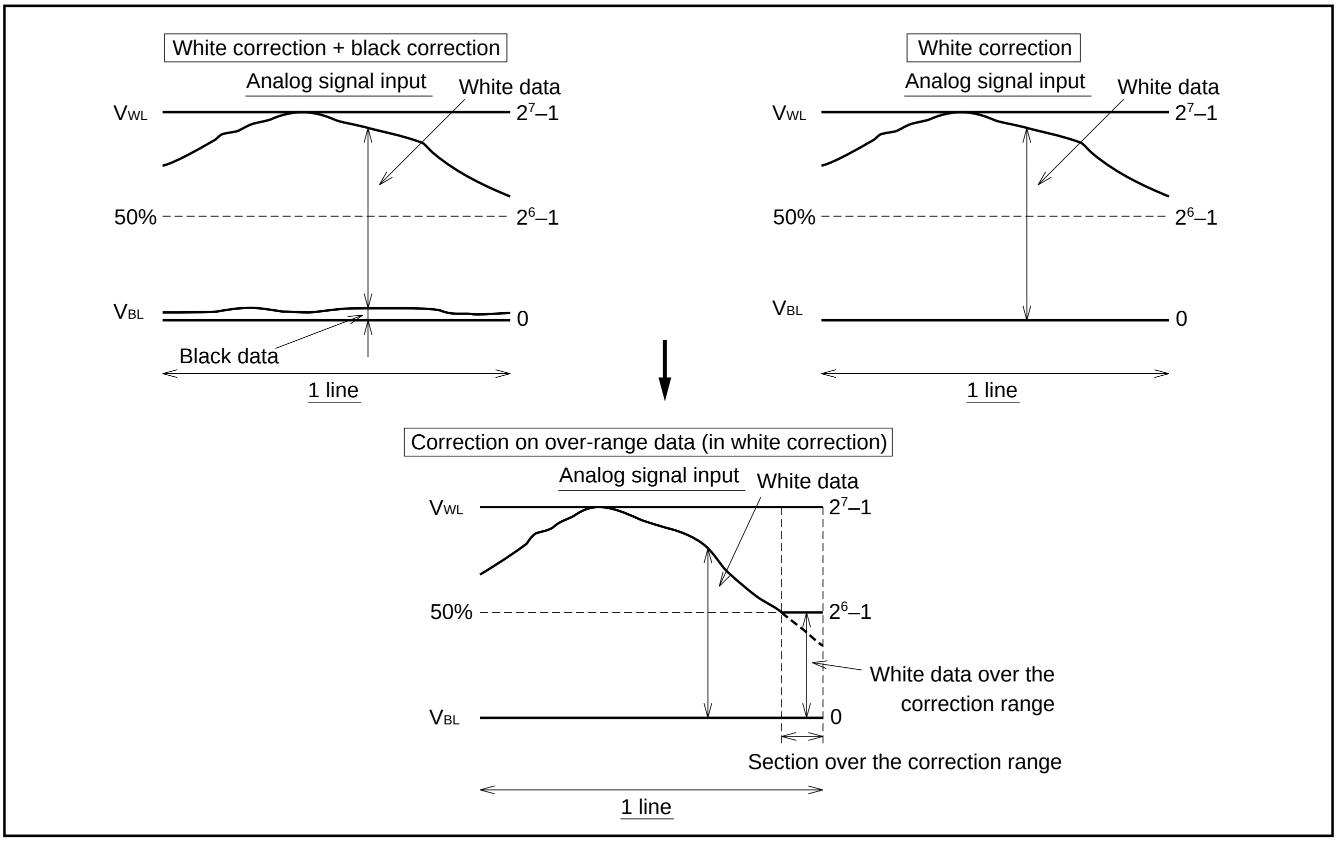


Fig. 7 Uniformity correction

● Resolution change

Resolution change is controlled through H/W in the horizontal scanning direction and through S/W in the vertical scanning direction. The sequence for resolution change is shown in Fig. 8.

` Horizontal scanning direction

The scaling factor is written from the register 15 (CNV_D) to the built-in resolution change memory (100W × 1 bit) bit by bit by 100 operations.
MSSEL of the register 6 must be set at “0” (which specifies the horizontal scanning direction) before the scaling factor is written in the memory.
The procedure to specify CNV_D is as follows.

◆ In the case of reduction

Data written in the resolution change memory have the following meaning.
“0”: 1 pixel is output.
“1”: No pixel is output.
(Example of reduction to 75%)
75 0’s and 25 1’s are written in the memory. The intervals of 1’s should be as equal as possible to obtain the image with better quality.

◆ In the case of enlargement

Data written in the resolution change memory have the following meaning.
“0”: 1 pixel is output.
“1”: 2 pixels are output.
(Example of enlargement to 150%)
50 0’s and 50 1’s are written in the memory. The intervals of 1’s should be as equal as possible to obtain the image with better quality as in the reduction.

` Vertical scanning direction

Processing of lines to implement the scaling factor in the vertical scanning direction is decided for each line through the register.
MSSEL of the register 6 must be set at “1” (which specifies the vertical scanning direction), and either “0” or “1” written in the register 15 (CNV_D) before the processing of each line.
The timing for this setting is in the period between the first transition of the INT signal (synchronized with that of ACCK) and that of the SH signal (the start of taking the SRDY signal in).
The procedure to specify CNV_D is as follows.

◆ In the case of reduction

CNV_D indicates the current line read.
“0”: 1 line of data are output.
“1”: No line of data are output.

◆ In the case of enlargement

CNV_D indicates the next line read.
“0”: 1 line of data are output with PTIM generated (paper driven).
“1”: 1 line of data are output with PTIM generated (paper not driven).
(Paper not driven: the same line is read again.)

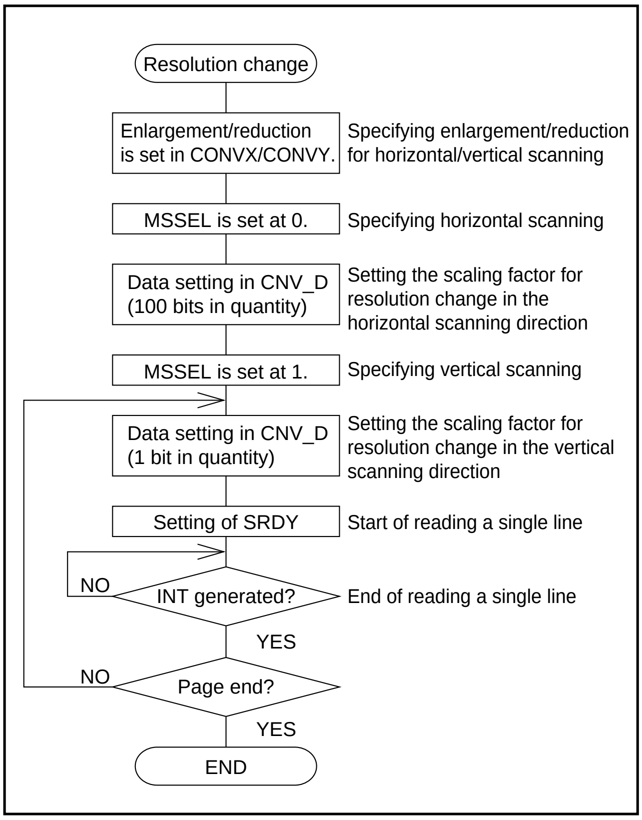
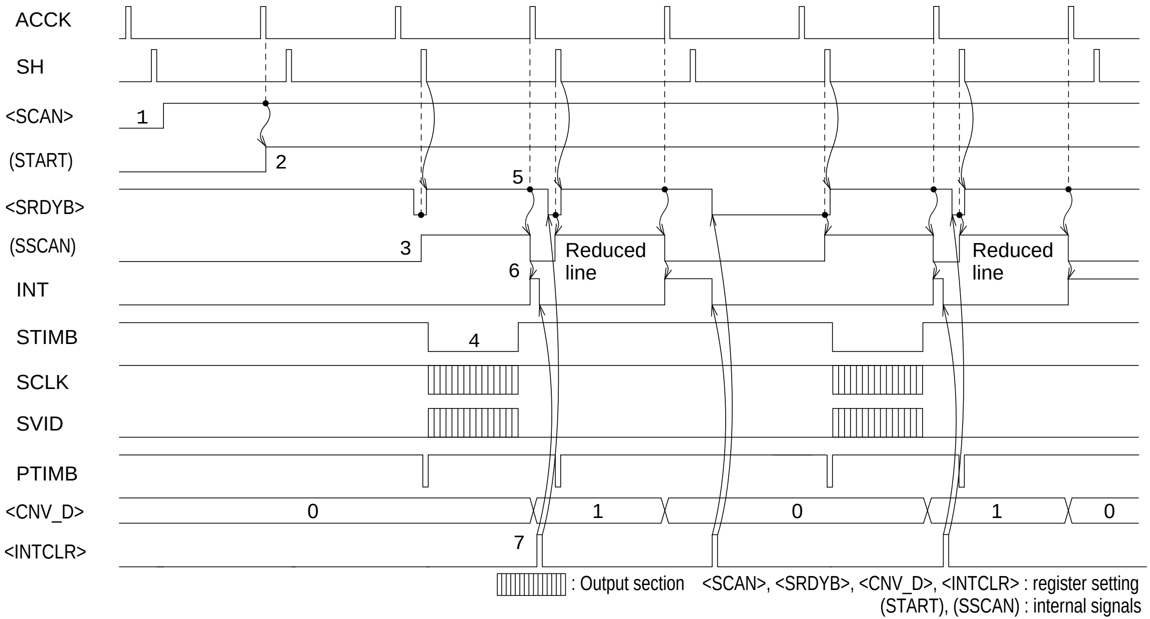


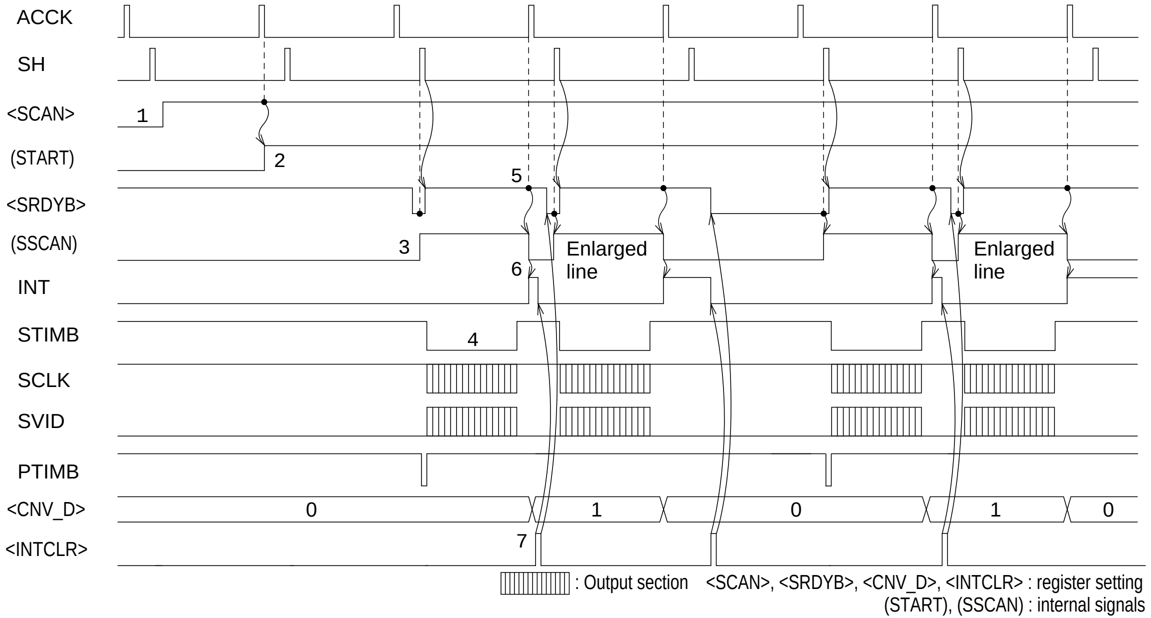
Fig. 8 Sequence of resolution change setting

Use the PTIMB signal as control signals for the pulse motor for the reading roller. The sequence for reduction is shown in Fig. 9 and that for enlargement in Fig. 10.



1 At the initial setting, the enlargement/reduction setting (CNV_D) in horizontal scanning is implemented. Then, after the system is switched into the setting mode for enlargement/reduction in vertical scanning, the first line is set.
2 With a ↓ flow of ACCK, the SCAN command is taken in, when the system comes into the standby mode for SRDYB. (START: ‘H’)
3 With a ↑ flow of SH, SRDYB: ‘L’ is taken in, when scanning starts and PTIMB is output. (SSCAN: ‘H’)
4 During the period that STIMB is at ‘L’, converted binary data are output while the data for reduced lines are not output because STIMB for them are at ‘H’.
5 With a ↑ flow of ACCK, SRDYB: ‘H’ is taken in, when the reading of the single line is completed. (SSCAN: ‘L’)
6 With a ↓ flow of SSCAN, INT is asserted. (INT: ‘H’)
7 With CPU ready for reading the next line, the enlargement/reduction setting (CNV_D) in vertical scanning is implemented; INTCLR is generated; INT is negated; and then SRDYB is set at ‘L’.

Fig. 9 Reduction processing sequence

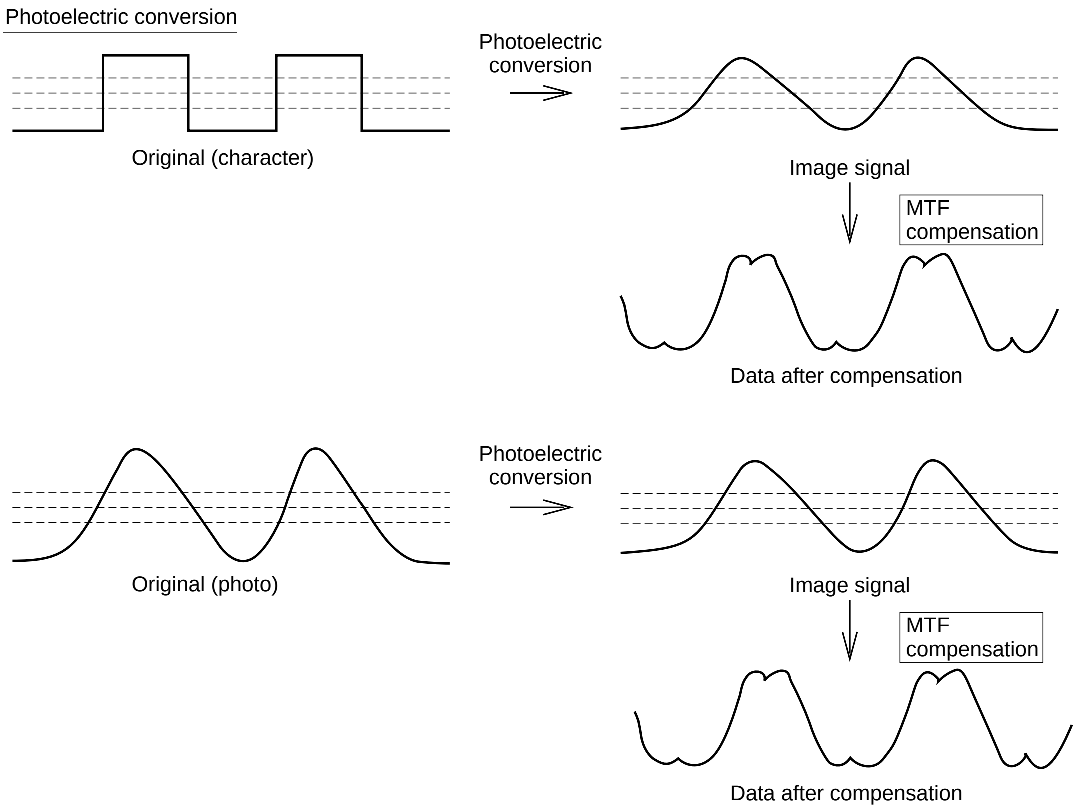


1 At the initial setting, the enlargement/reduction setting (CNV_D) in horizontal scanning is implemented. Then, after the system is switched into the setting mode for enlargement/reduction in vertical scanning, the first line is set.
2 With a ↓ flow of ACCK, the SCAN command is taken in, when the system comes into the standby mode for SRDYB. (START: ‘H’)
3 With a ↓ flow of SH, SRDYB: ‘L’ is taken in, when scanning starts and PTIMB is output while it is not output for enlarged lines. (SSCAN: ‘H’)
4 During the period that STIMB is at ‘L’, converted binary data are output.
5 With a ↑ flow of ACCK, SRDYB: ‘H’ is taken in, when the reading of the single line is completed. (SSCAN: ‘L’)
6 With a ↓ flow of SSCAN, INT is asserted. (INT: ‘H’)
7 With CPU ready for reading the next line, the enlargement/reduction setting (CNV_D) in vertical scanning is implemented; INTCLR is generated; INT is negated; and then SRDYB is set at ‘L’.

Fig. 10 Enlargement processing sequence

` MTF compensation

As shown in Fig. 11, image data of characters or pictures photoelectrically converted by the sensor unit show degradation in resolution. MTF compensation function of the M66335 restores the resolution of those data and expands the apparent dynamic range by strengthening the high-pass frequency constituent with the Laplacian filter.



Resolution compensation

$X' = X + \alpha ((X - A) + (X - B) + (X - C) + (X - D))$

where, α : MTF compensation coefficient in the register 08 (MTF_C, MTF_I)

In the above equation, α is set according to the register 07 : MODE (selection of conversion-into-binary mode) as follows:

MODE : 00 (simple binary)	α = MTF_C	
MODE : 01 (organized dither)	α = MTF_I	
MODE : 10 (image zone separation)	separation (character)	α = MTF_C for image zone
	separation (photo)	α = MTF_I for image zone
MODE : 11 (error diffusion)	α = MTF_I	

Fig. 11 MTF compensation

` γ correction

γ correction according to the sensitivity characteristics (logarithmic characteristics) of human eyes is implemented to approximate the image data to natural images.

To do this, the M66335 writes the γ correction table to the built-in SRAM and read the corrected values corresponding to read image data values from the SRAM.

$\gamma = 0.45$ is considered to be the optimal for γ correction for thermal head printers. Fig. 12 shows a characteristics example at $\gamma = 0.45$.

γ correction processing is set through the register 06 : GAMMA as follows.

GAMMA : 00 $\gamma = 1$
GAMMA : 01 γ = conversion table value
GAMMA : 10 γ = 1 for image zone separation (character)
γ = conversion table value for image zone separation (photo)
GAMMA : 11 γ = conversion table value for image zone separation (character)
γ = 1 for image zone separation (photo)

For the procedures of inputting/outputting of data, refer to the section on writing to/reading from the γ correction memory.

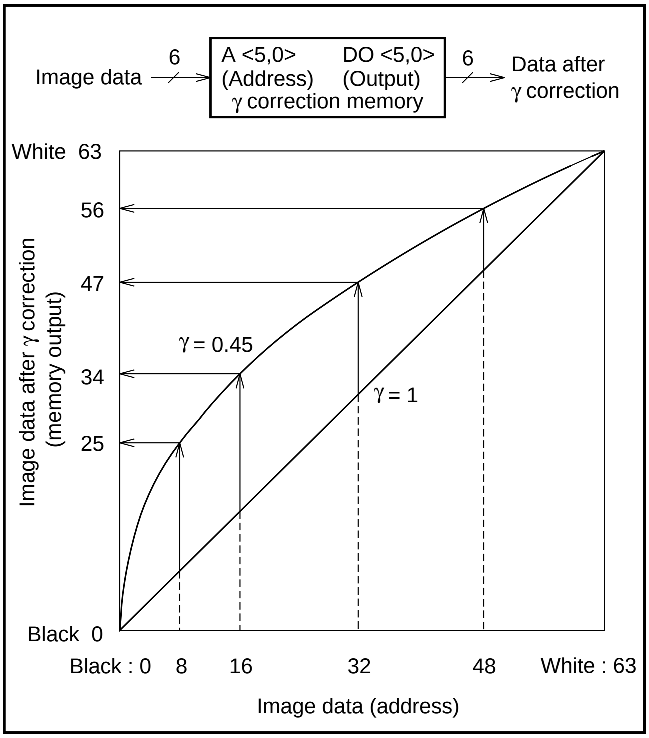
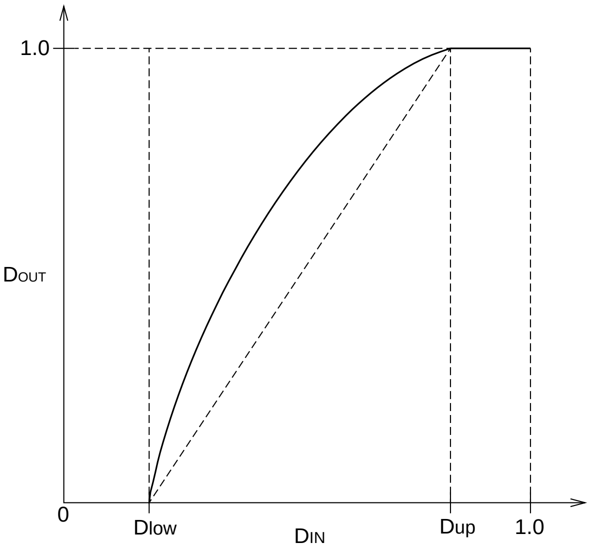


Fig. 12 γ correction by means of the conversion table



IF($D_{IN} < D_{low}$)
$D_{OUT} = 0$

IF($D_{low} \le D_{IN} < D_{up}$)

$$D_{OUT} = \left(\frac{D_{IN}-D_{low}}{D_{up}-D_{low}}\right)^{\gamma}$$

IF($D_{up} \le D_{IN}$)
$D_{OUT} = 1.0$

` Background/character level detection

The M66335 uses not the fixed threshold system but the floating threshold system, where the optimal threshold for simple conversion-to-binary of objective pixels are continually generated by constantly detecting background/character levels.

Accordingly, the threshold value proper for image data is generated without processing the data.

The threshold value is used for the areas to be converted to binary when simple conversion-to-binary or image zone separation is selected as the mode of conversion to binary in reading data.

: register 07 (MODE)

Background level counter

When image data greater (lighter in light) than the current value are input, this counter counts up to approximate to the data.

When image data smaller (darker in light) than the current value are input, this counter counts down to approximate to the data.

Setting of the rate of count-up/count-down following data input

: register 0C (MAX_UP, MAX_DOWN)

Setting of the lowest limit for background levels

: register 0E (LL_MAX)

Character level counter

When image data greater (lighter in light) than the current value are input, this counter counts up to approximate to the data.

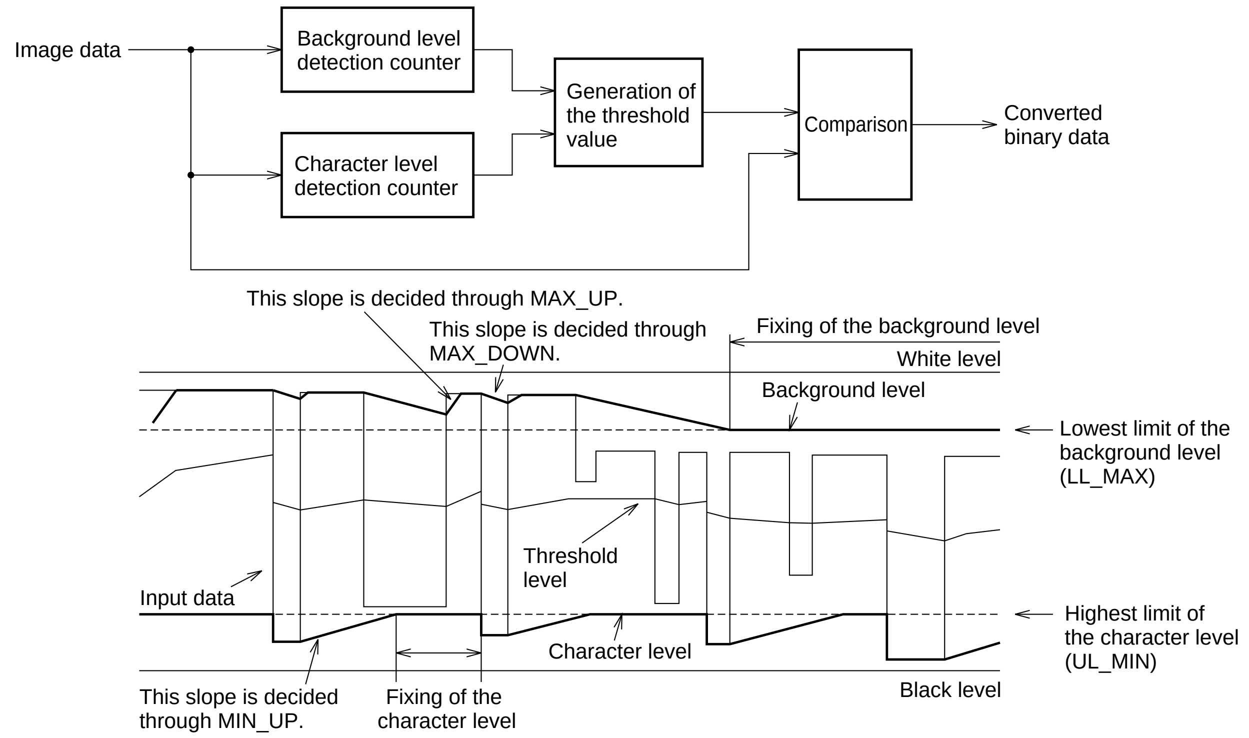
When image data smaller (darker in light) than the current value are input, this counter counts down to approximate to the data.

Setting of the rate of count-down following data input

: register 0C (MIN_UP)

Setting of the highest limit for character levels

: register 0D (UL_MIN)



Threshold level = (background level point – character level) × K + character level

K = threshold factor for conversion to binary: register 07 (SLICE)

Lowest limit of the background level (LL_MAX) > highest limit of the character level (UL_MIN)

Fig. 13 Background/character levels

` Error diffusion

The error diffusion, which is a conditional determination method, locally diffuses density errors between the original image and the result to obtain the best approximation. This generates images with good compatibility of gradation and resolution.

This is operated by selecting the error diffusion in conversion-into-binary mode selection.

: register 07 (MODE)

In error diffusion, dithers as well as density errors are added to image data. The dithers are data as commonly used for the dither matrix.

: register 08 (ERROR)

γ correction must be performed in the error diffusion.

- Organized dither

The M66335 has built-in SRAM with a configuration of 64 words × 6 bits for organized dither memory.

In the initial setting, write the threshold value proper for the preferred dither pattern to the dither memory after setting the dither matrix size.

: register 07 (DITH)

: register 10 (DITH_D)

An example of dither patterns is shown in Fig. xx.

For the procedure of inputting/outputting data, refer to the section on writing to/reading from the dither memory.

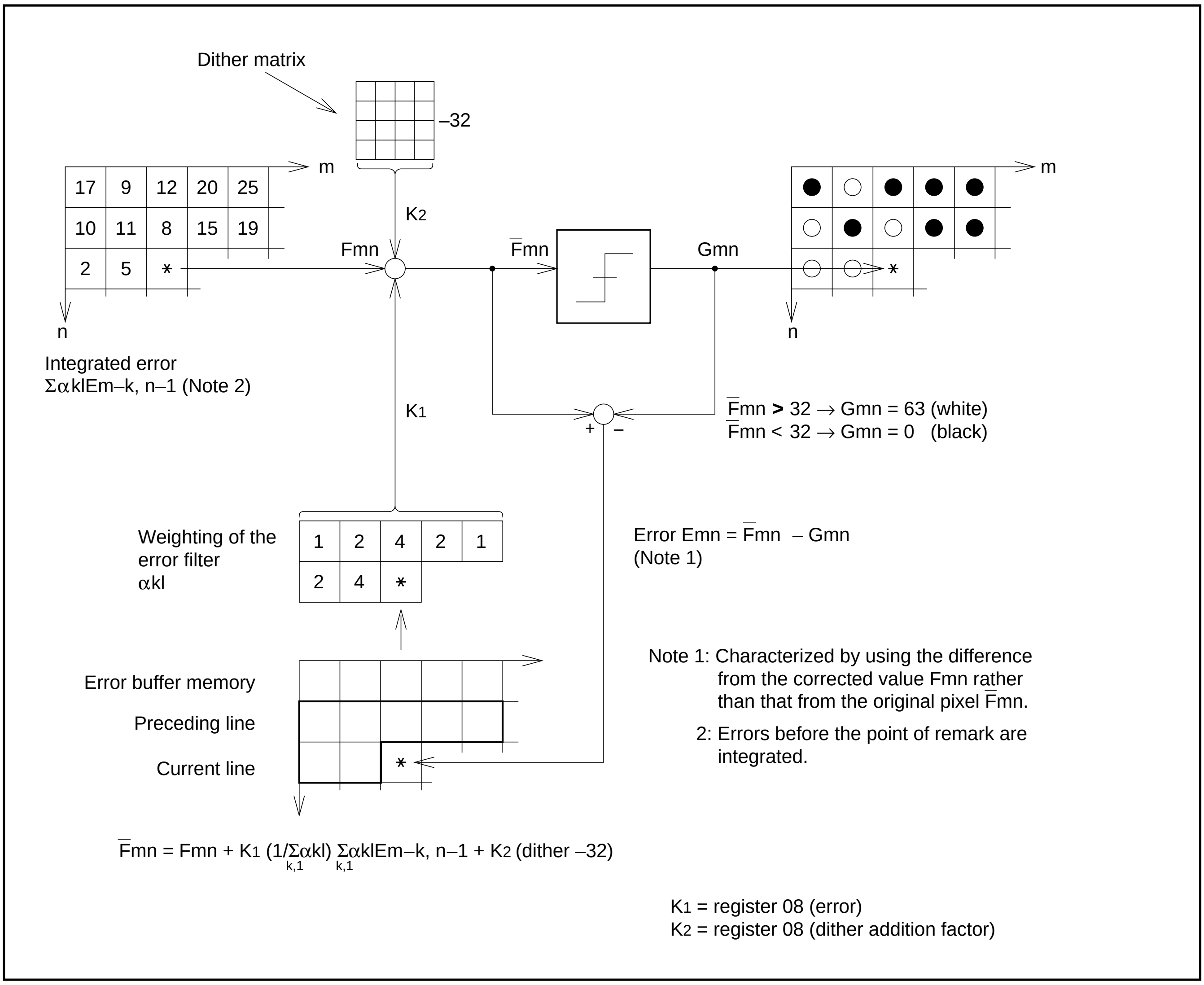


Fig. 14 Error diffusion method

` Image zone separation

To make data conversion fit for each image zone, a black and white image is separated into the zones to be converted to binary and the gradation zones. The binary zone is processed through simple conversion to binary and the gradation zone through the error diffusion.

: register 08 to 0E

In the black and white image, each window of the gradation zone (photo) does not have a large difference of luminance in it.
With this characteristic of the gradation zone, it is distinguished from the conversion-into-binary zone through the following method.

L_{max}: maximum illumination in window
L_{min} : minimum illumination in window

Determining inequality 1: $L_{max} - L_{min} > A$ (because the zone to be converted to binary has a large difference in luminance in it.): register 09 Difference (SEPA_A)
Determining inequality 2: $L_{min} > B$ (for the wholly white area): register 0A Minimum (SEPA_B)
Determining inequality 3: $L_{max} < C$ (for the wholly black area): register 0B Maximum (SEPA_C)

If the window satisfies determination inequalities 1, 2 or 3, simple conversion to binary is applied.
If the window does not satisfy any of determination inequalities 1, 2 and 3, change to pseudo-halftone is applied.

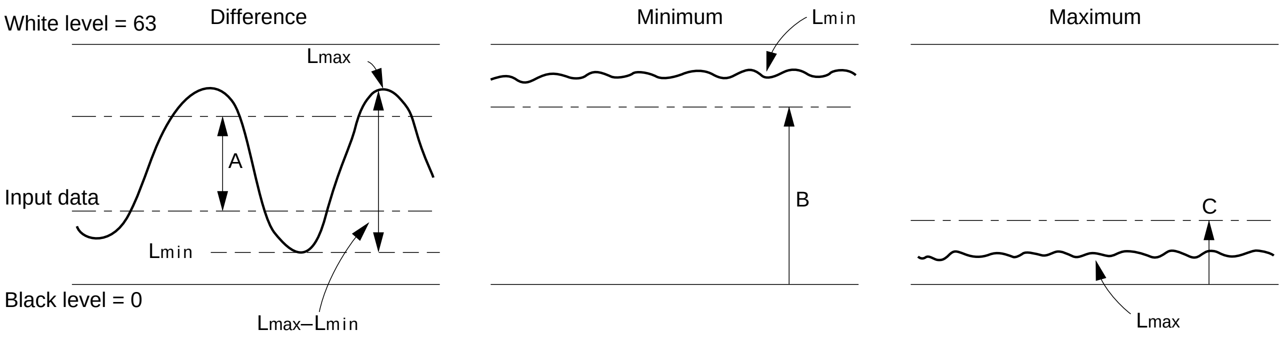


Fig. 15 Image zone separation

` Region designation function

The sensor width is fixed for A4 and B4.

The region designation function is to output only the data for a region defined and designated in terms of output data after resolution change (or after uniformity correction for multivalued data).

Registers 11 to 14 (OFFSET, OUTLENGTH)

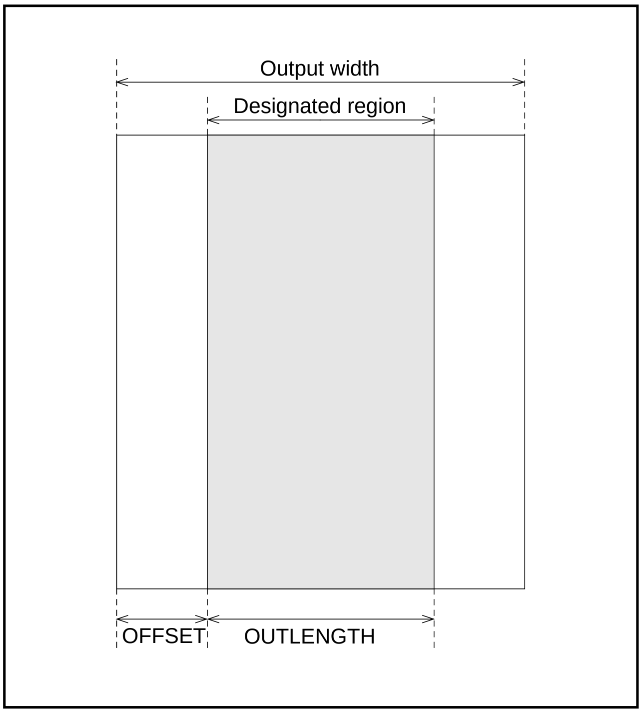
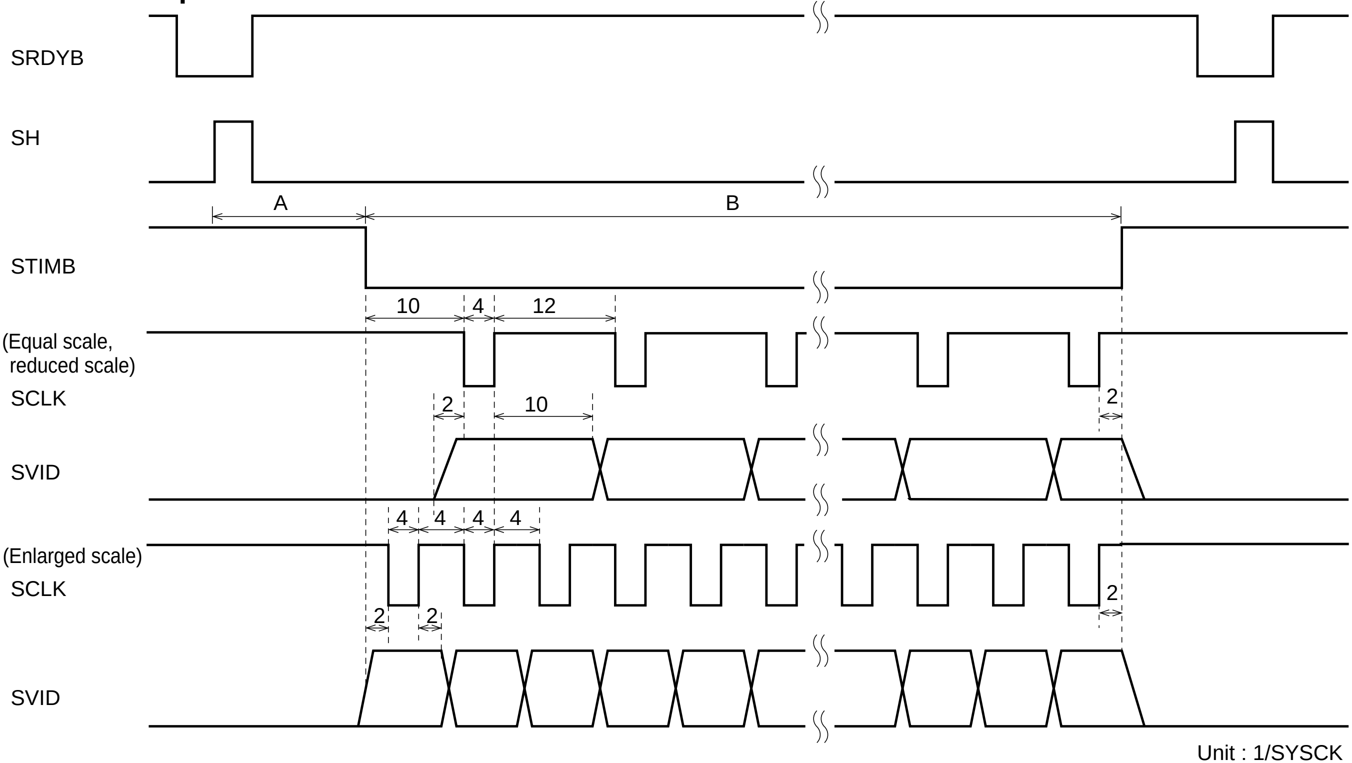


Fig. 16 Cut-out function

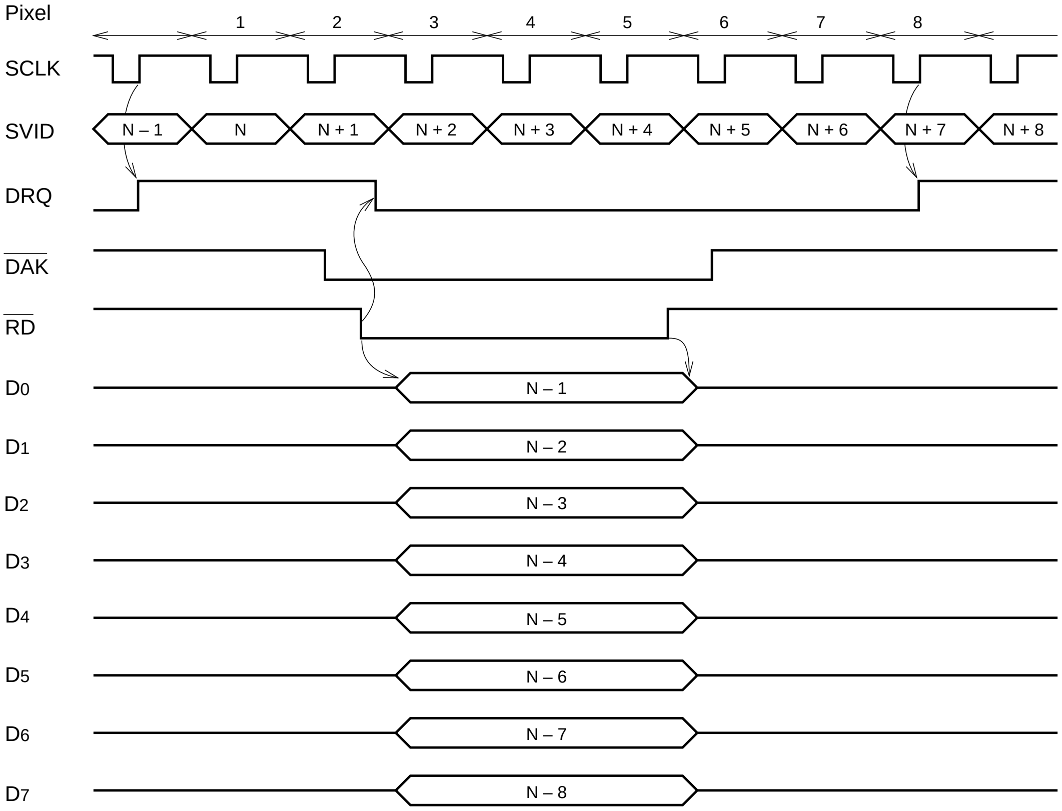
(4) CODEC interface (Binary data output)

Serial output



Note: A is decided through the registers 05 (ST_PL) 11 and 12 (OFFSET), and B through the registers 13 and 14 (OUTLENGTH).

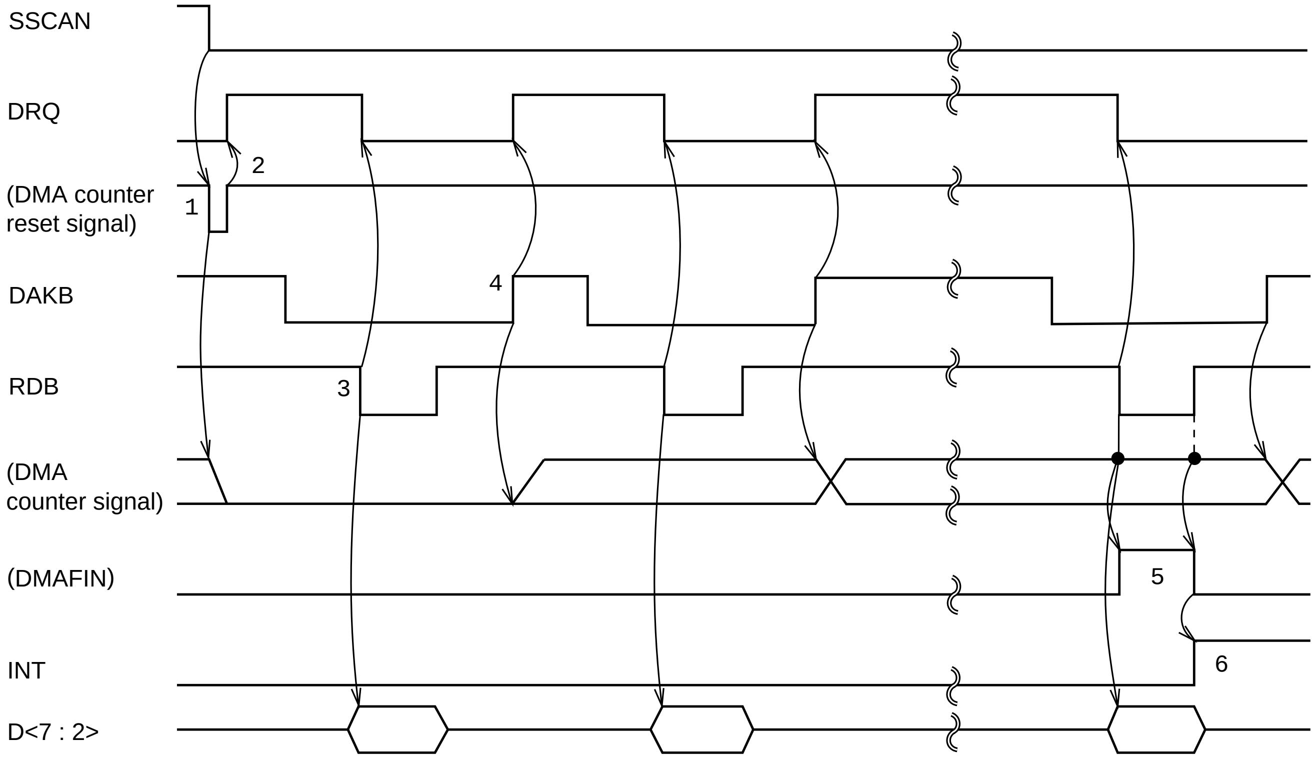
Parallel output



Note: The 3-line handshake of $\overline{\text{SRDY}}$, SH and $\overline{\text{STIM}}$, which is the interface with CODEC, is the same as serial output.

(5) DMA interface (multivalued output)

The DMA transfer of data after non-uniformity correction can be performed by setting P_O) of the register 01: at “1” (existence of DMA output) and M_B of that register at “1” (multivalue). With this setting, neither enlargement, nor reduction, nor 400 dpi of resolution can be set.



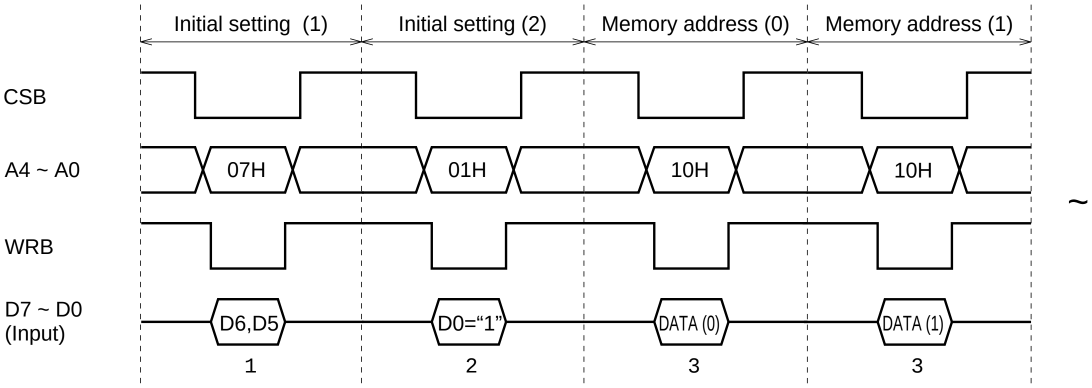
(XXXX): internal signal

1 On completion of reading one line, with a ↓ flow of SSCAN, the reset signal is entered in the DMA counter.
2 With a ↑ flow of the reset signal, DRQ shifts to ‘H’, when the DMA transfer becomes ready.
3 With DAKB at ‘L’ and a ↓ flow of RDB, DRQ shifts to ‘L’, when multivalued data are output to D <7 : 2> during the period that RDB is at ‘L’.
4 With a ↑ flow of DAKB, the DMA counter counts up and DRQ shifts to ‘H’, when the DMA transfer becomes ready again.
5 The cycle of the above 3 and 4 is repeated until the DMA counter counts up to reach the number of output pixels set in the registers 13 and 14 OUTLENGTH subtracted by one. By that repetitive operation, DMAFIN shifts to ‘H’ to terminate the DMA transfer when it reaches the set number.
6 With a ↓ flow of DMAFIN, INT shifts to ‘H’, when CPU has an interrupt.
7 Reading is resumed from the next line by negating the INT signal through the register 17 (INTCLR).

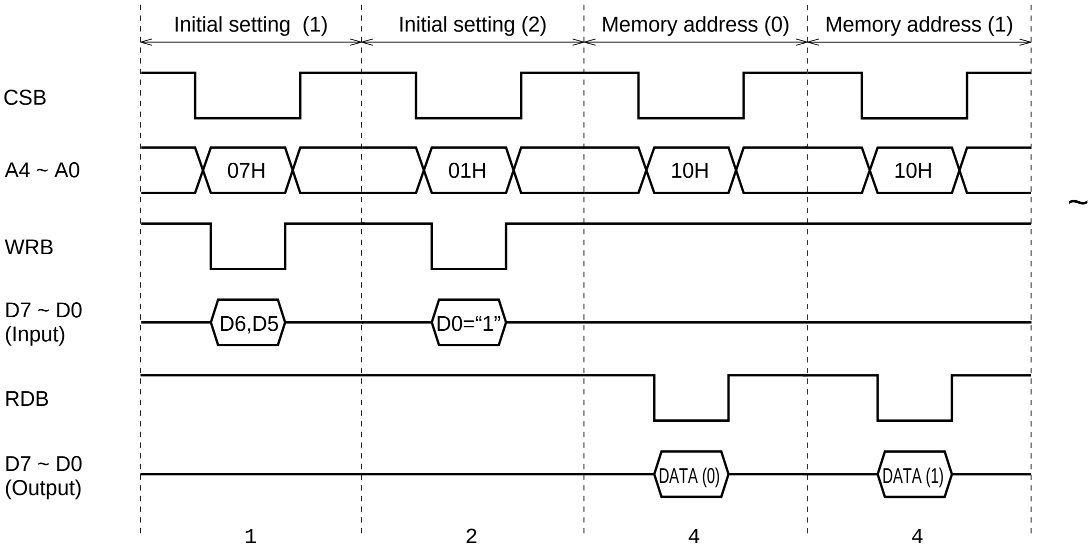
(6) Writing to/reading from the dither memory, γ correction memory, uniformity correction memory, and resolution change memory

The sequences of writing a dither pattern to and reading it from SRAM with a configuration of 64 words × 6 bits which is built in the M66335 for organized dither are shown below.

Writing to the dither memory (MPU → M66335)



Reading from the dither memory (M66335 → MPU)



1 D6 and D5 (DITH) of the register 07 are set to define the dither matrix size.
2 D0 (CNTRST) of the register 01 is set at "1" to reset the address counter of the dither memory.
3 DITH_D is selected in the register 10, and DATA (0) of the MPU bus (D5 to D0) is written in the memory. The address counter of the dither memory is incremented at the edge of the first transition of $\overline{\text{WR}}$. (For writing)
4 DITH_D is selected in the register 10, and DATA (0) of the dither memory is read into the MPU bus (D5 to D0). The address counter of the dither memory is incremented at the edge of the first transition of $\overline{\text{RD}}$. (For reading)

Dither matrix addresses

A0	A1	A2	A3
A4	A5	A6	A7
A8	A9	A10	A11
A12	A13	A14	A15

4 × 4 matrix

A0	A1	A2	A3
A4	A5	A6	A7
A8	A9	A10	A11
A12	A13	A14	A15
A16	A17	A18	A19
A20	A21	A22	A23
A24	A25	A26	A27
A28	A29	A30	A31

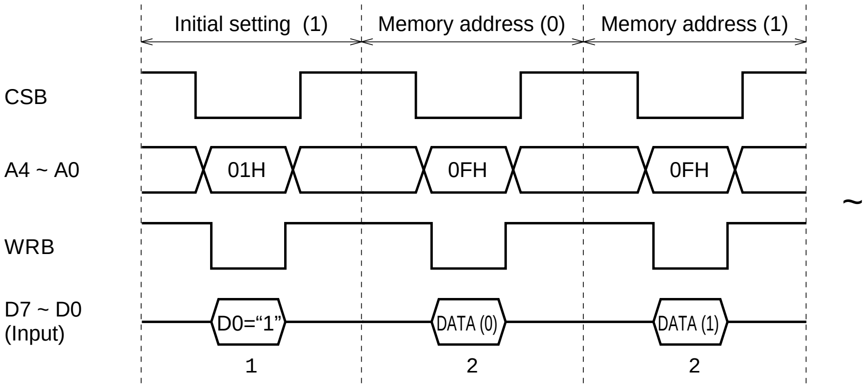
4 × 8 matrix

A0	A1	A2	A3	A4	A5	A6	A7
A8	A9	A10	A11	A12	A13	A14	A15
A16	A17	A18	A19	A20	A21	A22	A23
A24	A25	A26	A27	A28	A29	A33	A31
A32	A33	A34	A35	A36	A37	A38	A39
A40	A41	A42	A43	A44	A45	A46	A47
A48	A49	A50	A51	A52	A53	A54	A55
A56	A57	A58	A59	A60	A61	A62	A63

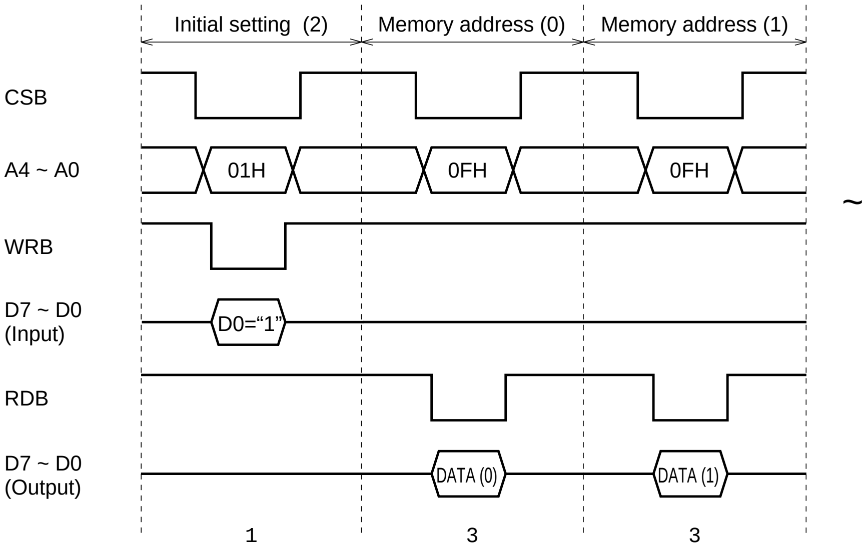
8 × 8 matrix

The sequences of writing γ correction table to and reading it from SRAM with a configuration of 64 words × 6 bits which is built in the M66335 for γ correction are shown below.

Writing to the γ correction memory (MPU → M66335)



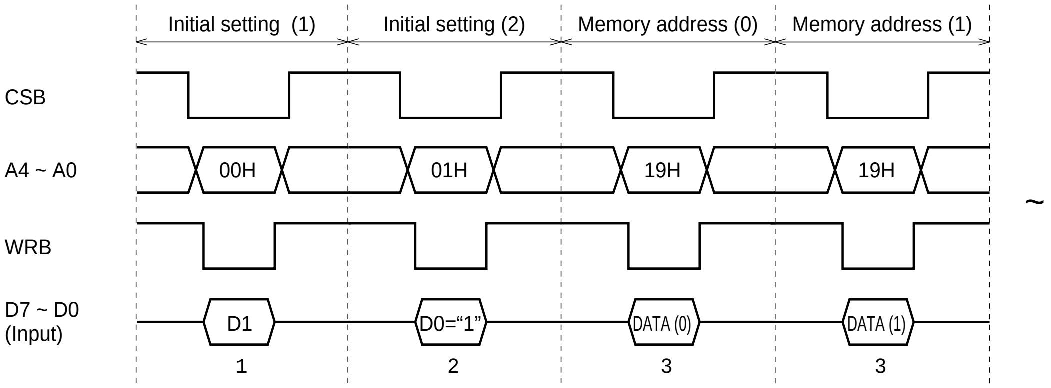
Reading from the γ correction memory (M66335 → MPU)



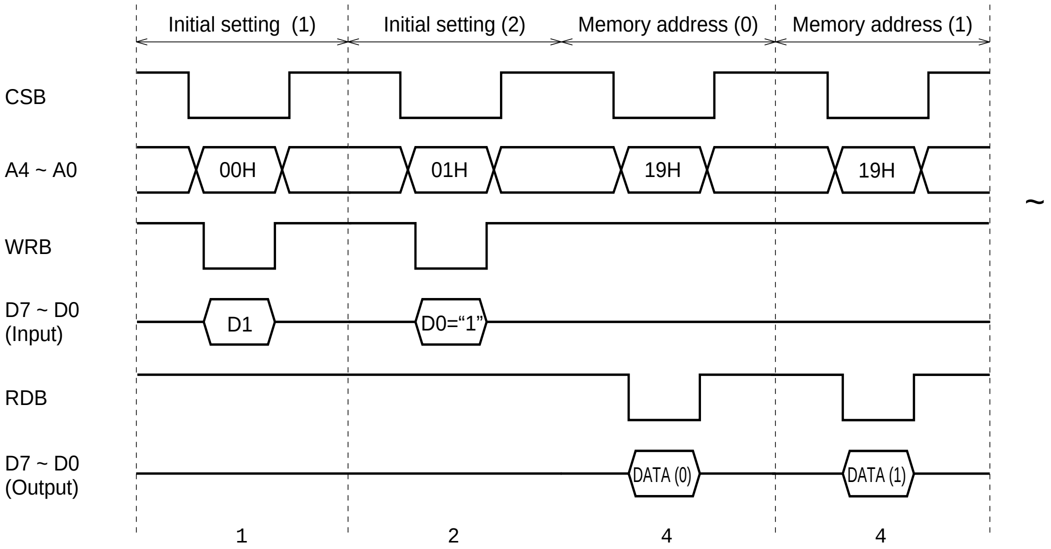
1 D0 (CNTRST) of the register 01 is set at “1” to reset the address counter of the γ correction memory.
2 GAMMA_D is selected in the register 0F, and DATA (0) of the MPU bus (D5 to D0) is written in the memory. The address counter of the γ correction memory is incremented at the edge of the first transition of WRB. (For writing)
3 GAMMA_D is selected in the register 0F, and DATA (0) of the γ correction memory is read into the MPU bus (D5 to D0). The address counter of the γ correction memory is incremented at the edge of the first transition of RDB. (For reading)

Uniformity correction data can be written to and read from SRAM for uniformity correction built in the M66335 through the MPU bus. With this operation, the uniformity data can be temporarily saved in the backup memory when the power is off. The sequences of writing and reading uniformity correction data are shown below.

Writing to the uniformity correction memory (MPU → M66335)



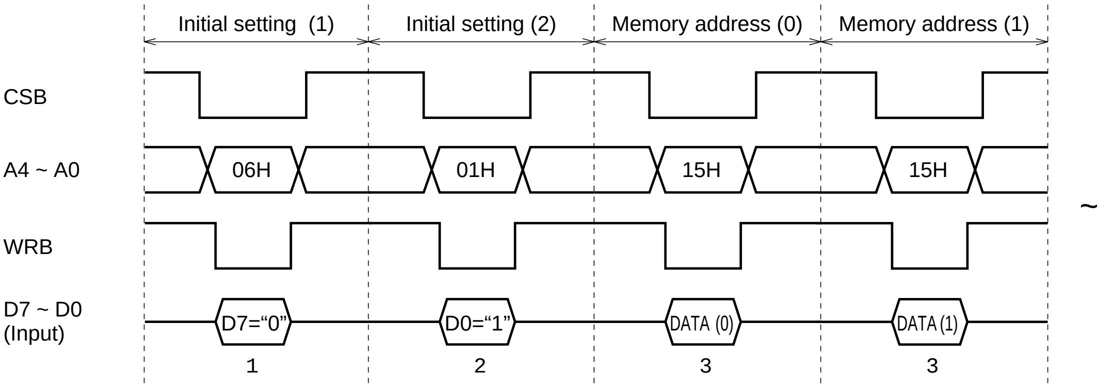
Reading from the uniformity correction memory (M66335 → MPU)



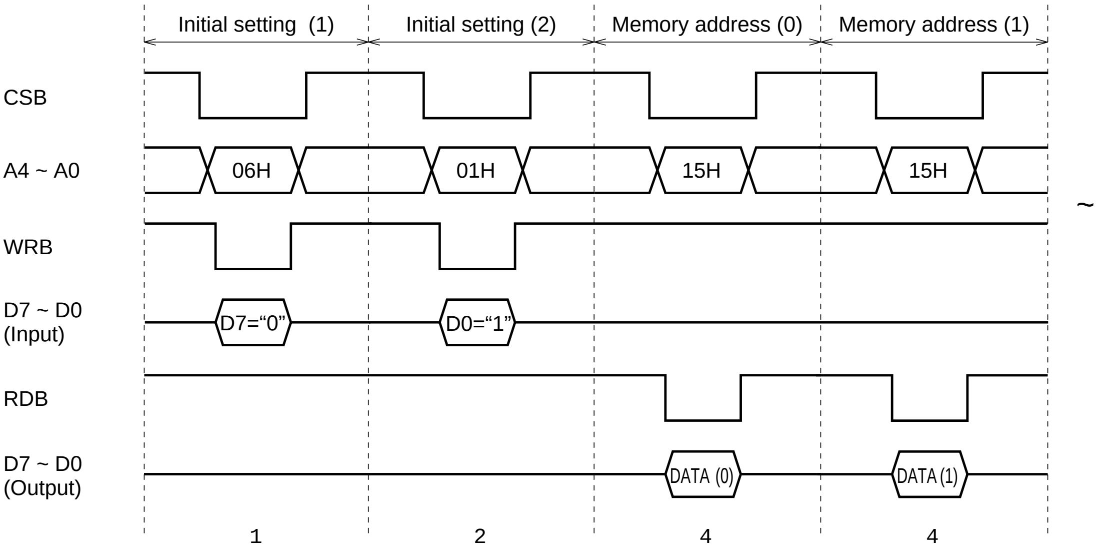
1 "0" (black correction) or "1" (white correction) is set in D1 (Umode) of the register 00.
2 D0 (CNTRST) of the register 01 is set at "1" to reset the address counter of the uniformity correction memory.
3 UNIF_D is selected in the register 19, and DATA (0) of the MPU bus (D5 to D0) is written in the memory. The address counter of the uniformity correction memory is incremented at the edge of the first transition of WRB. (For writing)
4 UNIF_D is selected in the register 19, and DATA (0) of the uniformity correction memory is read into the MPU bus (D5 to D0). The address counter of the uniformity correction memory is incremented at the edge of the first transition of RDB. (For reading)

The sequences of writing a resolution change table to and reading it from SRAM with a configuration of 100 words × 1 bit which is built in the M66335 for resolution change are shown below.

Writing to the resolution change memory (MPU → M66335)



Reading from the resolution change memory (M66335 → MPU)



1 "0" (horizontal scan) is set in D7 (MSSEL) of the register 06.
2 D0 (CNTRST) of the register 01 is set at "1" to reset the address counter of the resolution change memory.
3 CNV_D is selected in the register 15, and DATA (0) of the MPU bus (D0) is written in the memory. The address counter of the resolution change memory is incremented at the edge of the first transition of WRB. (For writing)
4 CNV_D is selected in the register 15, and DATA (0) of the resolution change memory is read into the MPU bus (D0). The address counter of the resolution change memory is incremented at the edge of the first transition of RDB. (For reading)

List of the M66335FP registers

R/W	A4 ~ A0	Default	D7	D6	D5	D4	D3	D2	D1	D0
R/W	00H	00H	RESET	SENS	SENS_W	AGC	UNIF	SCAN	UMODE	“L”
R/W	01H	00H	SOURCE	S/H_W	SH_W	UNIFS	P_O	M_B	UNIFM	CNTRST
W	02H	00H	RES	LCMPS	BLS	BLCMPS	CCD	CIS3	CIS2	CIS1
W	03H	00H	PRE_DATA (7 : 0)							
W	04H	00H			PRE_DATA (13 : 8)					
W	05H	00H	ST_PL (7 : 0)							
W	06H	00H	MSSEL	AVE	CONVX <1 : 0>		CONVY <1 : 0>		GAMMA <1 : 0>	
W	07H	00H	POL	DITH <1 : 0>		MODE <1 : 0>		SLICE <2 : 0>		
W	08H	00H			ERROR <1 : 0>		MTF_C <1 : 0>		MTF_I <1 : 0>	
W	09H	00H			SEPA_A (5 : 0)					
W	0AH	00H			SEPA_B (5 : 0)					
W	0BH	00H			SEPA_C (5 : 0)					
W	0CH	00H			MAX_UP <1 : 0>		MAX_DOWN <1 : 0>		MIN_UP <1 : 0>	
W	0DH	1FH			UL_MIN <5 : 0>					
W	0EH	20H			LL_MAX <5 : 0>					
R/W	0FH	—			GAMMA_D (5 : 0)					
R/W	10H	—			DITH_D (5 : 0)					
W	11H	00H	OFFSET <7 : 0>							
W	12H	00H				OFFSET <12 : 8>				
W	13H	00H	OUTLENGTH <7 : 0>							
W	14H	00H				OUTLENGTH <12 : 8>				
W	15H	—								CNV_D
R/W	16H	00H						AGCSTP	SRDYS	SRDYB
W	17H	—	INTCLR							
R/W	18H	00H	GAIN <7 : 0>							
R/W	19H	00H			UNIF_D <5 : 0>					

Register structure

<table>
<tr><th>Address</th><th>R/W</th><th>Description</th></tr>
<tr><td>00H</td><td>R/W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>RESET</td><td>SENS</td><td>SENS_W</td><td>AGC</td><td>UNIF</td><td>SCAN</td><td>UMODE</td><td>“L”</td></tr>
</table>
(Default value: 00H)
<table>
<tr><th>D7</th><th>RESET : system reset</th></tr>
<tr><td>0</td><td>Normal mode</td></tr>
<tr><td>1</td><td>Reset mode</td></tr>
</table>
• With D7 = 1, the system is reset during the period that the write pulse is “L”.
(*) Write only
<table>
<tr><th>D6</th><th>SENS : sensor type</th></tr>
<tr><td>0</td><td>CCD</td></tr>
<tr><td>1</td><td>CIS: (75% of clock duty)</td></tr>
</table>
<table>
<tr><th>D5</th><th>SENS_W : reading width of the sensor</th></tr>
<tr><td>0</td><td>A4</td></tr>
<tr><td>1</td><td>B4</td></tr>
</table>
<table>
<tr><th>D4</th><th>AGC : AGC mode</th></tr>
<tr><td>0</td><td>Stop</td></tr>
<tr><td>1</td><td>Start</td></tr>
</table>
• Controls start/stop of the AGC mode.
<table>
<tr><th>D3</th><th>UNIF : UNIF mode</th></tr>
<tr><td>0</td><td>Stop</td></tr>
<tr><td>1</td><td>Start</td></tr>
</table>
• Controls start/stop of the UNIF mode.
<table>
<tr><th>D2</th><th>SCAN : SCAN mode</th></tr>
<tr><td>0</td><td>Stop</td></tr>
<tr><td>1</td><td>Start</td></tr>
</table>
• Controls start/stop of the SCAN mode.
<table>
<tr><th rowspan="2">D1</th><th colspan="2">UMODE : uniformity correction in the UNIF mode</th></tr>
<tr><th>Black correction + white correction</th><th>Only white correction</th></tr>
<tr><td>0</td><td>Black correction</td><td>—</td></tr>
<tr><td>1</td><td>White correction</td><td>White correction</td></tr>
</table>
</td></tr>
<tr><td>01H</td><td>R/W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>SOURCE</td><td>S/H_W</td><td>SH_W</td><td>UNIFS</td><td>P_O</td><td>M_B</td><td>UNIFM</td><td>CNTRST</td></tr>
</table>
(Default value : 00H)
<table>
<tr><th>D7</th><th>SOURCE : reading width of the original</th></tr>
<tr><td>0</td><td>A4</td></tr>
<tr><td>1</td><td>B4</td></tr>
</table>
<table>
<tr><th>D6</th><th>S/H_W : S/W pulse width</th></tr>
<tr><td>0</td><td>Normal (quadruple the system clock cycle)</td></tr>
<tr><td>1</td><td>Normal multiplied by 0.5</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Address</th><th>R/W</th><th>Description</th></tr>
<tr><td>01H</td><td>R/W</td><td>
<table>
<tr><th>D5</th><th>SH_W : SH pulse width</th></tr>
<tr><td>0</td><td>Normal (16 times the system clock cycle)</td></tr>
<tr><td>1</td><td>Reverse of normal multiplied by 2</td></tr>
</table>
<table>
<tr><th>D4</th><th>UNIFS : uniformity correction</th></tr>
<tr><td>0</td><td>Valid</td></tr>
<tr><td>1</td><td>Invalid</td></tr>
</table>
<table>
<tr><th>D3</th><th>P_O : DMA output</th></tr>
<tr><td>0</td><td>Without DMA output</td></tr>
<tr><td>1</td><td>With DMA output</td></tr>
</table>
D0 is output in the form of LSB and D7 in the form of MSB.
<table>
<tr><th>D2</th><th>M_B : processing mode</th></tr>
<tr><td>0</td><td>Binary</td></tr>
<tr><td>1</td><td>Multivalue</td></tr>
</table>
With the multivalue selected, data (6 bit) after non-uniformity correction can be output through the DMA transfer.
<table>
<tr><th>D1</th><th>UNIF : uniformity correction in SCAN</th></tr>
<tr><td>0</td><td>White correction</td></tr>
<tr><td>1</td><td>Black correction + white correction</td></tr>
</table>
<table>
<tr><th>D0</th><th>CNTRST : address counter reset</th></tr>
<tr><td>0</td><td>Normal mode</td></tr>
<tr><td>1</td><td>Reset mode</td></tr>
</table>
With D0 = 1, the counter is reset during the period that the write pulse is “L”.
All the built-in RAM addresses are reset.
(∗) Write only
</td></tr>
<tr><td>02H</td><td>W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>RES</td><td>LCMPS</td><td>BLS</td><td>BLCMPS</td><td>CCD</td><td>CIS3</td><td>CIS2</td><td>CIS1</td></tr>
</table>
(Default value : 00H)
<table>
<tr><th>D7</th><th>RES : resolution</th></tr>
<tr><td>0</td><td>200dpi</td></tr>
<tr><td>1</td><td>400dpi</td></tr>
</table>
<table>
<tr><th>D6</th><th>LCMPS : line clamping</th></tr>
<tr><td>0</td><td>Invalid</td></tr>
<tr><td>1</td><td>Valid</td></tr>
</table>
<table>
<tr><th>D5</th><th>BLS : bit clamping</th></tr>
<tr><td>0</td><td>Invalid</td></tr>
<tr><td>1</td><td>Valid</td></tr>
</table>
<table>
<tr><th>D4</th><th>BLCMPS : black level line clamping</th></tr>
<tr><td>0</td><td>Invalid</td></tr>
<tr><td>1</td><td>Valid</td></tr>
</table>
<table>
<tr><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Sensors compatible with image sensor interfaces</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>CIS1 : sensors with the input level of 2V or higher</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>CIS2 : sensors with the input level of under 2V</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>CIS3 : sensors capable of line clamping</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>CCD</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Address</th><th>R/W</th><th>Description</th></tr>
<tr><td>03H</td><td>W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td colspan="8">PRE_DATA <7 : 0></td></tr>
</table>
(Default value : 00H)
D7 to D0 : PRE_DATA <7 : 0> the lowest order 8 bits of the single-line cycle counter value
</td></tr>
<tr><td>04H</td><td>W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td></td><td></td><td colspan="6">PRE_DATA <13 : 8></td></tr>
</table>
(Default value : 00H)
D5 to D0 : PRE_DATA <13 : 8> the highest order 6 bits of the single-line cycle counter value
</td></tr>
<tr><td>05H</td><td>W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td colspan="8">ST_PL <7 : 0></td></tr>
</table>
(Default value : 00H)
D7 to D0 : ST_PL <7 : 0> start pulse position to the sensor
• Set ST_PL = (dummy pixels of the sensor + 2).
</td></tr>
<tr><td>06H</td><td>W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>MSSEL</td><td>AVE</td><td colspan="2">CONVX</td><td colspan="2">CONVY</td><td colspan="2">GAMMA</td></tr>
</table>
(Default value : 00H)
<table>
<tr><th>D7</th><th>MSSEL : horizontal and vertical setting</th></tr>
<tr><td>0</td><td>Horizontal</td></tr>
<tr><td>1</td><td>Vertical</td></tr>
</table>
<table>
<tr><th>D6</th><th>AVE : averaging processing</th></tr>
<tr><td>0</td><td>With averaging</td></tr>
<tr><td>1</td><td>Without averaging</td></tr>
</table>
• When “with averaging” selected :
For enlargement : inserted lines are the average of the preceding one and the current one; and
For reduction : the subsequent lines from removed lines are the average of the removed one and the current one.
<table>
<tr><th>D5</th><th>D4</th><th>CONVX : enlargement/reduction mode in the horizontal scanning direction</th></tr>
<tr><td>0</td><td>0</td><td>Original scale</td></tr>
<tr><td>0</td><td>1</td><td>Enlargement</td></tr>
<tr><td>1</td><td>0</td><td>Reduction</td></tr>
<tr><td>1</td><td>1</td><td></td></tr>
</table>
• RES = 1
With the setting of 400dpi, enlargement cannot be set.
<table>
<tr><th>D3</th><th>D2</th><th>CONVY : enlargement/reduction mode in the horizontal scanning direction</th></tr>
<tr><td>0</td><td>0</td><td>Original scale</td></tr>
<tr><td>0</td><td>1</td><td>Enlargement</td></tr>
<tr><td>1</td><td>0</td><td>Reduction</td></tr>
<tr><td>1</td><td>1</td><td></td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Address</th><th>R/W</th><th>Description</th></tr>
<tr><td>06H</td><td>W</td><td>
<table>
<tr><th>D1</th><th>D0</th><th>GAMMA : γ correction processing</th></tr>
<tr><td>0</td><td>0</td><td>Character, photo : γ = 1</td></tr>
<tr><td>0</td><td>1</td><td>Character, photo : γ = download value</td></tr>
<tr><td>1</td><td>0</td><td>Character : γ = 1; photo : γ = download value</td></tr>
<tr><td>1</td><td>1</td><td>Character : γ = download value ; photo : γ = 1</td></tr>
</table>
Note: Judgment between character and photo is based on the result of image zone separation.
</td></tr>
<tr><td>07H</td><td>W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>POL</td><td colspan="2">DITH</td><td colspan="2">MODE</td><td colspan="3">SLICE</td></tr>
</table>
(Default value : 00H)
<table>
<tr><th>D7</th><th>POL : conversion-to-binary output mode</th></tr>
<tr><td>0</td><td>White : 1; black : 0</td></tr>
<tr><td>1</td><td>White : 0; black : 1</td></tr>
</table>
<table>
<tr><th>D6</th><th>D5</th><th>DITH : dither matrix size</th></tr>
<tr><td>0</td><td>0</td><td>4 × 4</td></tr>
<tr><td>0</td><td>1</td><td>4 × 8</td></tr>
<tr><td>1</td><td>0</td><td>8 × 8</td></tr>
<tr><td>1</td><td>1</td><td>—</td></tr>
</table>
<table>
<tr><th>D4</th><th>D3</th><th>MODE : selection of the conversion-to-binary mode</th></tr>
<tr><td>0</td><td>0</td><td>Simple binary</td></tr>
<tr><td>0</td><td>1</td><td>Organized dither</td></tr>
<tr><td>1</td><td>0</td><td>Image zone separation (simple binary + error diffusion)</td></tr>
<tr><td>1</td><td>1</td><td>Error diffusion</td></tr>
</table>
<table>
<tr><th>D2</th><th>D1</th><th>D0</th><th>SLICE : threshold factor for conversion to binary</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>6/16</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>7/16</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>8/16</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>9/16</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>10/16</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>11/16</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>12/16</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>13/16</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Address</th><th>R/W</th><th>Description</th></tr>
<tr><td>08H</td><td>W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td></td><td></td><td colspan="2">ERROR</td><td colspan="2">MTF_C</td><td colspan="2">MTF_I</td></tr>
</table>
(Default value : 00H)
<table>
<tr><th rowspan="2">D5</th><th rowspan="2">D4</th><th colspan="2">ERROR</th></tr>
<tr><th>Error (base)</th><th>Rate of dither addition to errors</th></tr>
<tr><td>0</td><td>0</td><td>Strong (7/8)</td><td>Weak (1/8)</td></tr>
<tr><td>0</td><td>1</td><td>Strong (7/8)</td><td>Strong (1/4)</td></tr>
<tr><td>1</td><td>0</td><td>Weak (3/4)</td><td>Weak (1/8)</td></tr>
<tr><td>1</td><td>1</td><td>Weak (3/4)</td><td>Strong (1/4)</td></tr>
</table>
<table>
<tr><th>D3</th><th>D2</th><th>MTF_C : MTF compensation factor</th></tr>
<tr><td>0</td><td>0</td><td>1/4</td></tr>
<tr><td>0</td><td>1</td><td>1/2</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td></tr>
</table>
Note: This is valid when MODE is simple binary or image zone separation (character).
<table>
<tr><th>D1</th><th>D0</th><th>MTF_I : MTF compensation factor</th></tr>
<tr><td>0</td><td>0</td><td>1/4</td></tr>
<tr><td>0</td><td>1</td><td>1/2</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td></tr>
</table>
Note: This is valid when MODE is organized dither, error diffusion or image zone separation (photo).
</td></tr>
<tr><td>09H</td><td>W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td></td><td></td><td colspan="6">SEPA_A</td></tr>
</table>
(Default value : 00H)
D5 to D0 : SEPA_A Image zone separation parameter (differential)
</td></tr>
<tr><td>0AH</td><td>W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td></td><td></td><td colspan="6">SEPA_B</td></tr>
</table>
(Default value : 00H)
D5 to D0 : SEPA_B Image zone separation parameter (minimum)
</td></tr>
<tr><td>0BH</td><td>W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td></td><td></td><td colspan="6">SEPA_C</td></tr>
</table>
(Default value : 00H)
D5 to D0 : SEPA_C Image zone separation parameter (maximum)
</td></tr>
</table>

<table>
<tr><th>Address</th><th>R/W</th><th>Description</th></tr>
<tr><td>0CH</td><td>W</td><td>
<table>
<tr><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td></td><td></td><td colspan="2">MAX_UP</td><td colspan="2">MAX_DOWN</td><td colspan="2">MIN_UP</td></tr>
</table>
(Default value : 00H)
<table>
<tr><th>D5</th><th>D4</th><th>MAX_UP : background level detection Clock for the up counter</th></tr>
<tr><td>0</td><td>0</td><td>Ordinary (T = (single pixel cycle) × 32)</td></tr>
<tr><td>0</td><td>1</td><td>Slow (T = (single pixel cycle) × 64)</td></tr>
<tr><td>1</td><td>0</td><td>Fast (T = (single pixel cycle) × 16)</td></tr>
<tr><td>1</td><td>1</td><td>Fastest (T = (single pixel cycle) × 8)</td></tr>
</table>
<table>
<tr><th>D3</th><th>D2</th><th>MAX_DOWN : background level detection Clock for the down counter</th></tr>
<tr><td>0</td><td>0</td><td>Ordinary (T = (single pixel cycle) × 128)</td></tr>
<tr><td>0</td><td>1</td><td>Slow (T = (single pixel cycle) × 256)</td></tr>
<tr><td>1</td><td>0</td><td>Fast (T = (single pixel cycle) × 64)</td></tr>
<tr><td>1</td><td>1</td><td>Fastest (T = (single pixel cycle) × 32)</td></tr>
</table>
<table>
<tr><th>D1</th><th>D0</th><th>MIN_UP : character level detection Clock for the up counter</th></tr>
<tr><td>0</td><td>0</td><td>Ordinary (T = (single pixel cycle) × 128)</td></tr>
<tr><td>0</td><td>1</td><td>Slow (T = (single pixel cycle) × 256)</td></tr>
<tr><td>1</td><td>0</td><td>Fast (T = (single pixel cycle) × 64)</td></tr>
<tr><td>1</td><td>1</td><td>Fastest (T = (single pixel cycle) × 32)</td></tr>
</table>
</td></tr>
<tr><td>0DH</td><td>W</td><td>
<table>
<tr><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td></td><td></td><td colspan="6">UL_MIN</td></tr>
</table>
(Default value : 1FH)
D5 to D0 : UL_MIN Detection of background/character levels
Highest limit of character levels
</td></tr>
<tr><td>0EH</td><td>W</td><td>
<table>
<tr><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td></td><td></td><td colspan="6">LL_MAX</td></tr>
</table>
(Default value : 20H)
D5 to D0 : LL_MAX Detection of background/character levels
Lowest limit of background levels
Lowest limit of background levels (LL_MAX) > highest limit of character levels (UL_MIN)
</td></tr>
<tr><td>0FH</td><td>R/W</td><td>
<table>
<tr><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td></td><td></td><td colspan="6">GAMMA_D <5 : 0></td></tr>
</table>
D5 to D0 : GAMMA_D Built-in γ memory data
</td></tr>
<tr><td>10H</td><td>R/W</td><td>
<table>
<tr><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td></td><td></td><td colspan="6">DITH_D <5 : 0></td></tr>
</table>
D5 to D0 : DITH_D Built-in dither memory data
</td></tr>
</table>

Address	R/W	Description
11H	W	D7 D6 D5 D4 D3 D2 D1 D0 OFFSET <7 : 0> (Default value : 00H) D7 to D0 : OFFSET <7 : 0> Offset for cut-out Lowest order 8 bits
12H	W	D7 D6 D5 D4 D3 D2 D1 D0 OFFSET <12 : 8> (Default value : 00H) D3 to D0 : OFFSET <12 : 8> Offset for cut-out Highest order 5 bits
13H	W	D7 D6 D5 D4 D3 D2 D1 D0 OUTLENGTH <7 : 0> (Default value : 00H) D7 to D0 : OUTLENGTH <7 : 0> No. of output pixels Lowest order 8 bits
14H	W	D7 D6 D5 D4 D3 D2 D1 D0 OUTLENGTH <12 : 8> (Default value : 00H) D3 to D0 : OUTLENGTH <12 : 8> No. of output pixels Highest order 5 bits Note: OUTLENGTH <12 : 8> must be a multiple of 8. If a number of output pixels is not a multiple of 8, the remainder of the division must be omitted.
15H	R/W	D7 D6 D5 D4 D3 D2 D1 D0 CNV_D D0 : CNV_D Indication of enlargement/reduction

<table>
<tr><th>Address</th><th>R/W</th><th>Description</th></tr>
<tr><td>16H</td><td>R/W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>AGCSTP</td><td>SRDYS</td><td>SRDYB</td></tr>
</table>
(Default value : 00H)
<table>
<tr><th>D2</th><th>AGCSTP : gain control counter</th></tr>
<tr><td>0</td><td>Gain control counter valid.</td></tr>
<tr><td>1</td><td>Gain fixed.</td></tr>
</table>
<table>
<tr><th>D1</th><th>SRDYS : SRDY control</th></tr>
<tr><td>0</td><td>SRDY control through the register</td></tr>
<tr><td>1</td><td>SRDY control through the external pin</td></tr>
</table>
<table>
<tr><th>D0</th><th>SRDYB : data transfer start ready.</th></tr>
<tr><td>0</td><td>Transfer allowed.</td></tr>
<tr><td>1</td><td>Transfer not allowed.</td></tr>
</table>
- In the case of data control through the register, the SDRYB input pin must be always set at “H”. For the control through the register, the SRDY register must be controlled line by line.

(∗) Write only
</td></tr>
<tr><td>17H</td><td>W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td colspan="8">INTCLR</td></tr>
</table>
INT signals are negated by accessing to this address.
</td></tr>
<tr><td>18H</td><td>R/W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td colspan="8">GAIN <7 : 0></td></tr>
</table>
In reading : the current gain value of the gain control counter can be read.
In writing : the gain value of the gain control counter can be set.
However, this is valid only if AGCSTP = 1.
</td></tr>
<tr><td>19H</td><td>R/W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td></td><td></td><td colspan="6">UNIF <5 : 0></td></tr>
</table>
D5 to D0 : UNIF_D Built- in uniformity correction memory data

- With UMODE = 0, access to the uniformity correction memory for black correction is available.
- With UMODE = 1, access to the uniformity correction memory for white correction is available.
</td></tr>
</table>

Description of the Operations of the Analog Circuits

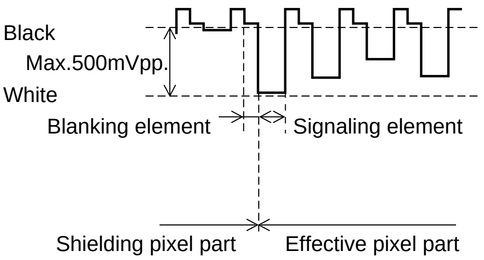
The configuration of the analog processing circuits is shown in Fig. 17.

(1) Sensor selection circuit

The four types of sensors in the table can be connected to the circuit.

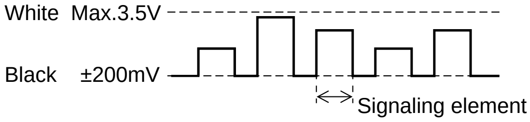
Register 02H	Sensor type
CCD	CCD sensor
CIS1	CIS sensor which outputs light voltages (white voltage) of 3.5V or lower
CIS2	CIS sensor which outputs light voltages (white voltage) of 2V or lower
CIS3	CIS sensor which output shielding pixels for each line

<CCD mode>



The amplitudes of sensor signals are multiplied by –4 through the two operating amplifiers directly after the switch to select the CCD mode. (The waveforms of the signals are inverted at the same time.) As a result, the sensor signals input to the sample and hold circuit have a dark voltage of 2.2V.

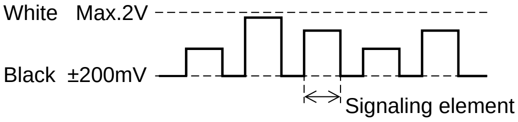
<CIS1 mode>



The amplitude of signals input from the sensor are halved. Then, their reference potential is shifted up to 2.2V.

As a result, the sensor signals input to the sample and hold circuit have a dark voltage of 2.2V.

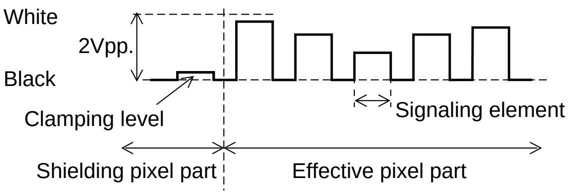
<CIS2 mode>



The reference potential of signals input from the sensor is shifted up to 2.2V.

As a result, the sensor signals input to the sample and hold circuit have a dark voltage of 2.2V.

<CIS3 mode>



Sensor signals with a dark voltage of 2.2V clamped by line clamping input are directly input to the sample and hold circuit.

(2) Line clamping circuit

This circuit is used for CCD (line clamping mode) and CIS3.

The reference voltage (dark voltage) output in the shielding pixel part of the sensor is sampled by LCMP (line clamping pulses) and shifted up to the internal reference voltage of 2.2V. This is not used for the CIS1 or CIS2 input sensor (set off constantly).

: register 02 (LCMPS)

(3) Sample and hold circuit and bit clamping circuit

In the CCD mode, bit clamping, as well as line clamping, can be performed. The blanking elements of each pixel of sensor output is sampled by BTCMP (bit clamping pulses). The differences of signals from the reference potential sampled by the bit clamping circuit are input to the gain control circuit of next step as signaling elements. To turn off bit clamping, set BLS invalid, so that the reference potential will be fixed at the internal reference potential of 2.2V.

: register 02 (BLS)

(4) Gain control circuit

The amplifying factor (gain) must be adjusted so that the amplitudes of sensor signals can come within the dynamic range of the A/D converter. The gain is set through the automatic gain control in the AGC mode (register 00) or directly through the register 18 (GAIN <7 : 0>). The gain changes within the following ranges according to the sensor used.

Mode	Amplifying factor of signals (gain)
CCD	4 to 20
CIS1	0.5 to 2.5
CIS2	1 to 5
CIS3	1 to 5

In the AGC mode, the gain control counter is set at the greatest gain in the initial state and then counted down each time an overflow bit is output from the A/D converter. The count (gain) of the gain control counter is directly read/written through the register 18 (GAIN <7 : 0>). The counting operation of the counter can be controlled through the register 16 (AGCSTP).

(5) Internal reference voltage

Internal reference voltage source for the analog circuits:

this generates the reference voltage (2.2V) for the line clamping circuit, the sample and hold circuit, and the bit clamping circuit.

A/D converter reference voltage generation circuit:

this generates VWL (white level reference voltage of 3.8V) and VBL (black level reference voltage of 1.8V) for the A/D converter.

(6) Black level clamping circuit

This circuit adjust the level of reference voltage to the A/D converter from analog circuits.

The black clamping circuit is used in the CCD or CID3 mode. (See Figs. 18, 19 and 22) The GCAO pin and the BCMI pin are capacity-coupled. The output reference potential in the shielding pixel part of sensor signals are applied to the BCMV pin as the VBL (black level reference voltage of 1.8V) for the A/D converter.

BLCMP (black level clamping pulses) are generated concurrently with the shielding pixel part of each line. To turn off this circuit, set BLCMPS invalid and apply the black level reference voltage of the A/D converter to the BCMV pin. : register 02 (BLCMPS)

In the CIS1 or CIS2 mode, the LEVAJ pin is used. (See Figs. 20 and 21) Voltage is applied to the LEVAJ pin so that the reference potential of output at the GCAO pin can be adjusted to the VBL (black level reference voltage of 1.8V) of the A/D converter. Set voltage input to the LEVAJ pin as follows.

$V_{LEVAJ} = V_{VBL} - A \times G_V + 0.2$ [V]

$V_{GCAO} = V_{LEVAJ} + G_V \times V_{IN}$ [V]

where,

A: the lowest limit of dark voltage of the sensor [V]

G_V: gain (multiplying factor) of the gain control circuit

V_{IN}: signals input from the sensor [V]

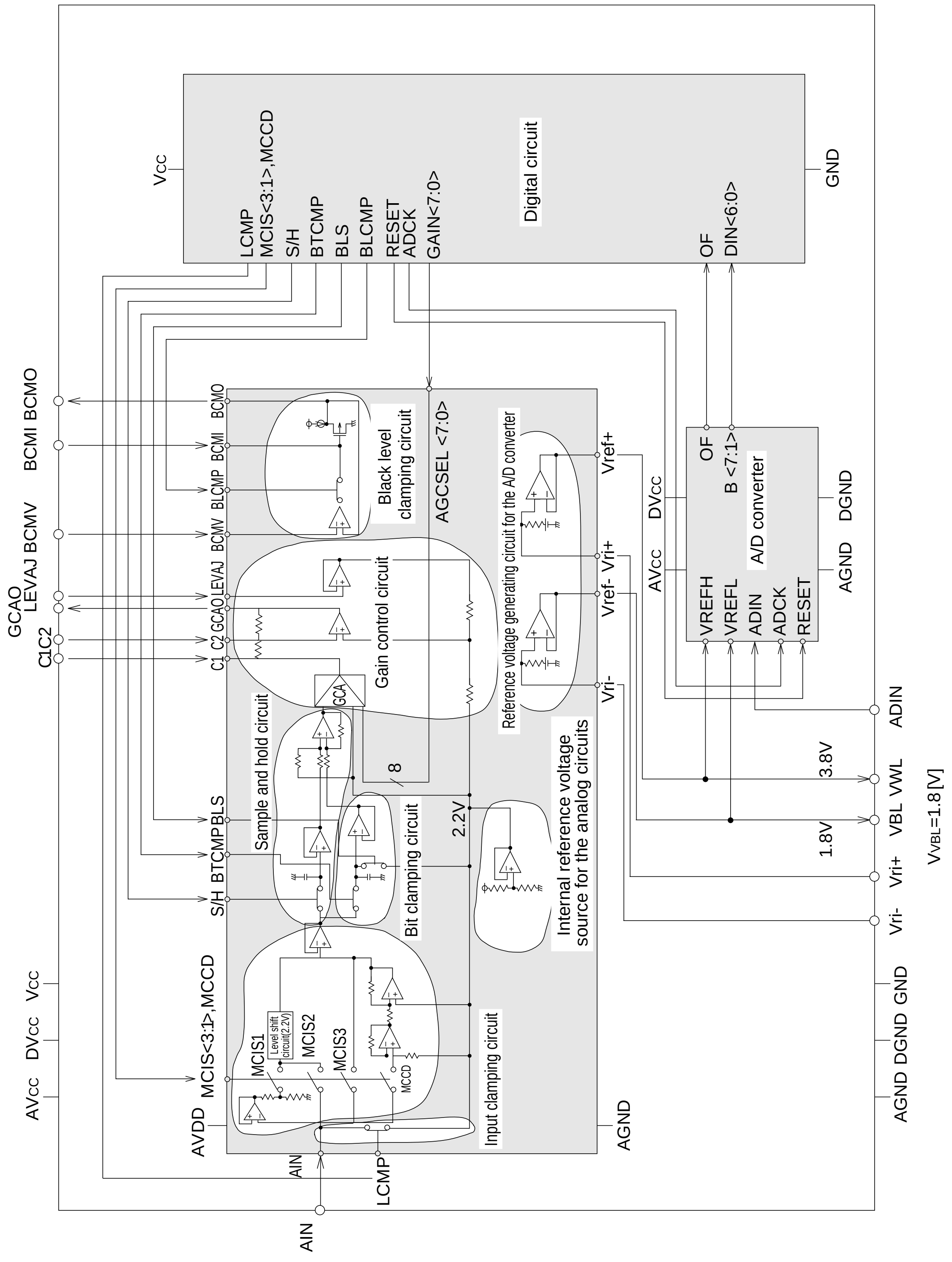
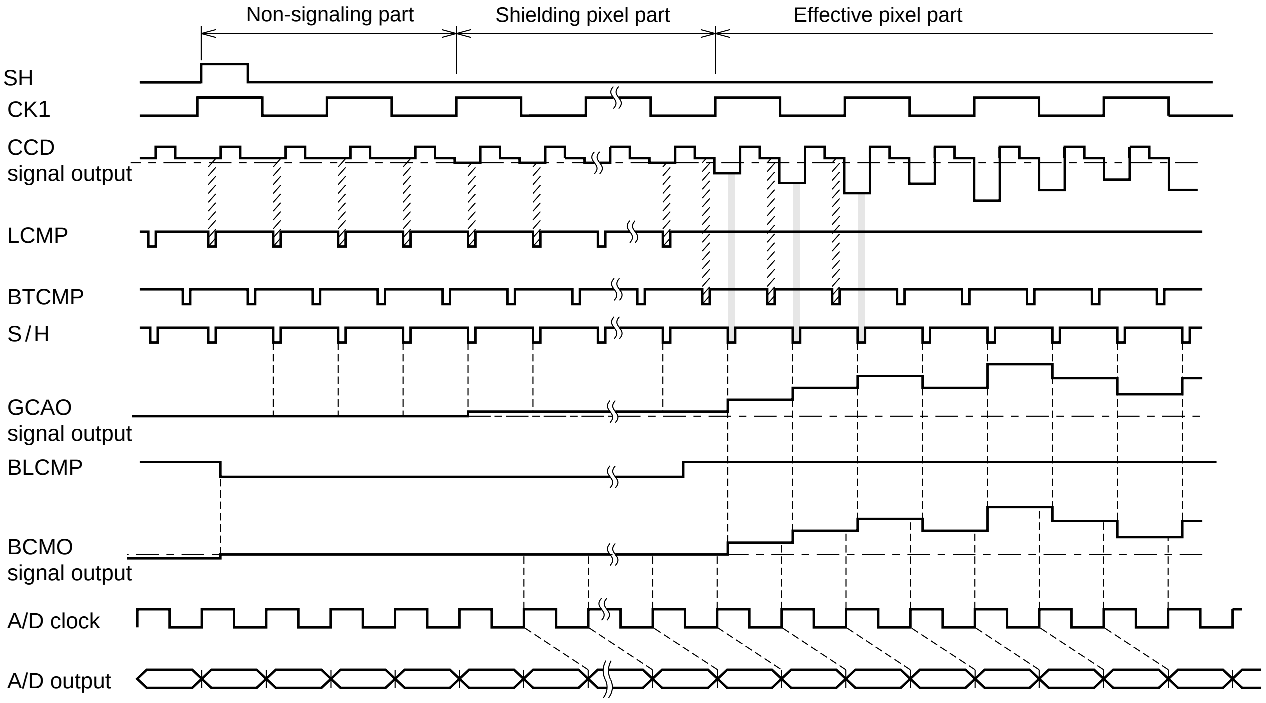
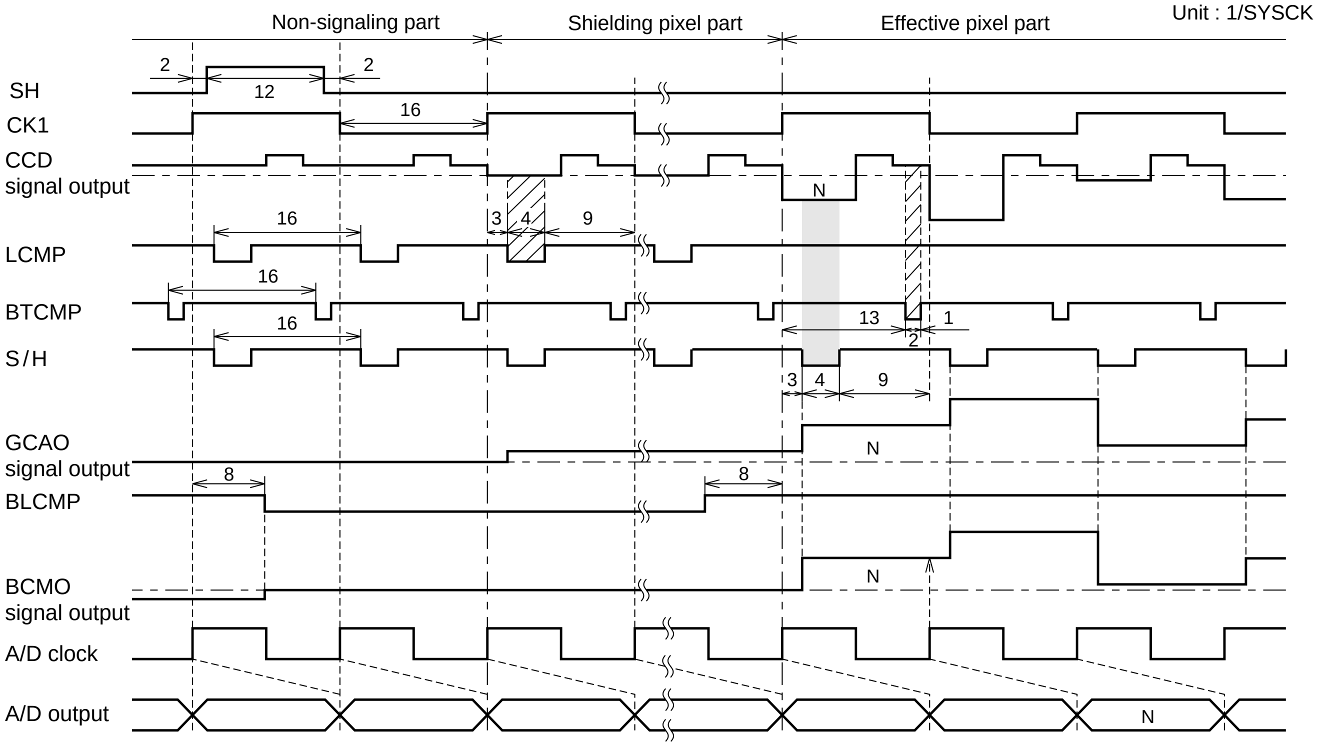


Fig. 17 Circuit Configuration of the Analog Part of the M66335FP

ANALOG CIRCUIT TIMING CHART (FOR CCD MODE/BIT CLAMPING)

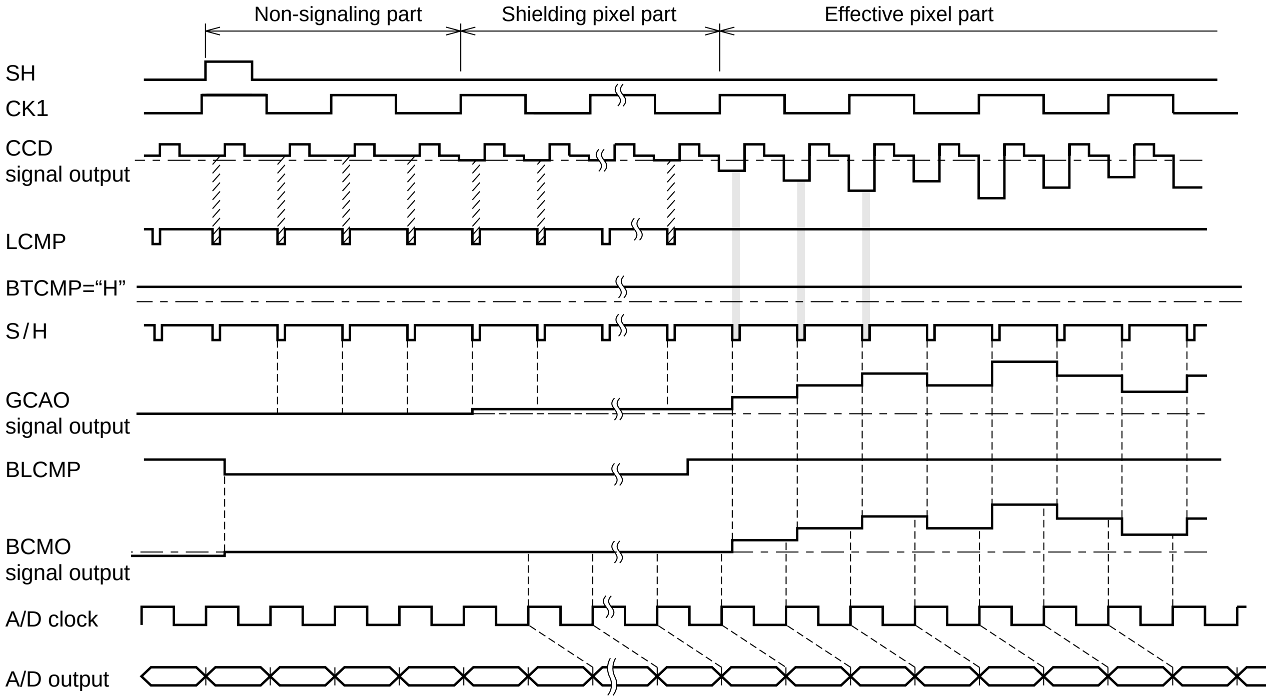
Register / Mode	Address	00H	02H						
	Bit	D6	D6	D5	D4	D3	D2	D1	D0
	Signal	SENS	LCMPS	BLS	BLCMPS	CCD	CIS3	CIS2	CIS1
CCD (bit clamping)	Setting	1	1	1	1	1	0	0	0

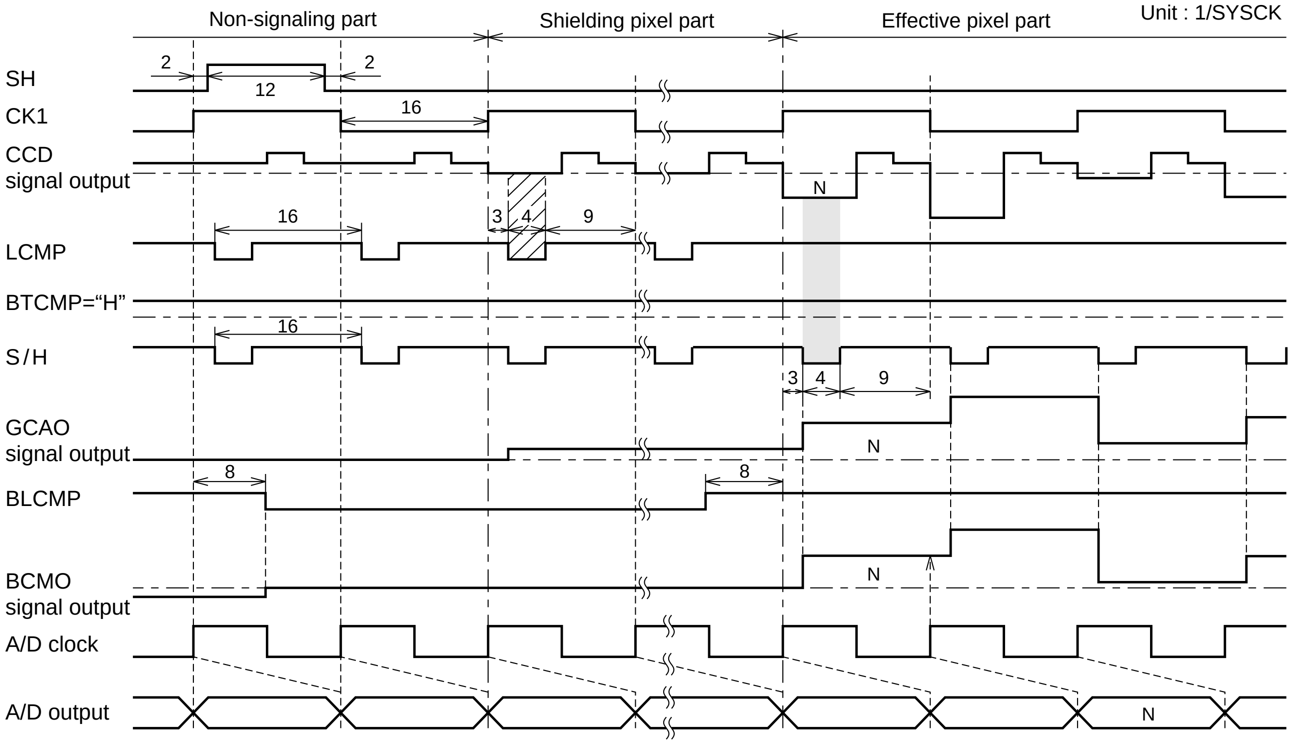




ANALOG CIRCUIT TIMING CHART (FOR CCD MODE/LINE CLAMPING)

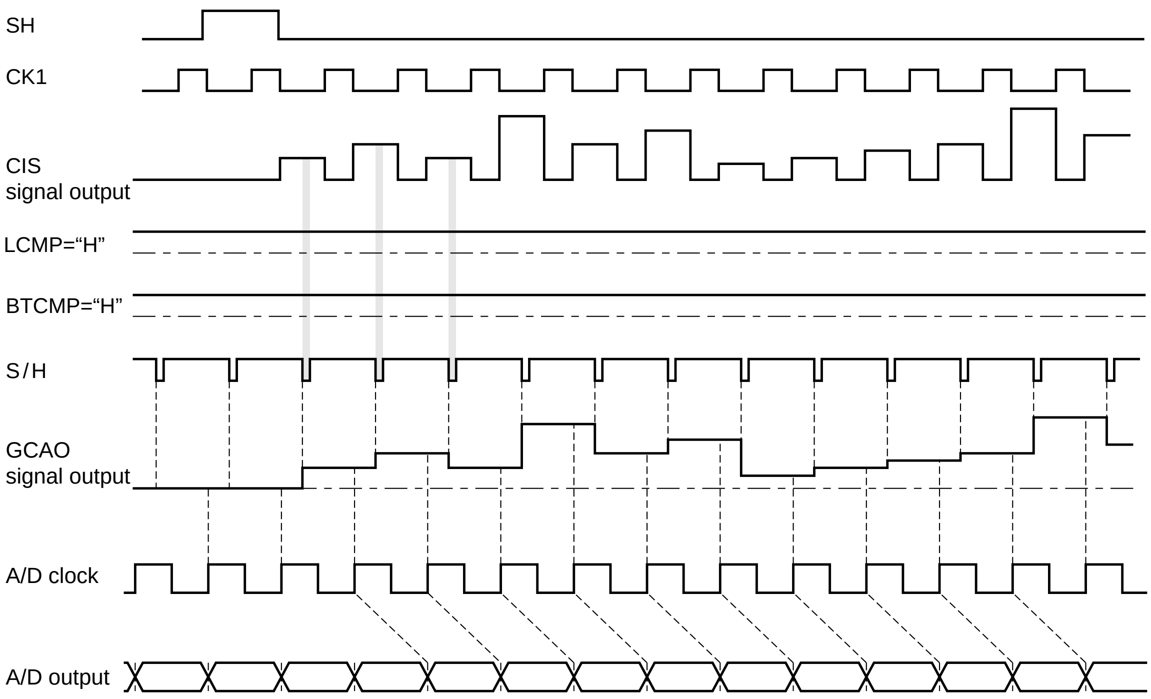
Register Mode	Address	00H	02H						
	Bit	D6	D6	D5	D4	D3	D2	D1	D0
	Signal	SENS	LCMPS	BLS	BLCMPS	CCD	CIS3	CIS2	CIS1
CCD (line clamping)	Setting	1	1	0	1	1	0	0	0

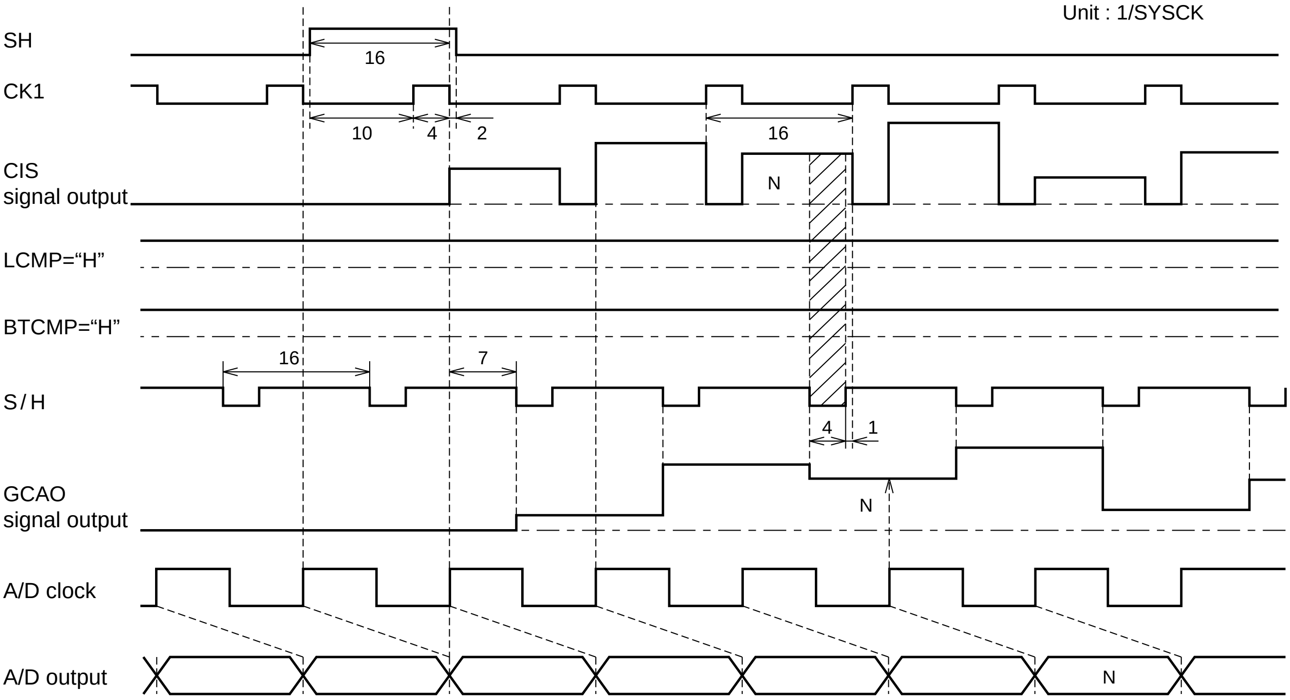




ANALOG CIRCUIT TIMING CHART (FOR CIS1 MODE)

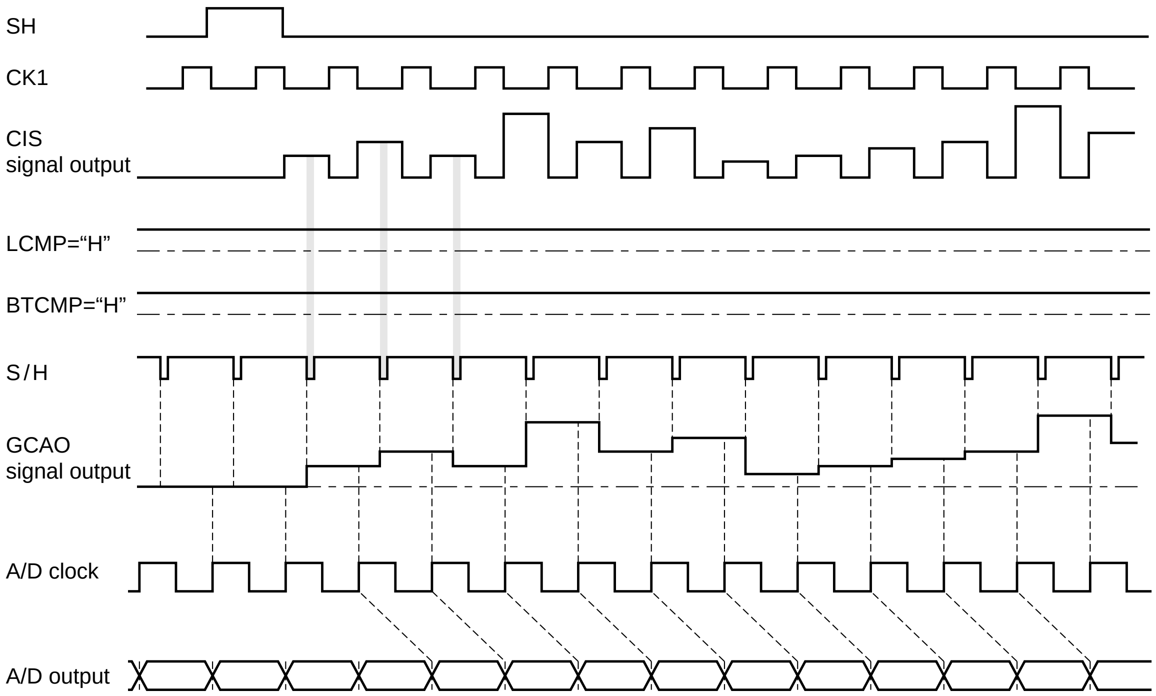
Register / Mode	Address	00H	02H							
	Bit	D6	D6	D5	D4	D3	D2	D1	D0	
	Signal	SENS	LCMPS	BLS	BLCMPS	CCD	CIS3	CIS2	CIS1	
CIS1	Setting	0	0	0	0	0	0	0	1	

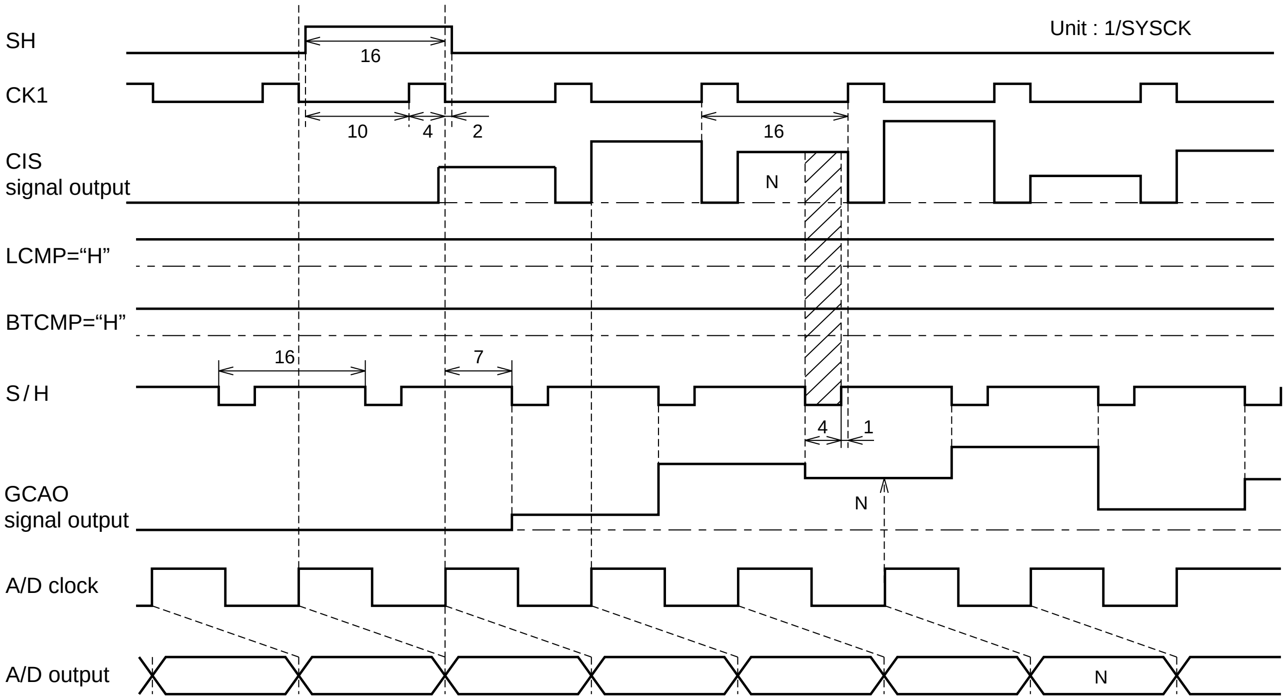




ANALOG CIRCUIT TIMING CHART (FOR CIS2 MODE)

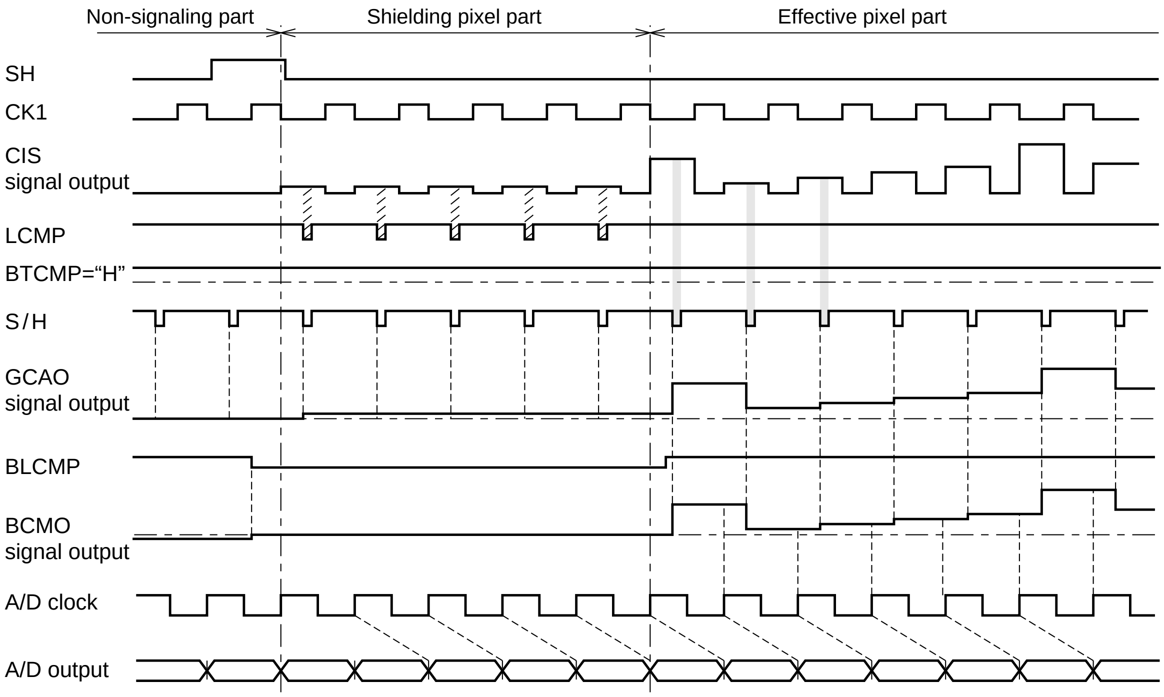
Register / Mode	Address	00H	02H						
	Bit	D6	D6	D5	D4	D3	D2	D1	D0
	Signal	SENS	LCMPS	BLS	BLCMPS	CCD	CIS3	CIS2	CIS1
CIS2	Setting	0	0	0	0	0	0	1	0

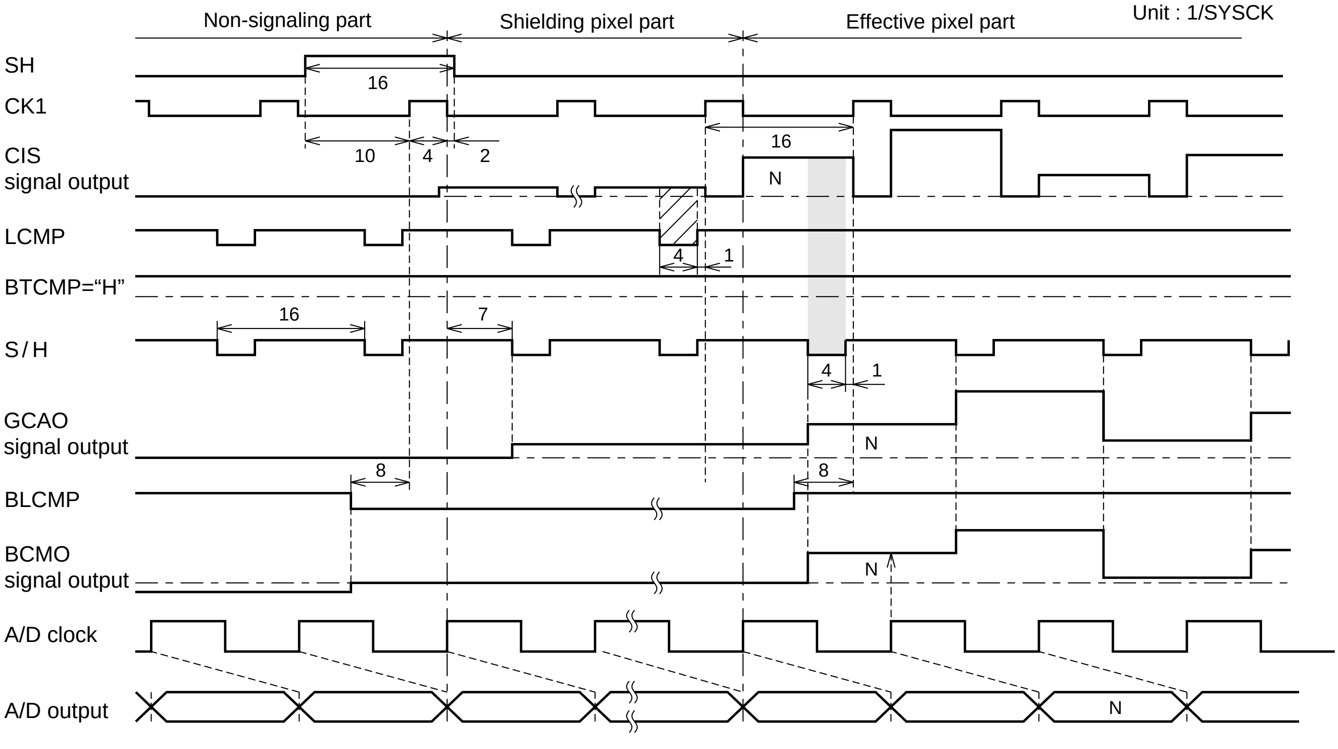




ANALOG CIRCUIT TIMING CHART (FOR CIS3 MODE)

Register / Mode	Address	00H	02H						
	Bit	D6	D6	D5	D4	D3	D2	D1	D0
	Signal	SENS	LCMPS	BLS	BLCMPS	CCD	CIS3	CIS2	CIS1
CIS3	Setting	1	1	0	1	0	1	0	0





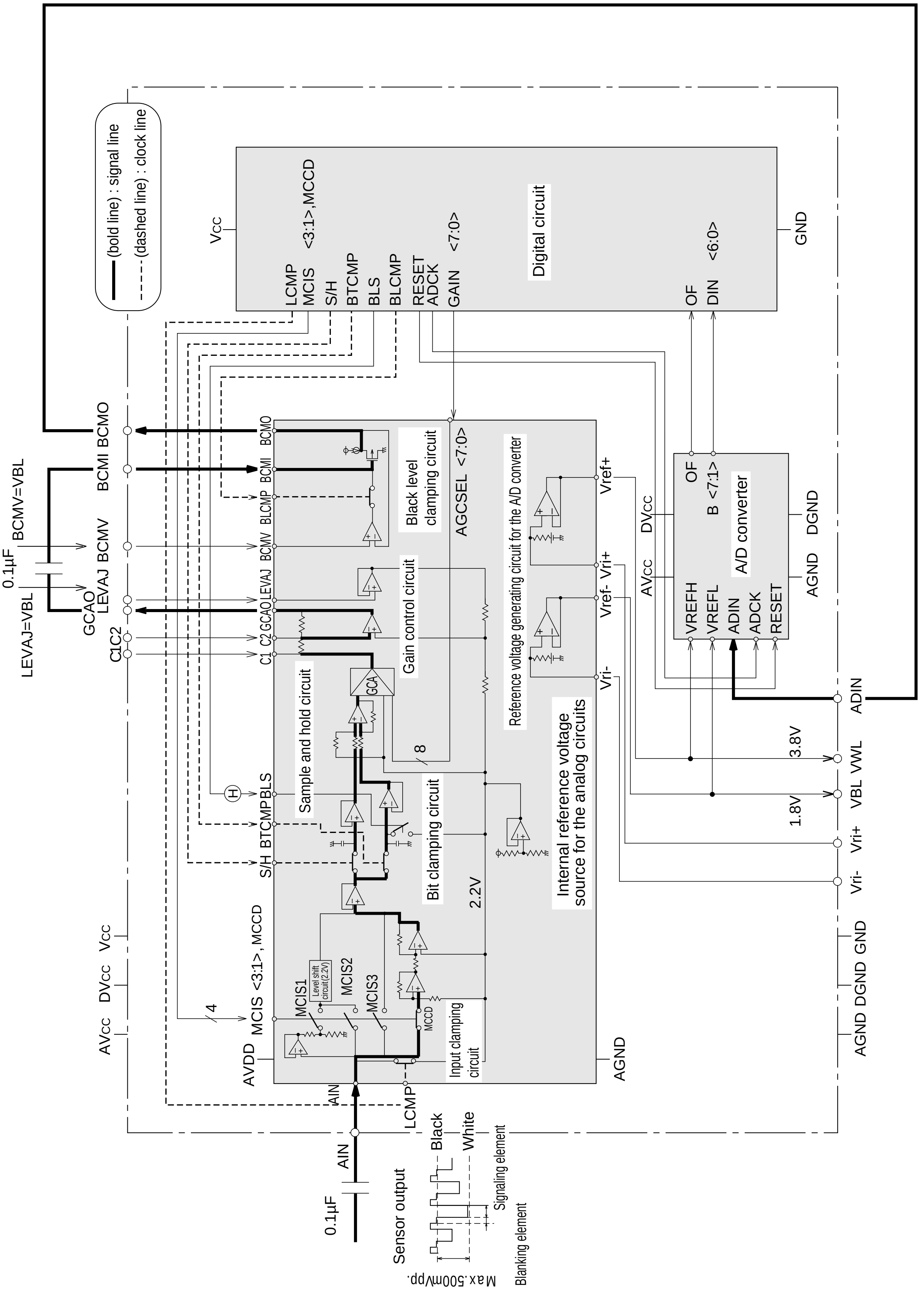


Fig. 18 External pin connections of the analog part (for the CCD mode/bit clamping)

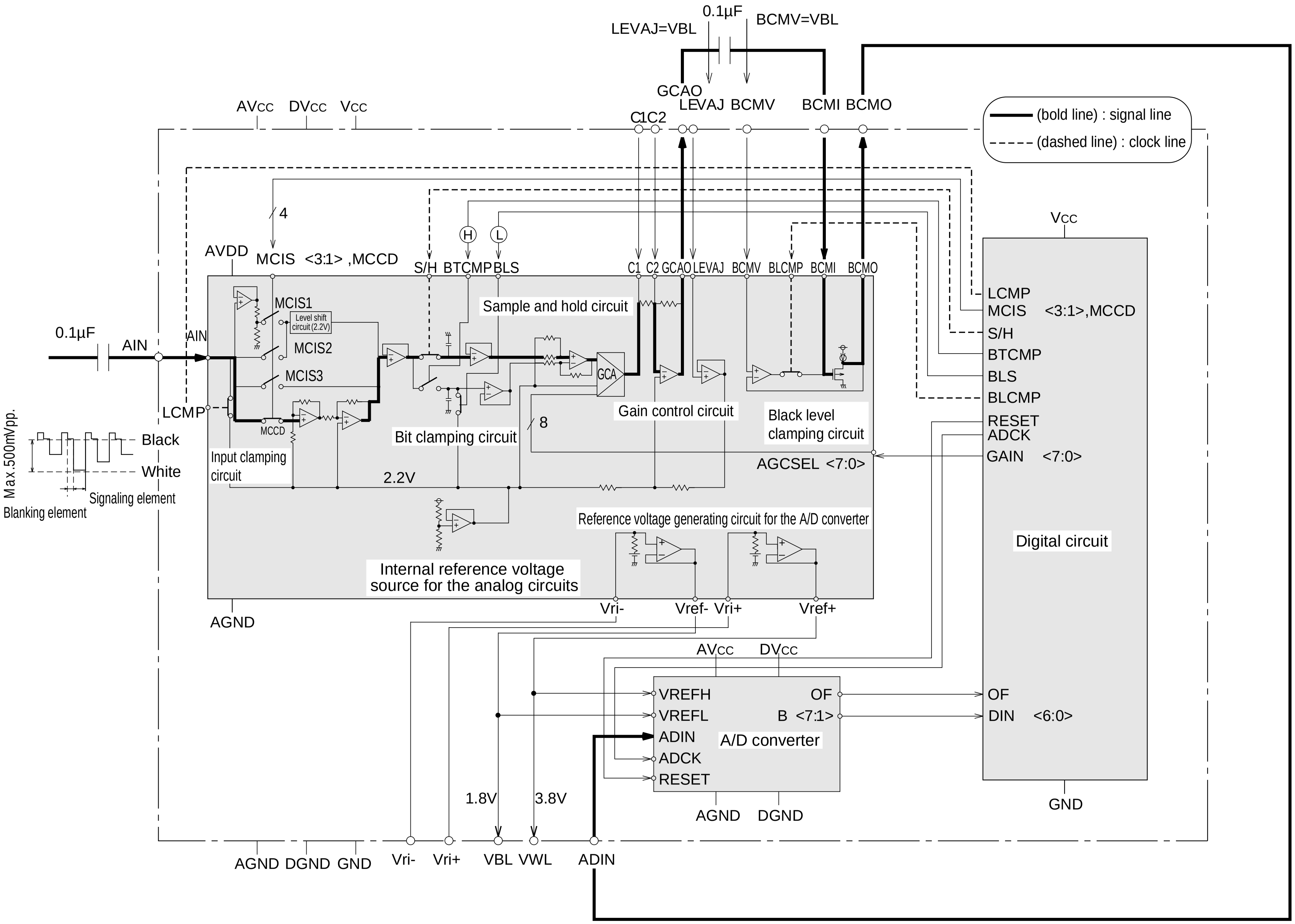
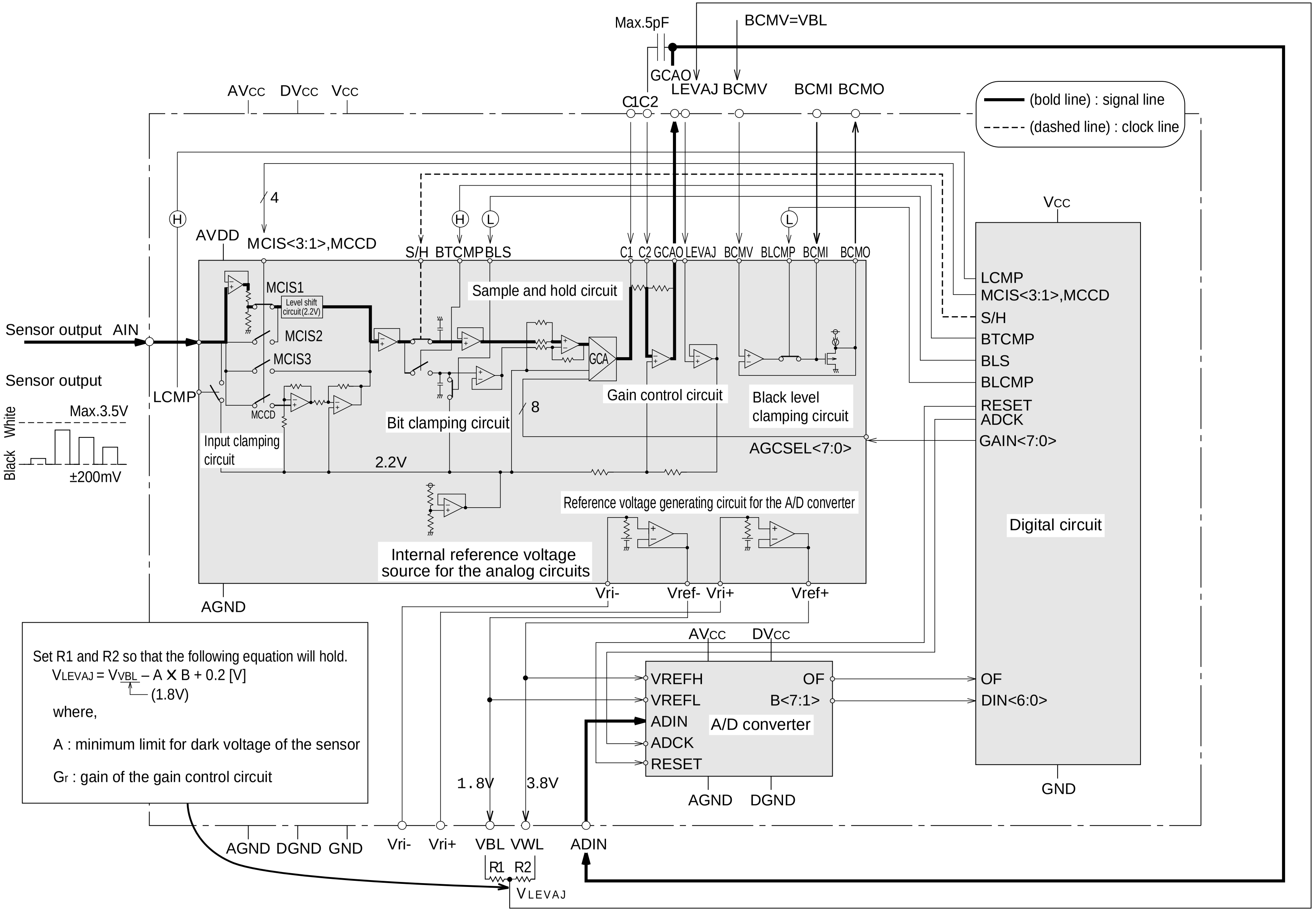


Fig. 19 External pin connections of the analog part (for the CCD mode/line clamping)



Set R1 and R2 so that the following equation will hold.

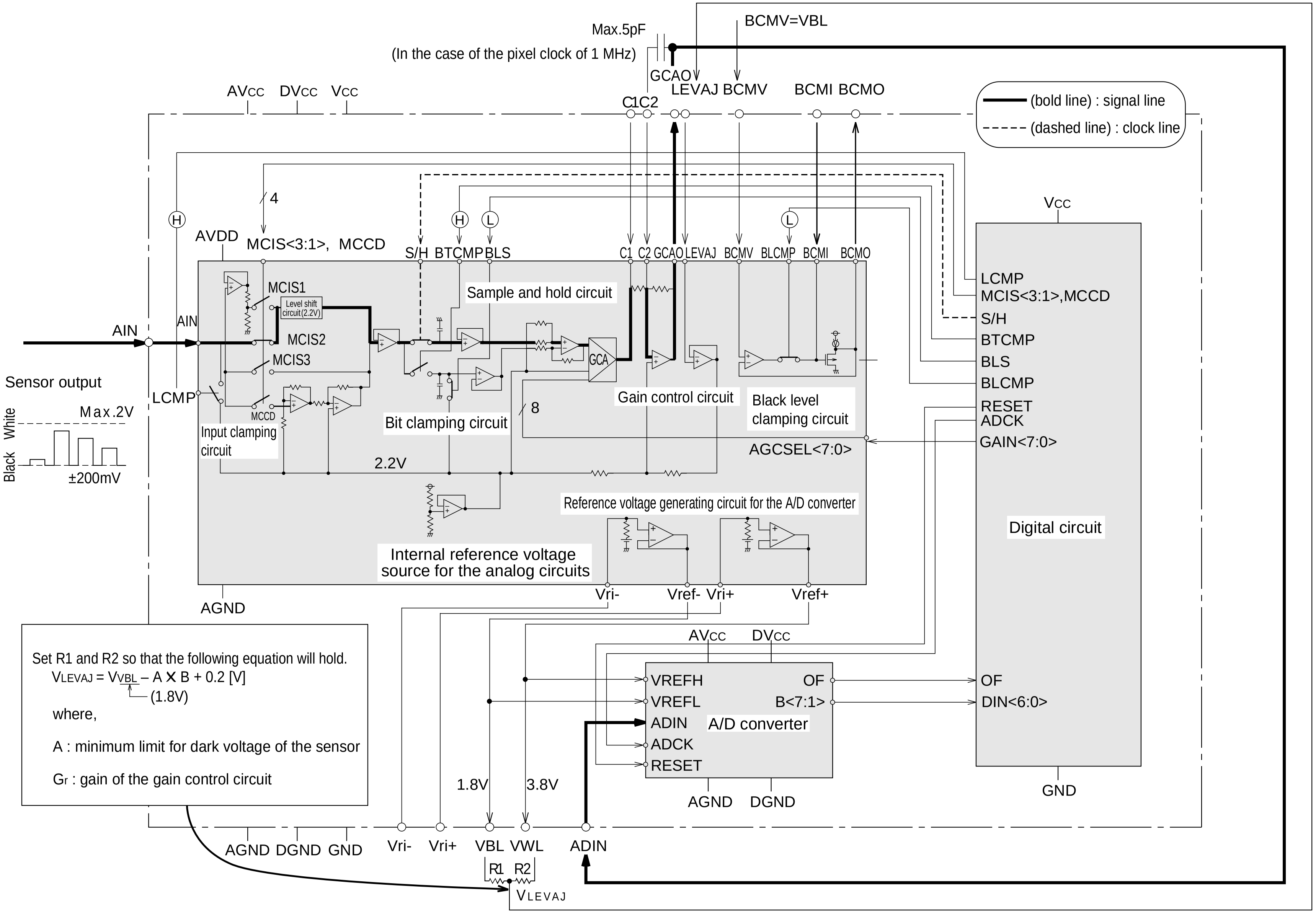
$V_{LEVAJ} = \underset{(1.8V)}{V_{VBL}} - A \times B + 0.2$ [V]

where,

A : minimum limit for dark voltage of the sensor

G_r : gain of the gain control circuit

Fig. 20 External pin connections of the analog part (for the CIS1 mode)



Set R1 and R2 so that the following equation will hold.

$V_{LEVAJ} = \underset{\text{(1.8V)}}{V_{VBL}} - A \times B + 0.2$ [V]

where,

A : minimum limit for dark voltage of the sensor

G_r : gain of the gain control circuit

Fig. 21 External pin connections of the analog part (for the CIS2 mode)

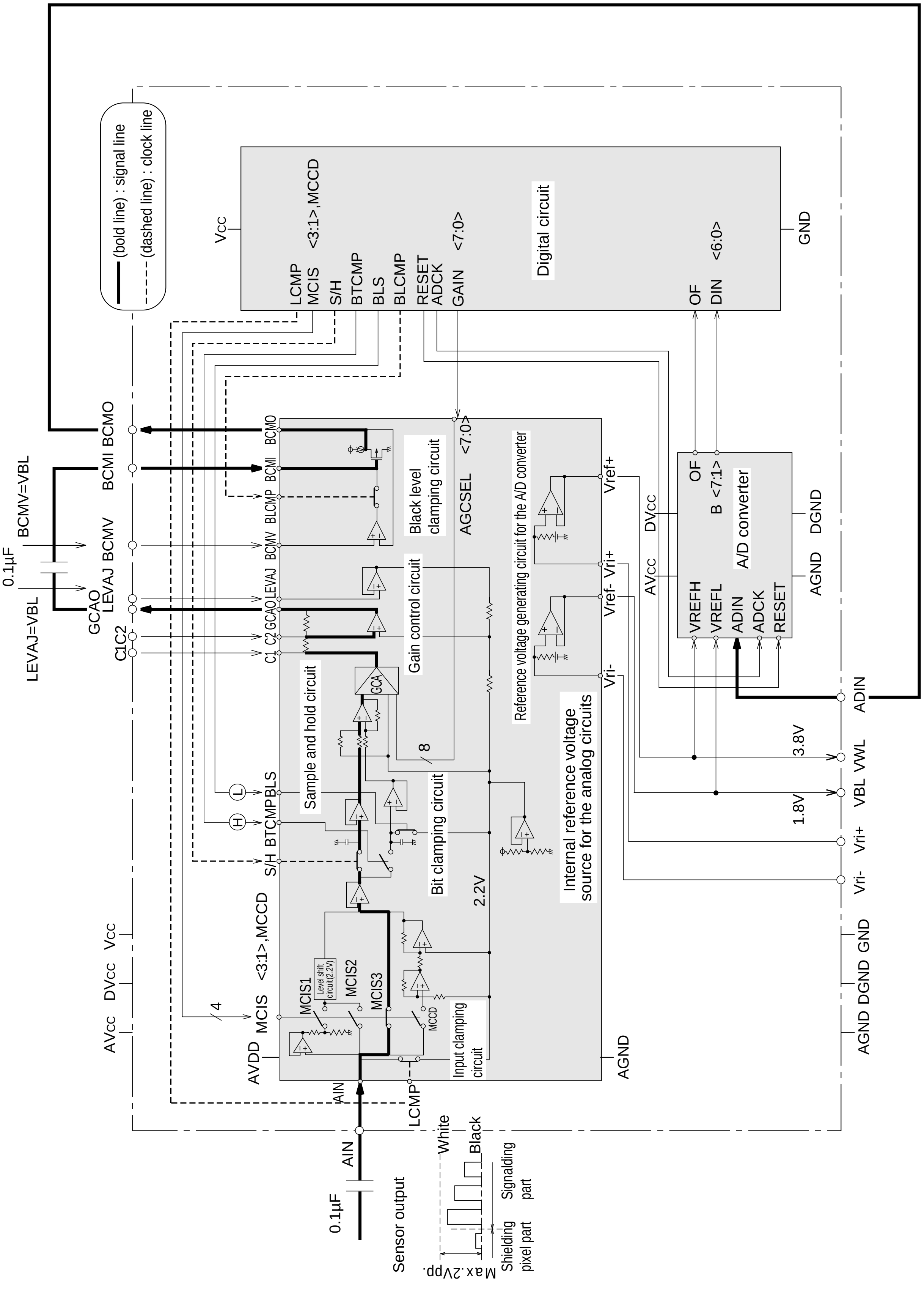
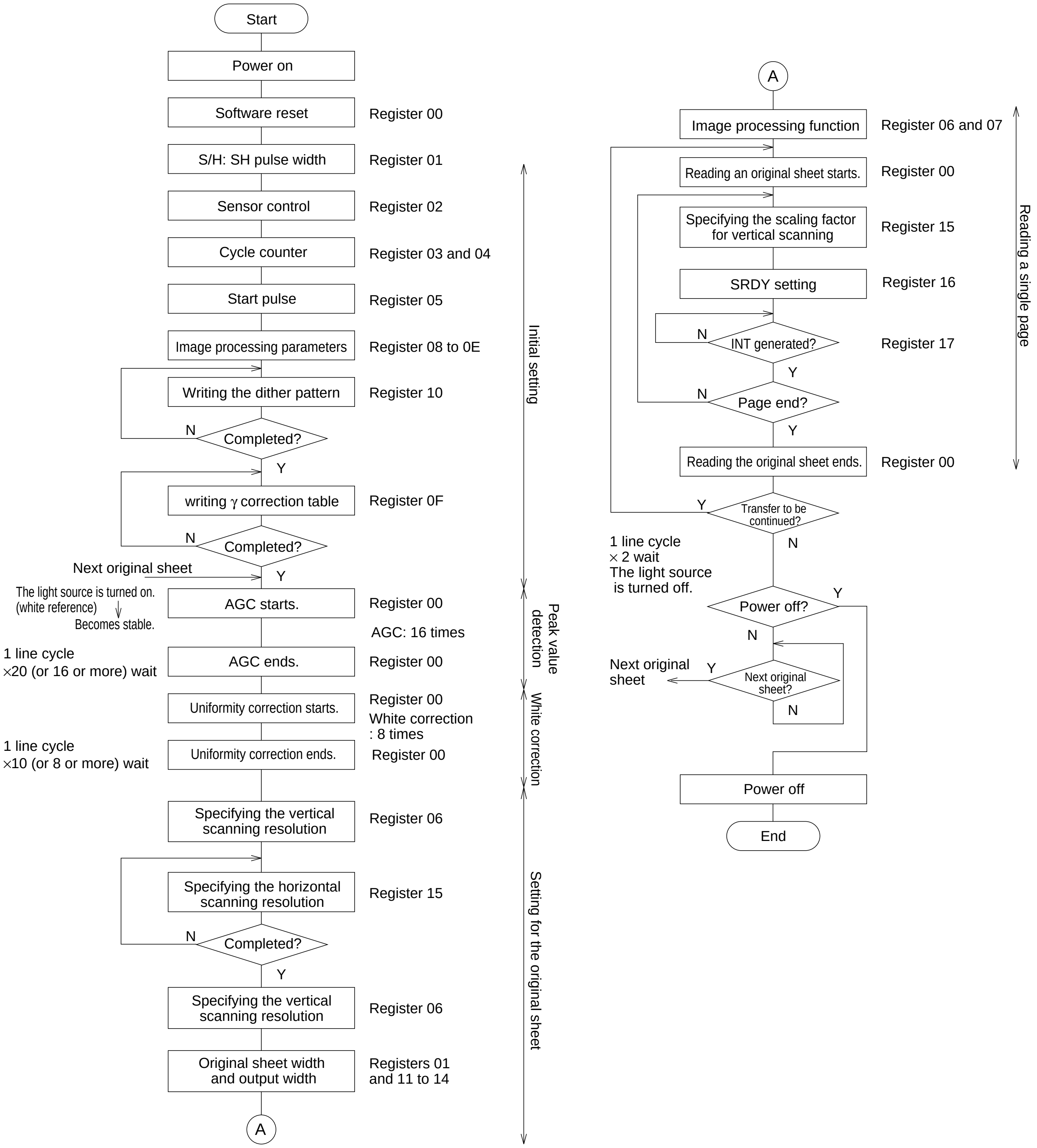
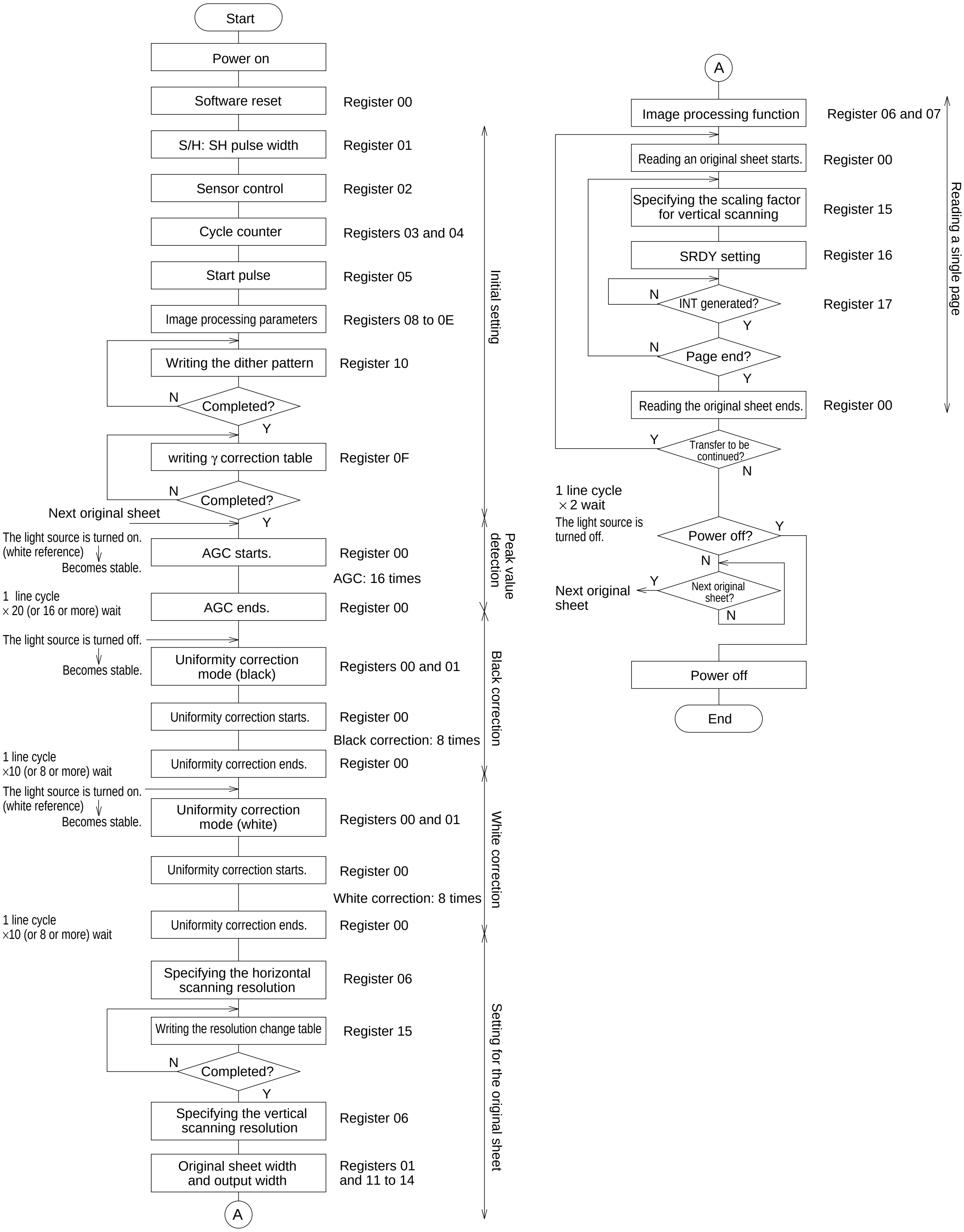


Fig. 22 External pin connections of the analog part (for the CIS3 mode)

FLOWCHART:
READING OPERATIONS (FOR THE CCD SENSOR)



READING OPERATIONS (FOR THE CIS SENSOR)



ABSOLUTE MAXIMUM RATINGS (Ta = –20 ~ 75°C unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		–0.3 ~ +6.5	V
V_I	Input voltage		–0.3 ~ V_{CC}+0.3	V
V_O	Output voltage		0 ~ V_{CC}	V
AV_{CC}	Analog supply voltage		V_{CC} –0.3 ~ V_{CC} +0.3	V
DV_{CC}	Supply voltage		V_{CC} –0.3 ~ V_{CC} +0.3	V
V_{WL}	Reference voltage (white)		–0.3 ~ AV_{CC} +0.3	V
V_{BL}	Reference voltage (black)		–0.3 ~ AV_{CC} +0.3	V
V_{AIN}	Analog input voltage		–0.3 ~ AV_{CC} +0.3	V
T_{stg}	Storage temperature		–55 ~ +150	°C

RECOMMENDED OPERATIONAL CONDITIONS

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage (for the digital system component)	4.75	5.0	5.25	V
GND	GND voltage		0.0		V
V_I	Input voltage	0		V_{CC}	V
AV_{CC}	Analog supply voltage	4.75	5.0	5.25	V
A_{GND}	Analog GND voltage		0.0		V
DV_{CC}	Supply voltage (for the digital system component)	4.75	5.0	5.25	V
D_{GND}	GND voltage		0.0		V
V_{AIN}	Input range: $V_{WL} \leq AV_{CC}$; $V_{BL} \geq A_{GND}$	1.8	2.0	2.2	V_{P-P}
T_{opr}	Operating temperature	–20		+75	°C

Note: Connect the analog system component and the digital system component separately to power supply on the evaluation board for noise prevention.

ELECTRICAL CHARACTERISTICS (Ta = –20 ~ 75°C, V_{CC} = 5V±5% unless otherwise noted)

Symbol	Parameter		Test conditions	Ratings			Unit
				Min.	Typ.	Max.	
V_{IH}	“H” input voltage			2.0			V
V_{IL}	“L” input voltage					0.8	V
V_{T+}	Positive direction input threshold					2.4	V
V_{T-}	Negative direction input threshold			0.6			V
V_H	Hysteresis value				0.2		V
V_{OH}	“H” output voltage		I_{OH} = –12mA	V_{CC}–0.8			V
V_{OL}	“L” output voltage		I_{OL} = 12mA			0.55	V
V_{OH}	“H” output voltage		I_{OH} = –4mA	V_{CC}–0.8			V
V_{OL}	“L” output voltage		I_{OL} = 4mA			0.55	V
I_{IH}	“H” input current		V_{CC} = 5.25V V_I = 5.25V			1.0	mA
I_{IL}	“L” input current		V_{CC} = 5.25V V_I = 0V			–1.0	mA
I_{OZH}	“H” input current in the off state		V_{CC} = 5.25V V_O = 5.25V			5.0	mA
I_{OZL}	“L” input current in the off state		V_{CC} = 5.25V V_O = 0V			–5.0	mA
I_{AIN}	Analog input current					1.0	mA
R_L	Reference resistance				120		Ω
E_d	Differential non-linear error				±1.0		LSB
I_{CCS}	Static current dissipation (during standby)		V_{CC} = 5.25V V_I = V_{CC}, GND		21	35	mA

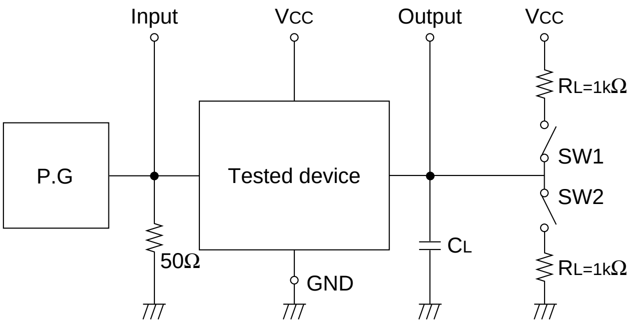
TIMING CONDITIONS (T_a = –20 ~ 75°C, V_{CC} = 5V±5% unless otherwise noted)

Symbol	Parameter		Test conditions	Ratings			Unit
				Min.	Typ.	Max.	
t_c (SYS)	System clock cycle			50			ns
t_{w+} (SYS)	System clock “H” pulse width			25			ns
t_{w-} (SYS)	System clock “L” pulse width			25			ns
t_r (SYS)	System clock rise time					20	ns
t_f (SYS)	System clock fall time					20	ns
t_w ($\overline{\text{RD}}$)	Read pulse width			100			ns
t_{su} ($\overline{\text{CS}}$-$\overline{\text{RD}}$)	Set-up time before read	$\overline{\text{CS}}$		20			ns
t_{su} (A-$\overline{\text{RD}}$)	Set-up time before read	A0 ~ A4		20			ns
t_{su} ($\overline{\text{DAK}}$-$\overline{\text{RD}}$)	Set-up time before read	$\overline{\text{DAK}}$		20			ns
t_h ($\overline{\text{RD}}$-$\overline{\text{CS}}$)	Hold time after read	$\overline{\text{CS}}$		10			ns
t_h ($\overline{\text{RD}}$-A)	Hold time after read	A0 ~ A4		10			ns
t_h ($\overline{\text{RD}}$-$\overline{\text{DAK}}$)	Hold time after read	$\overline{\text{DAK}}$		10			ns
t_w ($\overline{\text{WR}}$)	Write pulse width			100			ns
t_{su} ($\overline{\text{CS}}$-$\overline{\text{WR}}$)	Set-up time before write	$\overline{\text{CS}}$		20			ns
t_{su} (A-$\overline{\text{WR}}$)	Set-up time before write	A0 ~ A4		20			ns
t_{su} (D-$\overline{\text{WR}}$)	Set-up time before write	D0 ~ D7		50			ns
t_h ($\overline{\text{WR}}$-$\overline{\text{CS}}$)	Hold time after write	$\overline{\text{CS}}$		20			ns
t_h ($\overline{\text{WR}}$-A)	Hold time after write	A0 ~ A4		10			ns
t_h ($\overline{\text{WR}}$-D)	Hold time after write	D0 ~ D7		0			ns
t_h ($\overline{\text{STIM}}$-$\overline{\text{SRDY}}$)	Hold time after $\overline{\text{STIM}}$	$\overline{\text{SRDY}}$		0			ns

SWITCHING CHARACTERISTICS (Ta = –20 ~ 75°C, VCC = 5V±5% unless otherwise noted)

Symbol	Parameter	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
t_{PZL} ($\overline{RD}$-D)	Enable time for data output after read	C_L = 150pF			75	ns
t_{PZH} ($\overline{RD}$-D)						ns
t_{PLZ} ($\overline{RD}$-D)	Disable time for data output after read		10		50	ns
t_{PHZ} ($\overline{RD}$-D)						ns
t_{PHL} ($\overline{RD}$-DRO)	Propagation time of DRO output after read	C_L = 50pF			50	ns

TEST CIRCUIT

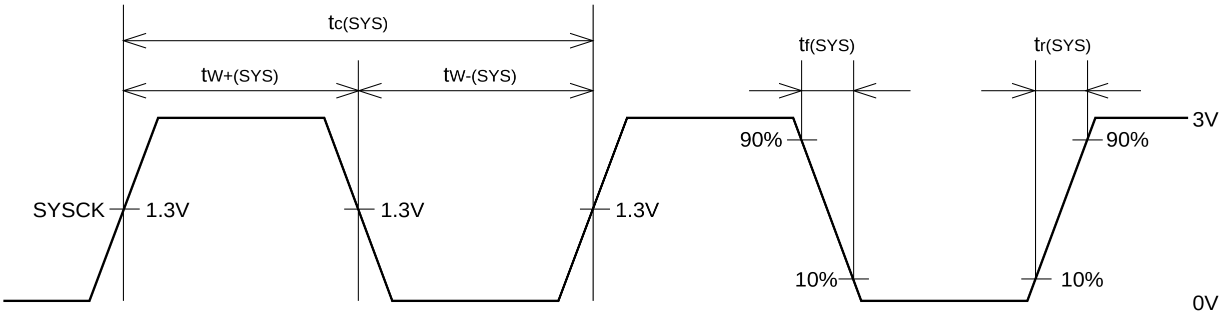


Parameter	SW1	SW2
t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) Characteristics (10% to 90%) of the pulse generator (PG): t_r = 3ns; t_f = 3ns

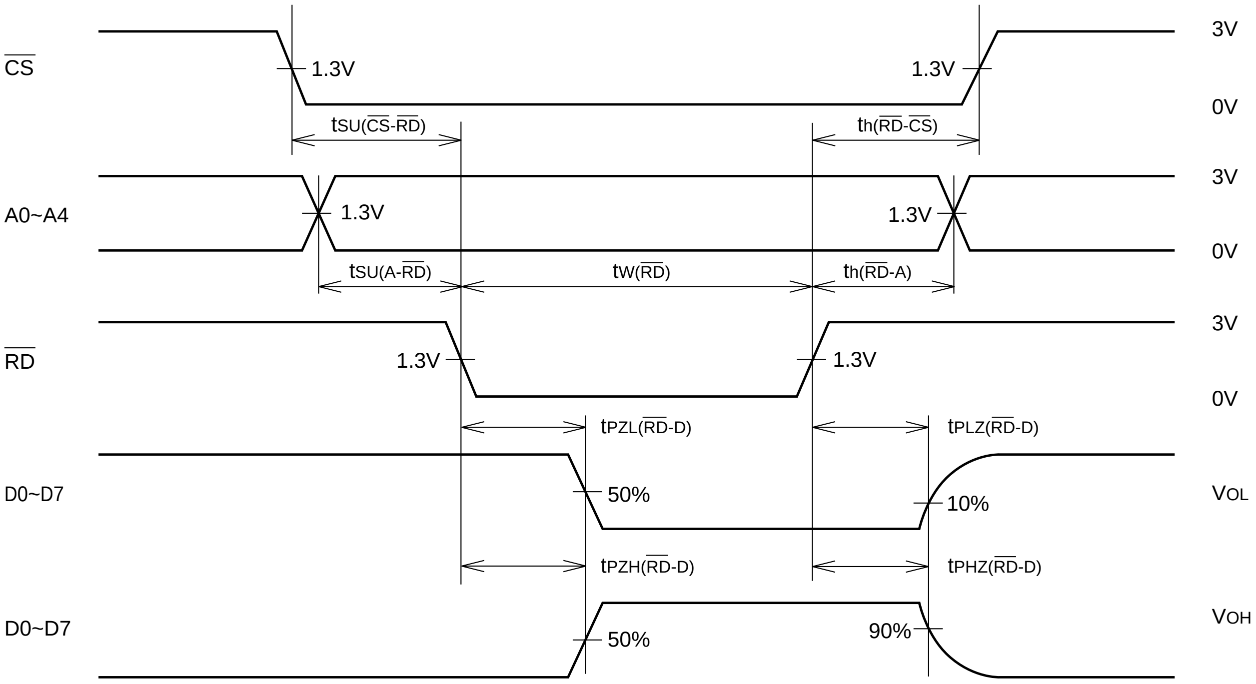
(2) Capacitance CL (= 150pF) includes the stray capacitance of connections and input capacitance of the probe.

SYSTEM CLOCK

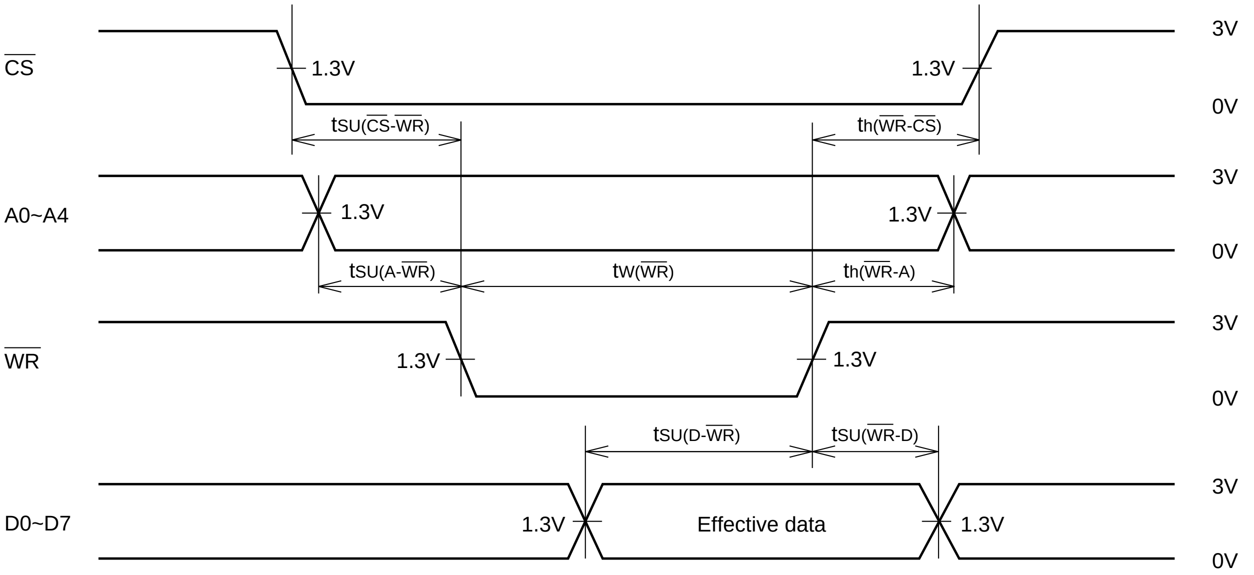


MPU INTERFACE

1) Timing for read operation (M66335 → MPU)

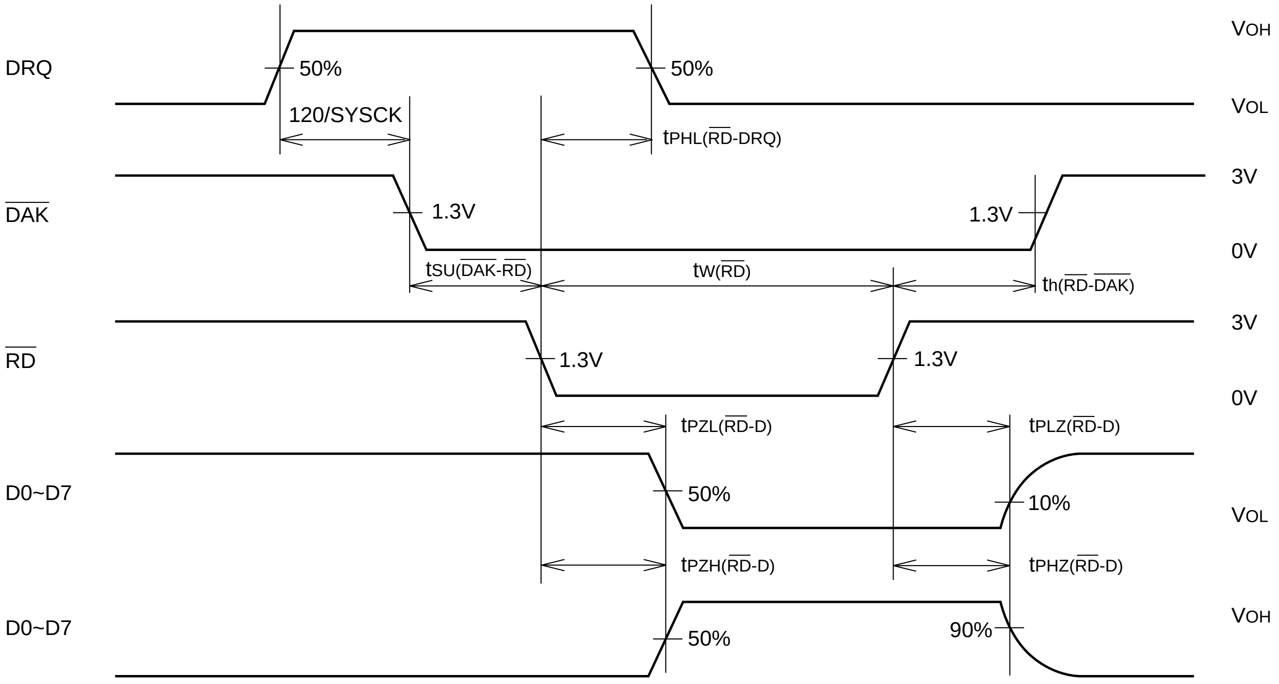


2) Timing for write operation (MPU → M66335)

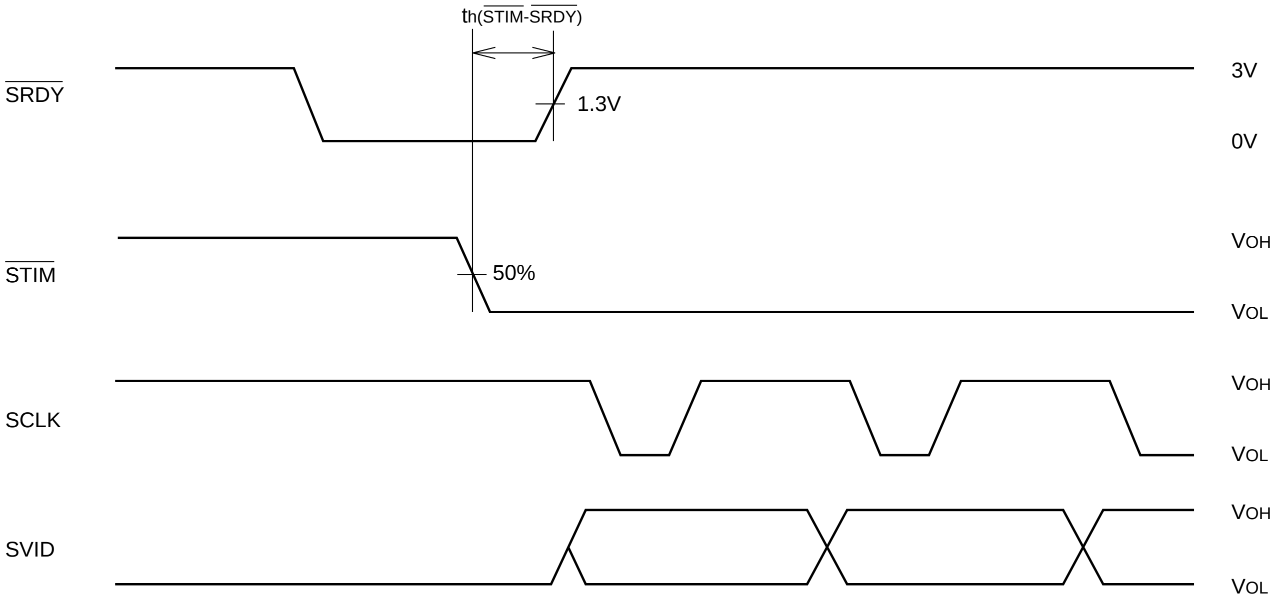


DMA TIMING

Timing for read operation (M66335 → system bus)



Timing of CODEC

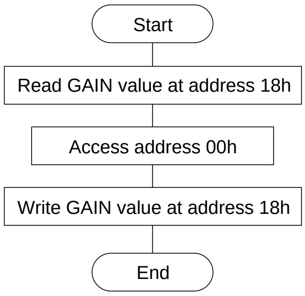


Cautions for Use

(1) Access to Address 00h

To gain access to address 00h, the value of built-in GCC (gain control counter) may be set to FFh.

This requires to read GAIN value at address 18h before access to address 00h and write the GAIN value at address 18h after the access (see Flowchart A).



Flowchart A. Address 00h Access Flow

(2) Reset

The M66335FP adopts the two types of reset. These reset functions are provided in Table A.

Table A. Reset functions

Function Reset type	Register initialization	Internal F/F initialization	GCC initialization
Hardware reset ($\overline{\text{RESET}}$)	○	○	○
Software reset register 0 (RESET)		○	○