Integrated Device Technology, Inc.

# 3.3V CMOS OCTAL TRANSPARENT LATCHES

**IDT54/74FCT3573/A**
**ADVANCE INFORMATION**

## FEATURES:

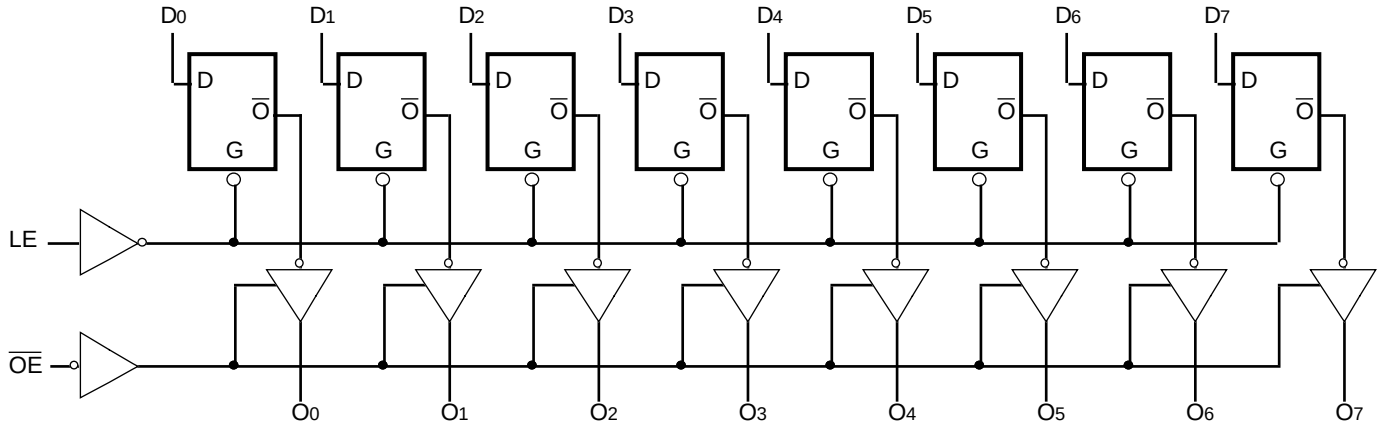
- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP Packages
- Extended commercial range of -40°C to +85°C
- $V_{CC}$ = 3.3V ±0.3V, Normal Range or $V_{CC}$ = 2.7V to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

The FCT3573/A are octal transparent latches built using an advanced dual metal CMOS technology.

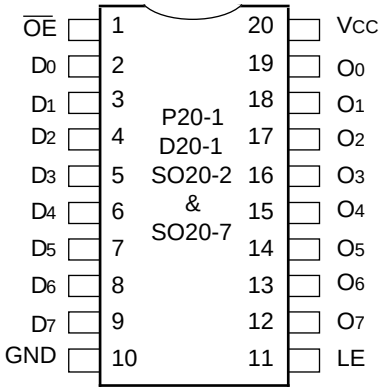
These octal latches have 3-state outputs and are intended for bus oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high-impedance state.

## FUNCTIONAL BLOCK DIAGRAM




3093 drw 01

## PIN CONFIGURATION




**DIP/SOIC/SSOP**
**TOP VIEW**

3093 drw 02

## FUNCTION TABLE (1)

| Inputs | | | Outputs |
|---|---|---|---|
| $D_N$ | LE | $\overline{OE}$ | $O_N$ |
| H | H | L | H |
| L | H | L | L |
| X | X | H | Z |

3093 tbl 02

**NOTE:**
1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level
   Z = High Impedance

## DEFINITION OF FUNCTIONAL TERMS

| Pin Names | Description |
|---|---|
| $D_N$ | Data Inputs |
| LE | Latch Enable Input (Active HIGH) |
| $\overline{OE}$ | Output Enable Input (Active LOW) |
| $O_N$ | 3-State Outputs |
| $\overline{O}_N$ | Complementary 3-State Outputs |

3093 tbl 03

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Rating | Commercial | Military | Unit |
|---|---|---|---|---|
| $V_{TERM}$(2) | Terminal Voltage with Respect to GND | –0.5 to +4.6 | –0.5 to +4.6 | V |
| $V_{TERM}$(3) | Terminal Voltage with Respect to GND | –0.5 to +7.0 | –0.5 to +7.0 | V |
| $V_{TERM}$(4) | Terminal Voltage with Respect to GND | –0.5 to $V_{CC}$ + 0.5 | –0.5 to $V_{CC}$ + 0.5 | V |
| $T_A$ | Operating Temperature | –40 to +85 | –55 to +125 | °C |
| $T_{BIAS}$ | Temperature Under Bias | –55 to +125 | –65 to +135 | °C |
| $T_{STG}$ | Storage Temperature | –55 to +125 | –65 to +150 | °C |
| $P_T$ | Power Dissipation | 1.0 | 1.0 | W |
| $I_{OUT}$ | DC Output Current | –60 to +60 | –60 to +60 | mA |

**NOTES:** 3093 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

## CAPACITANCE ($T_A$ = +25°C, f = 1.0MHz)

| Symbol | Parameter(1) | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 3.5 | 6.0 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 4.0 | 8.0 | pF |

**NOTE:** 3093 lnk 04

1. This parameter is measured at characterization but not tested.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: $T_A$ = –40°C to +85°C, $V_{CC}$ = 2.7V to 3.6V; Military: $T_A$ = –55°C to +125°C, $V_{CC}$ = 2.7V to 3.6V

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Level (Input pins) | Guaranteed Logic HIGH Level | | 2.0 | — | 5.5 | V |
| | Input HIGH Level (I/O pins) | | | 2.0 | — | $V_{CC}$+0.5 | |
| $V_{IL}$ | Input LOW Level (Input and I/O pins) | Guaranteed Logic LOW Level | | –0.5 | — | 0.8 | V |
| $I_{IH}$ | Input HIGH Current (Input pins)[6] | $V_{CC}$ = Max. | $V_I$ = 5.5V | — | — | ±1 | µA |
| | Input HIGH Current (I/O pins)[6] | | $V_I$ = $V_{CC}$ | — | — | ±1 | |
| $I_{IL}$ | Input LOW Current (Input pins)[6] | | $V_I$ = GND | — | — | ±1 | |
| | Input LOW Current (I/O pins)[6] | | $V_I$ = GND | — | — | ±1 | |
| $I_{OZH}$ | High Impedance Output Current | $V_{CC}$ = Max. | $V_O$ = $V_{CC}$ | — | — | ±1 | µA |
| $I_{OZL}$ | (3-State Output pins)[6] | | $V_O$ = GND | — | — | ±1 | |
| $V_{IK}$ | Clamp Diode Voltage | $V_{CC}$ = Min., $I_{IN}$ = –18mA | | — | –0.7 | –1.2 | V |
| $I_{ODH}$ | Output HIGH Current | $V_{CC}$ = 3.3V, $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $V_O$ = 1.5V[3] | | –36 | –60 | –110 | mA |
| $I_{ODL}$ | Output LOW Current | $V_{CC}$ = 3.3V, $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $V_O$ = 1.5V[3] | | 50 | 90 | 200 | mA |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min. | $I_{OH}$ = –0.1mA | $V_{CC}$–0.2 | — | — | V |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –3mA | 2.4 | 3.0 | — | |
| | | $V_{CC}$ = 3.0V, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –6mA MIL. $I_{OH}$ = –8mA COM'L. | 2.4[5] | 3.0 | — | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min. | $I_{OL}$ = 0.1mA | — | — | 0.2 | V |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 16mA | — | 0.2 | 0.4 | |
| | | | $I_{OL}$ = 24mA | — | 0.3 | 0.55 | |
| | | $V_{CC}$ = 3.0V, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 24mA | — | 0.3 | 0.50 | |
| $I_{OS}$ | Short Circuit Current[4] | $V_{CC}$ = Max., $V_O$ = GND[3] | | –60 | –135 | –240 | mA |
| $V_H$ | Input Hysteresis | — | | — | 150 | — | mV |
| $I_{CCL}$ $I_{CCH}$ | Quiescent Power Supply Current | $V_{CC}$ = Max., $V_{IN}$ = GND or $V_{CC}$ | COM'L. | — | 0.1 | 10 | µA |
| $I_{CCZ}$ | | | MIL. | — | 0.1 | 100 | |

**NOTES:**

3093 lnk 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. $V_{OH}$ = $V_{CC}$ –0.6V at rated current.
6. The test limits for this parameter is ± 5µA at $T_A$ = –55°C.

## POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $\Delta I_{CC}$ | Quiescent Power Supply Current | $V_{CC}$ = Max. | $V_{IN} = V_{CC} - 0.6V$[3] | | | | µA |
| $I_{CCD}$ | Dynamic Power Supply Current[4] | $V_{CC}$ = Max.<br>Outputs Open<br>$\overline{OE}$ = GND<br>One Input Toggling<br>50% Duty Cycle | $V_{IN} = V_{CC}$<br>$V_{IN}$ = GND | | | | µA/ MHz |
| $I_C$ | Total Power Supply Current[6] | $V_{CC}$ = Max.<br>Outputs Open<br>fi =10MHz | $V_{IN} = V_{CC}$<br>$V_{IN}$ = GND | | | | mA |
| | | 50% Duty Cycle<br>$\overline{OE}$ = GND<br>LE = VCC<br>One Bit Toggling | $V_{IN} = V_{CC} - 0.6V$<br>$V_{IN}$ = GND | | | | |
| | | $V_{CC}$ = Max.<br>Outputs Open<br>fi = 2.5MHz | $V_{IN} = V_{CC}$<br>$V_{IN}$ = GND | | | | |
| | | 50% Duty Cycle<br>$\overline{OE}$ = GND<br>LE = $V_{CC}$<br>Eight Bits Toggling | $V_{IN} = V_{CC} - 0.6V$<br>$V_{IN}$ = GND | | | | |

**NOTES:** 3093 tbl 06

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC}$ = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at $V_{CC}$ or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the $I_{CC}$ formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   $I_{CC}$ = Quiescent Current ($I_{CCL}$, $I_{CCH}$ and $I_{CCZ}$)
   $\Delta I_{CC}$ = Power Supply Current for a TTL High Input
   $D_H$ = Duty Cycle for TTL Inputs High
   $N_T$ = Number of TTL Inputs at $D_H$
   $I_{CCD}$ = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   $f_{CP}$ = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   $N_{CP}$ = Number of Clock Inputs at $f_{CP}$
   $f_i$ = Input Frequency
   $N_i$ = Number of Inputs at $f_i$

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE[3]

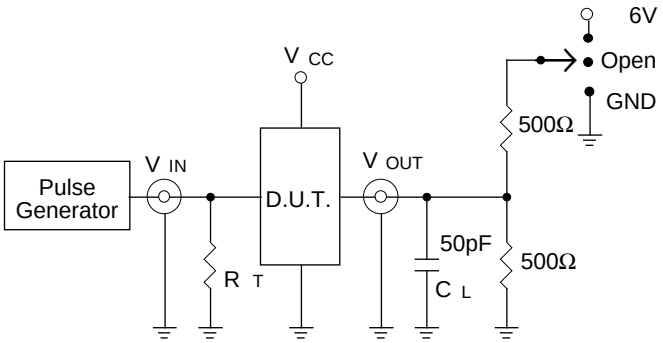
| | | | FCT3573 | | | | FCT3573A | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Com'l. | | Mil. | | Com'l. | | Mil. | | |
| Symbol | Parameter | Conditions[1] | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | Unit |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$D_N$ to $O_N$ | $C_L$ = 50pF<br>$R_L$ = 500Ω | 1.5 | 8.0 | 1.5 | 8.5 | 1.5 | 5.2 | 1.5 | 5.6 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>LE to $O_N$ | | 2.0 | 13.0 | 2.0 | 15.0 | 2.0 | 8.5 | 2.0 | 9.8 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time | | 1.5 | 12.0 | 1.5 | 13.5 | 1.5 | 6.5 | 1.5 | 7.5 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable Time | | 1.5 | 7.5 | 1.5 | 10.0 | 1.5 | 5.5 | 1.5 | 6.5 | ns |
| $t_{SU}$ | Set-up Time HIGH or LOW, $D_N$ to LE | | 2.0 | — | 2.0 | — | 2.0 | — | 2.0 | — | ns |
| $t_H$ | Hold Time HIGH or LOW, $D_N$ to LE | | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| $t_W$ | LE Pulse Width HIGH | | 6.0 | — | 6.0 | — | 5.0 | — | 6.0 | — | ns |

3093 tbl 07

**NOTES:**
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Propagation Delays and Enable/Disable times are with $V_{CC}$ = 3.3V ±0.3V, Normal Range. For $V_{CC}$ = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

# TEST CIRCUITS AND WAVEFORMS

## TEST CIRCUITS FOR ALL OUTPUTS




3093 drw 03

## SWITCH POSITION

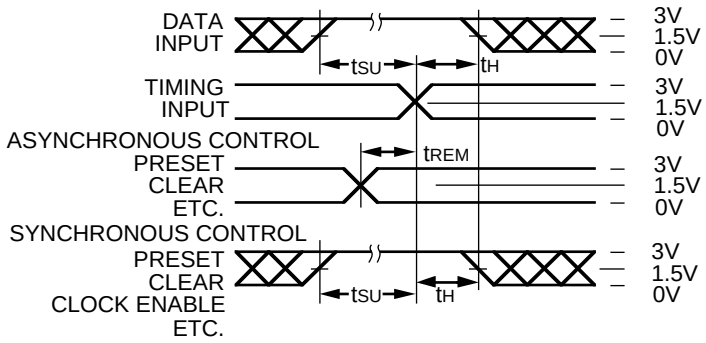
| Test | Switch |
|---|---|
| Open Drain<br>Disable Low<br>Enable Low | 6V |
| Disable High<br>Enable High | GND |
| All Other tests | Open |

3093 lnk 08

**DEFINITIONS:**

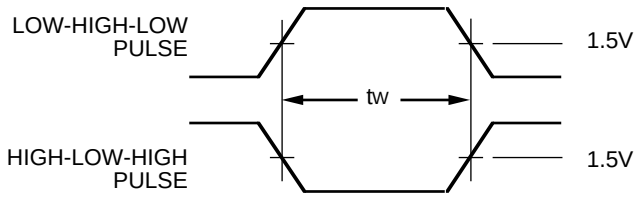
$C_L$= Load capacitance: includes jig and probe capacitance.
$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.

## SET-UP, HOLD AND RELEASE TIMES



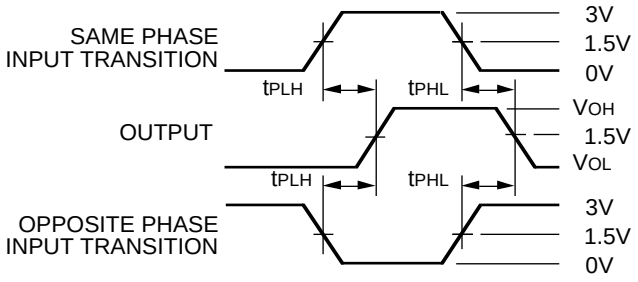

3093 drw 04

## PULSE WIDTH



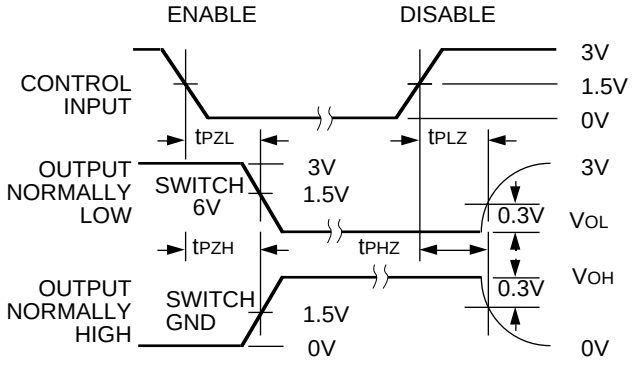

3093 drw 05

## PROPAGATION DELAY




3093 drw 06

## ENABLE AND DISABLE TIMES

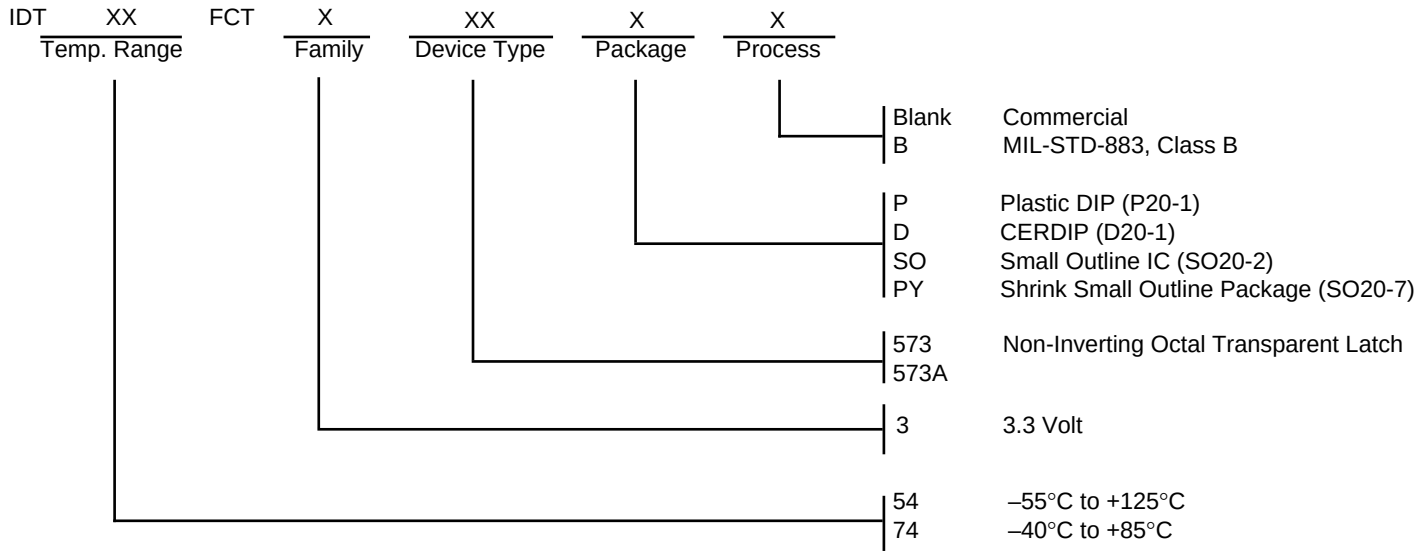



3093 drw 07

**NOTES:**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $t_F$ ≤ 2.5ns; $t_R$ ≤ 2.5ns.
3. If $V_{CC}$ is below 3V, input voltage swings should be adjusted not to exceed $V_{CC}$.

## ORDERING INFORMATION




3093 drw 08