HN62W4416N Series

1048576-word × 16-bit/2097152-word × 8-bit CMOS Mask Programmable ROM

HITACHI

ADE-203-468 (Z)
Preliminary
Rev. 0.0
Nov. 20, 1995

Description

The HN62W4416N is a 16-Mbit CMOS mask-Programmable ROM organized either as 1048576 words by 16 bits or 2097152 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. And a high speed access of 150 ns (max) is the most suitable to the system using a high speed micro-computer by 16 bits.

Feature

- Low voltage operation Mask ROM
  Single 3.3 V supply
- High speed
  Normal access time: 150 ns (max)
  Page access time: 50 ns (max)
- Low power
  Active: 252 mW (max)
  Standby: 108 µW (max)
- Byte-wide or word-wide data organization (Switched by BHE terminal)
- 4 word page access on word-wide mode
- 8 byte page access on byte-wide mode
- Three-state data output for or-tying
- Directly LVTTL compatible
  All inputs and outputs

Ordering Information

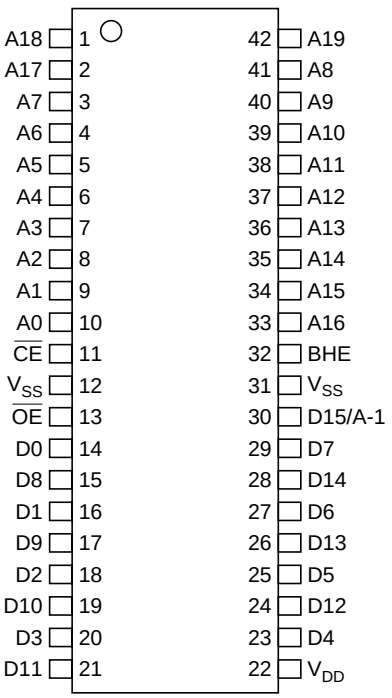
Type No.	Access time	Package
HN62W4416NP-15	150 ns	600 mil 42-pin plastic DIP (DP-42)
HN62W4416NFB-15	150 ns	600 mil 44-pin plastic SOP (FP-44D)
HN62W4416NTT-15	150 ns	400 mil 44-pin plastic TSOP II (TTP-44D)

Preliminary: This document contains information on a product. Specifications and information contained herein are subject to change without notice.

Hitachi semiconductor

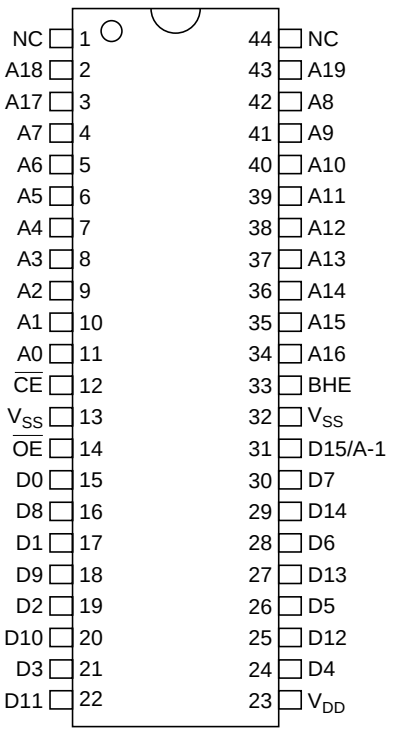
Pin Arrangement

HN62W4416NP Series



(Top View)

HN62W4416NFB Series
HN62W4416NTT Series

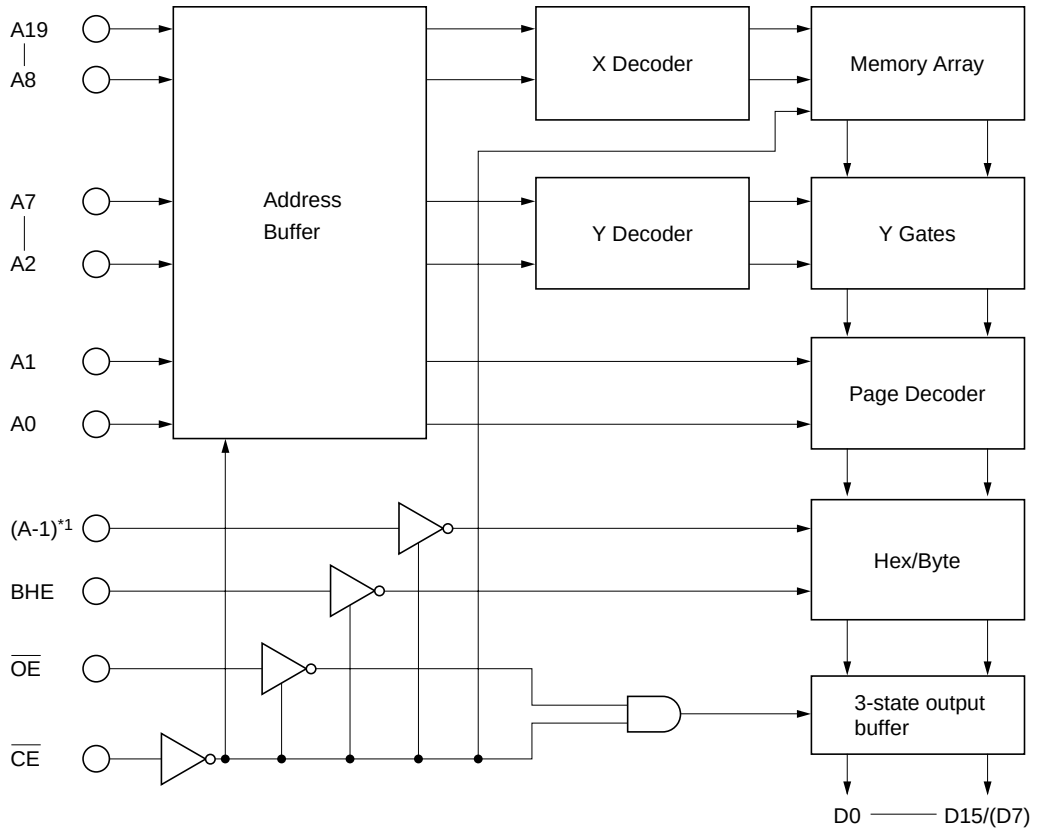


(Top View)

Pin Description

Pin name	Function
A2 to A19	Address inputs
D0 to D15	Data outputs
BHE	8/16 bit (byte/word) mode switch
A-1, A0 , A1	Page address inputs
BHE	8/16 bit (byte/word) mode switch
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
NC	No connection
V_{DD}	Power supply
V_{SS}	Ground

Block Diagram



$BHE = V_{IH}$: 16-bit (D15 to D0)
$BHE = V_{IL}$: 8-bit (D7 to D0)

Note : 1. A-1 is least significant address.
When BHE is 'low', D14 to D8 goes the high impedance state, and D15 should be A-1.

Mode Selection

	Pin				Data output		Address input	
Mode	**$\overline{CE}$**	**$\overline{OE}$**	**BHE**	**D15/A-1**	**D0-D7**	**D8-D15**	**LSB**	**MSB**
Standby	H	×*1	×	×	High-Z*2	High-Z	—	—
Output disable	L	H	×	×	High-Z	High-Z	—	—
Read (16-bit)	L	L	H	Dout	D0 to D7	D8 to D15	A0	A19
Read (8-bit)	L	L	L	L	D0 to D7	High-Z	A-1	A19
Read (8-bit)	L	L	L	H	D8 to D15	High-Z	A-1	A19

Notes: 1. ×: Don't care.
2. High-Z: High impedance

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage[*1]	V_{DD}	–0.3 to +5.5	V
All input and output voltage[*1]	Vin, Vout	–0.3 to V_{DD} + 0.3	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C
Temperature under bias	Tbias	–20 to +85	°C

Note: 1. With respect to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	V_{DD} + 0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Characteristics (V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = 0 to + 70°C)

Parameter		Symbol	Min	Max	Unit	Test conditions
Supply current	Active	I_{DD}	—	70	mA	V_{DD} = 3.6 V, I_{DOUT} = 0 mA, t_{RC} = 150 ns
	Standby	I_{SB1}	—	30	µA	V_{DD} = 3.6 V, $\overline{CE} \geq V_{DD} - 0.2$ V
	Standby	I_{SB2}	—	3	mA	V_{DD} = 3.6 V, $\overline{CE} \geq$ 2.2 V
Input leakage current		$\|I_{IL}\|$	—	10	µA	Vin = 0 to V_{DD}
Output leakage current		$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, Vout = 0 to V_{DD}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –2.0 mA
		V_{OL}	—	0.4	V	I_{OL} = 2.0 mA

Capacitance (V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance[*1]	Cin	—	10	pF
Output capacitance[*1]	Cout	—	15	pF

Note: 1. This parameter is sampled and not 100% tested. D15/A-1 pin is output.

AC Characteristics (V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = 0 to + 70°C)

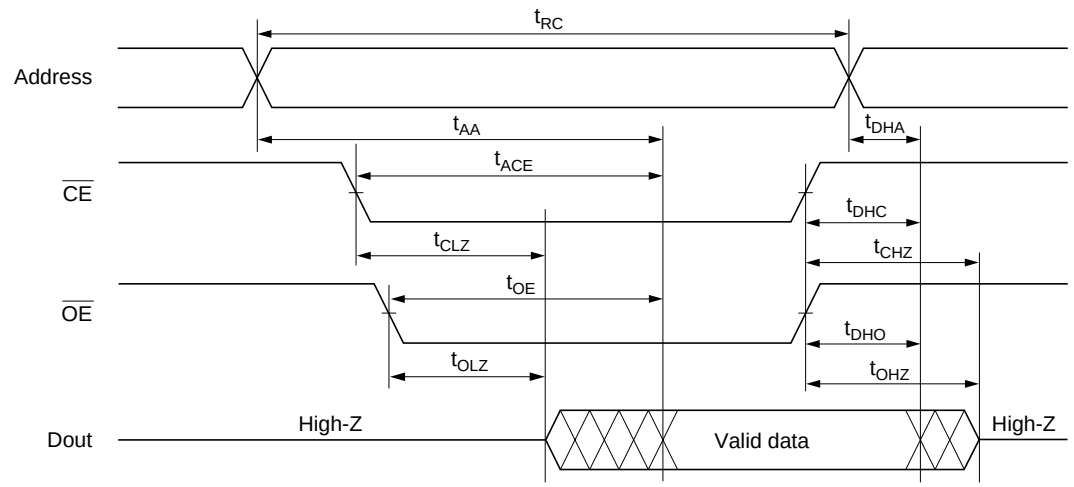
- Output load: 1TTL + C_L = 100 pF (including jig)
- Input pulse level: 0.4 to 2.4 V
- Input and output timing reference level: 1.4 V
- Input rise and fall time: 5 ns

		HN62W4416N-15			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Note**
Read cycle time	t_{RC}	150	—	ns	
Page read cycle time	t_{PC}	50	—	ns	
Address access time	t_{AA}	—	150	ns	
Page address access time	t_{PA}	—	50	ns	
$\overline{CE}$ access time	t_{ACE}	—	150	ns	
$\overline{OE}$ access time	t_{OE}	—	50	ns	
BHE access time	t_{BHE}	—	150	ns	
Output hold time from address change	t_{DHA}	5	—	ns	
Output hold time from $\overline{CE}$	t_{DHC}	0	—	ns	
Output hold time from $\overline{OE}$	t_{DHO}	0	—	ns	
Output hold time from BHE	t_{DHB}	0	—	ns	
$\overline{CE}$ to output in high-Z	t_{CHZ}	—	50	ns	1
$\overline{OE}$ to output in high-Z	t_{OHZ}	—	50	ns	1
BHE to output in high-Z	t_{BHZ}	—	30	ns	1
$\overline{CE}$ to output in low-Z	t_{CLZ}	5	—	ns	
$\overline{OE}$ to output in low-Z	t_{OLZ}	5	—	ns	
BHE to output in low-Z	t_{BLZ}	5	—	ns	

Note: 1. t_{CHZ}, t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

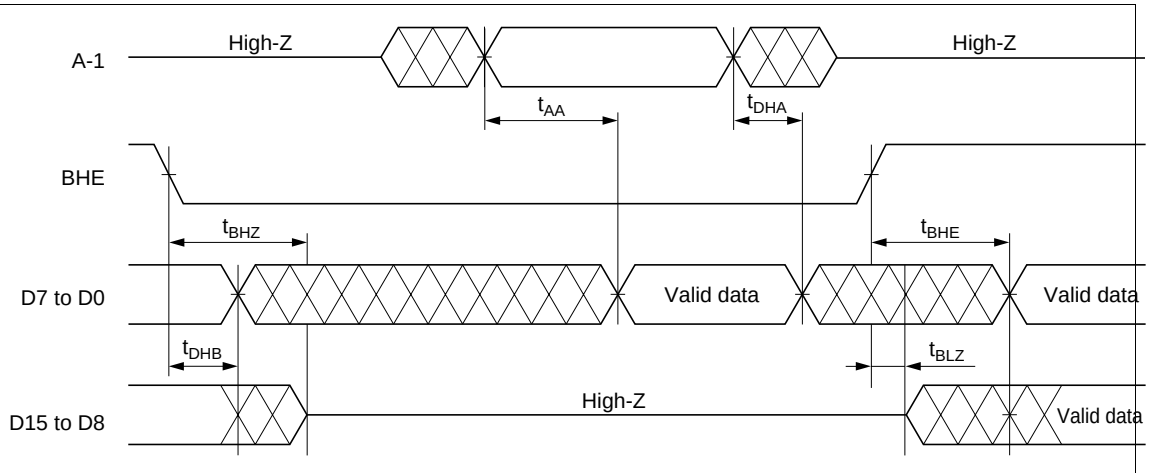
Timing Waveforms

Word Mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}')



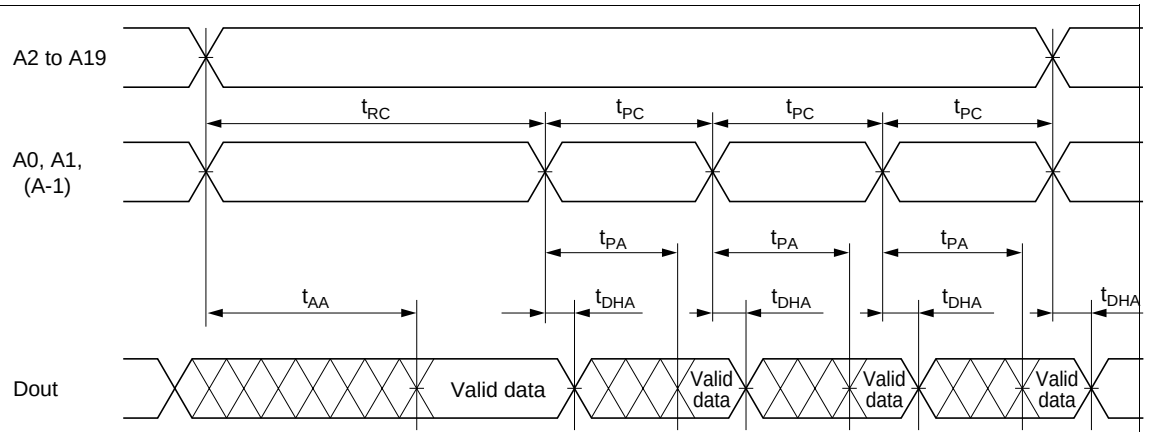
Notes : 1. t_{DHA}, t_{DHC}, t_{DHO} : Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE} : Determined by slower.
3. t_{CLZ}, t_{OLZ} : Determined by slower.

Word Mode, Byte Mode Switch



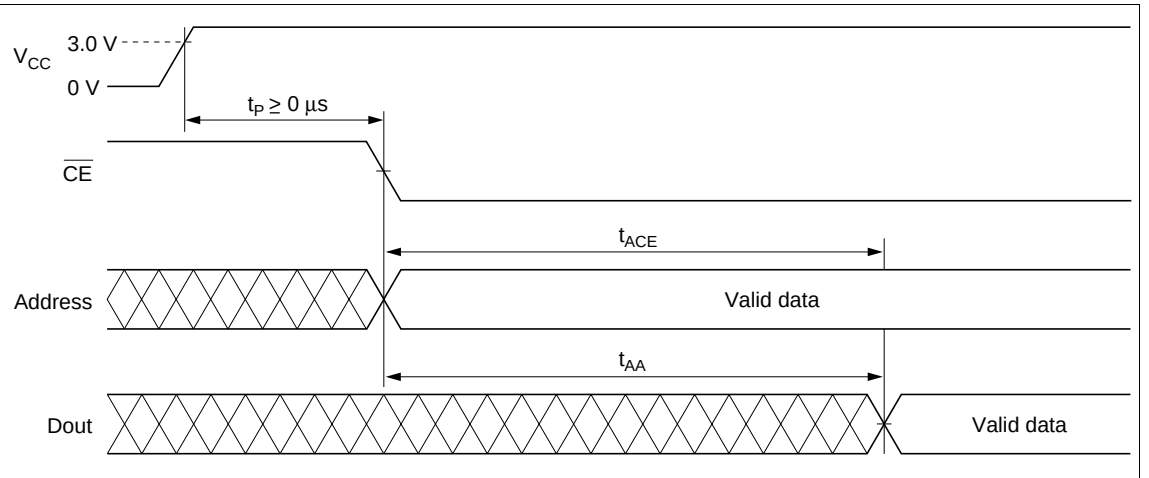
Notes : 1. $\overline{CE}$ and $\overline{OE}$ are enable, A19 to A0 are valid.
2. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable.
Therefore, the input signals of opposite phase to the output must not be applied to them.

Page mode



Notes : 1. Page address is determined as below.
Word mode (BHE = 'High') : A0, A1.
Byte mode (BHE = 'Low') : A-1, A0, A1
2. $\overline{CE}$ and $\overline{OE}$ are eneble.

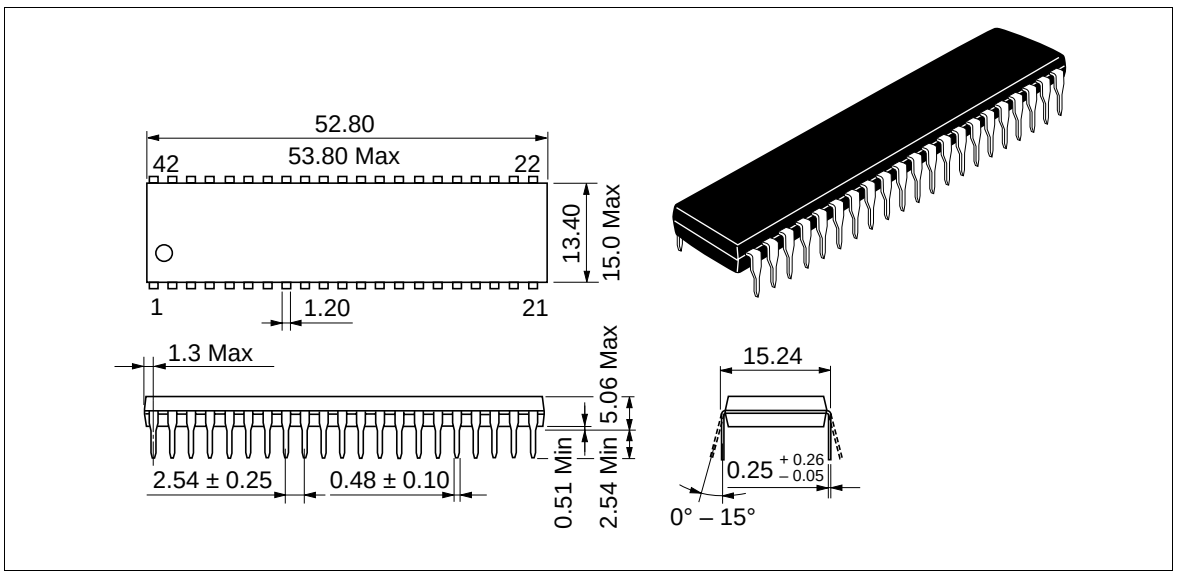
Power Up Sequence



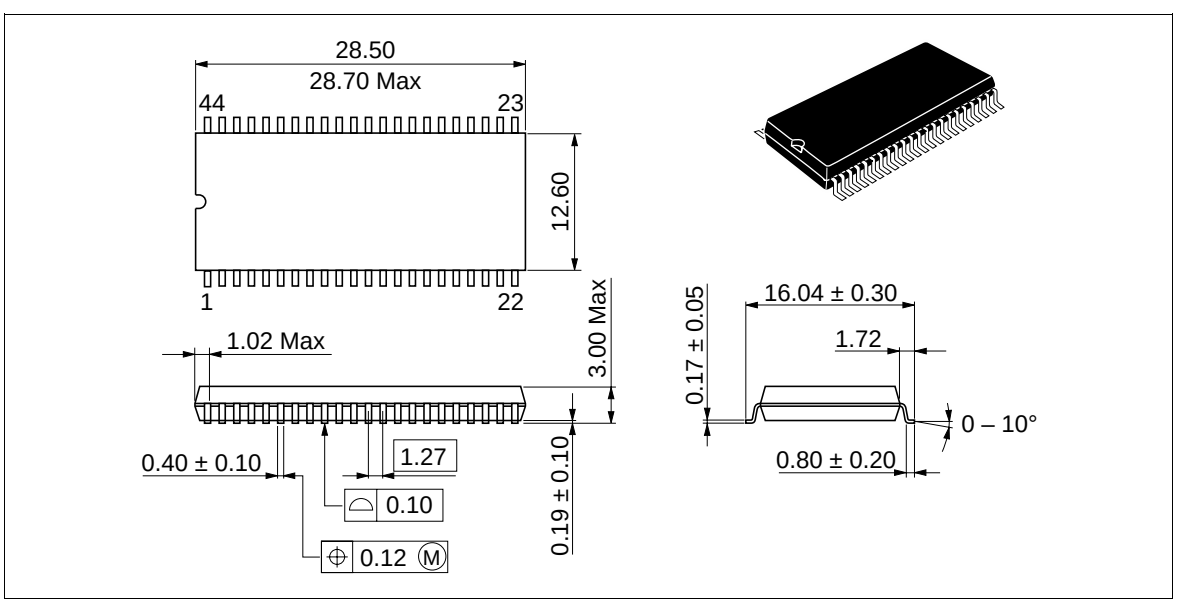
Note : 1. This device is used ATD (Address Transition Detecter). Therefore, transfer either $\overline{CE}$ or address (A19 to A2) after power up to 3.0 V.

Package Dimensions

HN62W4416P Series (DP-42) Unit: mm



HN62W4416FB Series (FP-44D) Unit: mm



Package Dimensions (cont)

HN62W4416TT Series (TTP-44D) Unit: mm