CA3097
T-43-25

Thyristor/Transistor Array

For Military, Commercial, and Industrial Applications

Features:

- *Complete isolation between elements*
- *n-p-n transistor - V_{CEO} = 30 V (min.) I_C = 100 mA (max.)*
- *p-n-p/n-p-n transistor pair - beta ≥ 8000 (typ.) @ I_C = 10 mA, individual p-n-p, n-p-n, or transistor pair operation*
- *Programmable unijunction transistor [PUT] - peak-point current = 15 nA (typ.) at R_G = 1 MΩ; V_{AK} = ± 30 V*
- *(PUT) Extremely long RC time constants with low value of external capacitor*
- *Sensitive-gate silicon controlled rectifier (SCR) - 150 mA forward current (max.)*
- *Zener-diode impedance (Z_Z) = 15Ω (typ.) at 10 mA*

RCA-CA3097E* Thyristor/Transistor Array is a monolithic integrated circuit that enables circuit designers to further integrate control systems. The CA3097E consists of five independent and completely isolated elements on one chip: an n-p-n transistor, a p-n-p/n-p-n transistor pair, a zener diode, a programmable unijunction transistor (PUT), and a sensitive-gate silicon controlled rectifier (SCR).

The CA3097 is supplied in either the 16-lead dual-in-line plastic package ("E" suffix) or the chip version ("H" suffix), and operates over the full military-temperature range of −55 to +125° C.

*Formerly Dev. No. TA6281.

Applications:

- *Timers*
- *Light dimmers/motor controls*
- *Oscillators*
- *"One-shot" multivibrators*
- *Voltage regulators*
- *Comparators, Schmitt triggers*
- *Constant-current sources*
- *Amplifiers*
- *Logic circuits*
- *SCR triggering*
- *Pulse circuits*

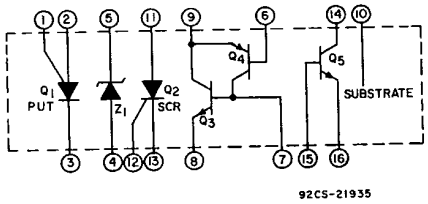

Fig. 1 — Schematic diagram of CA3097E.

File Number **633**

CA3097

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

Isolation Voltage, any terminal to substrate*	+50 V
Dissipation, Total Package:	
Up to $T_A = 55^oC$	750 mW
Above $T_A = 55^oC$	derate linearly at 6.67 mW/°C
Ambient Temperature Range:	
Operating	−55 to +125°C
Storage	−65 to +150°C
Lead Temperature (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265 °C
Each n-p-n Transistor (Q3,Q5)	
The following ratings apply with terminals 6 & 9 connected together.	
Collector-to-Emitter Voltage (V_{CEO})	30 V
Collector-to-Base Voltage (V_{CBO})	50 V
Emitter-to-Base Voltage (V_{EBO})	5 V
Collector Current (I_C)	100 mA
Base Current (I_B)	20 mA
Dissipation (P_D)	500 mW
p-n-p Transistor (Q4)	
The following ratings apply with terminals 7 & 8 connected together.	
Collector-to-Emitter Voltage (V_{CEO})	−40 V
Collector-to-Base Voltage (V_{CBO})	−50 V
Emitter-to-Base Voltage (V_{EBO})	−40 V
Collector Current (I_C)	−10 mA
Base Current (I_B)	−3 mA
Dissipation (P_D)	200 mW
p-n-p/n-p-n Transistor Pair (Q3,Q4)	
Dissipation (P_D)	500 mW
Programmable Unijunction Transistor, PUT (Q1)	
Gate-to-Cathode Positive Voltage (V_{GK})	30 V
Gate-to-Cathode Negative Voltage (V_{GKR})	5 V
Gate-to-Anode Negative Voltage (V_{GA})	30 V
Anode-to-Cathode Voltage (V_{AK})	±30 V
DC Anode Current	150 mA
Peak Anode Non-Recurrent Forward (On-State) Current (10 μs pulse)	2 A
Total Average Dissipation	300 mW
Silicon Controlled Rectifier, SCR (Q2)	
Repetitive Peak Reverse Voltage (V_{RRXM}), R_{GK} = 1 KΩ	30 V
Repetitive Peak Off-State Voltage (V_{DRXM}), R_{GK} = 1 kΩ	30 V
DC On-State Current (I_{TDC})	150 mA
Peak Surge (Non-Repetitive) On-State Current (10 μs pulse)	2 A
Forward Peak Gate Current (I_{GFM})	20 mA
Peak Gate-to-Cathode Reverse Voltage (V_{GRM})	5 V
Total Average Dissipation	300 mW
Zener Diode, (Z1)	
DC Current (I_Z)	25 mA
Dissipation (P_D)	250 mW

* One or more of the terminals of each element of the CA3097E is isolated from the substrate by a junction diode. In order to maintain electrical isolation between elements, the substrate terminal must be connected to a voltage which is no more positive than that of any other terminal. To avoid undesirable coupling between elements, the substrate terminal (terminal 10) should be maintained at either dc or signal (ac) ground.

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ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS Ambient Temperature (T_A) = 25°C Unless Otherwise Specified	FIG. NO.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
n-p-n TRANSISTORS Q3, Q5 (TERMINALS 6 and 9 CONNECTED)							
COLLECTOR CUTOFF CURRENT	I_{CBO}	V_{CB} = 10 V, I_E = 0		–	–	1	μA
COLLECTOR CUTOFF CURRENT	I_{CEO}	V_{CE} = 10 V, I_B = 0		–	–	10	μA
COLLECTOR-TO-EMITTER BREAKDOWN VOLTAGE	$V_{(BR)CEO}$	I_C = 100μA, I_B = 0		30	–	–	V
COLLECTOR-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)CBO}$	I_C = 100μA, I_E = 0		50	–	–	V
COLLECTOR-TO-SUBSTRATE BREAKDOWN VOLTAGE	$V_{(BR)CIO}$	I_{CI} = 100μA, I_B = 0, I_E = 0		50	–	–	V
EMITTER-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)EBO}$	I_E = 100μA, I_C = 0		5	7.5	10	V
COLLECTOR-TO-EMITTER SATURATION VOLTAGE	$V_{CE}(SAT)$	I_C = 50mA, I_B = 5mA	5	–	–	0.65	V
		I_C = 10mA, I_B = 1 mA		–	0.10	–	
BASE-TO-EMITTER SATURATION VOLTAGE	$V_{BE}(SAT)$	I_C = 10mA, I_B = 1mA	2	–	0.76	–	V
BASE-TO-EMITTER VOLTAGE	V_{BE}	V_{CE} = 3V, I_C = 10mA	3	0.65	0.73	0.85	V
DC FORWARD-CURRENT TRANSFER RATIO	h_{FE}	V_{CE} = 3V, I_C = 10mA	4	100	130	–	
		V_{CE} = 3V, I_C = 50mA		80	120	–	
p-n-p TRANSISTOR Q4 (TERMINALS 7 and 8 CONNECTED)							
COLLECTOR CUTOFF CURRENT	I_{CBO}	V_{CB} = -10 V, I_E = 0		–	–	–1	μA
COLLECTOR CUTOFF CURRENT	I_{CEO}	V_{CE} = -10 V, I_B = 0		–	–	–10	μA
COLLECTOR-TO-EMITTER BREAKDOWN VOLTAGE	$V_{(BR)CEO}$	I_C = -100μA, I_B = 0		–40	–	–	V
COLLECTOR-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)CBO}$	I_C = -10μA, I_E = 0		–50	–	–	V
EMITTER-TO-SUBSTRATE BREAKDOWN VOLTAGE	$V_{(BR)EIO}$	I_{EI} = 10μA, I_B = 0, I_E = 0		–50	–	–	V
EMITTER-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)EBO}$	I_E = –10μA, I_C = 0		–40	–	–	V
COLLECTOR-TO-EMITTER SATURATION VOLTAGE	$V_{CE}(SAT)$	I_C = -1mA, I_B = -100μA	6	–	–	–0.33	V
BASE-TO-EMITTER SATURATION VOLTAGE	$V_{BE}(SAT)$	I_C = -1mA, I_B = –100μA	7	–	–0.7	–	V
BASE-TO-EMITTER VOLTAGE	V_{BE}	V_{CE} = -3 V, I_C = –100μA	8	–0.5	–0.6	–0.7	V
DC FORWARD-CURRENT TRANSFER RATIO	h_{FE}	V_{CE} = – 3 V, I_C = –100μA	9	30	60	–	
		V_{CE} = –3 V, I_C = –1 mA		40	–	–	
n-p-n/p-n-p TRANSISTOR PAIR Q3, Q4							
DC FORWARD-CURRENT TRANSFER RATIO	h_{FE}	V_{CE} (n-p-n) = 3V, I_C = 10mA	10	–	8000	–	
		V_{CE} (n-p-n) = 3V, I_C = 50mA	10	–	6500	–	

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ELECTRICAL CHARACTERISTICS (Cont'd.)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS Ambient Temperature (T_A) = 25°C Unless Otherwise Specified	FIG. NO.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
PROGRAMMABLE UNIJUNCTION TRANSISTOR (PUT), Q1							
OFFSET VOLTAGE	V_T*	V_S = 10V, R_G = 10kΩ	11,22[a]	0.2	–	0.7	V
		V_S = 10V, R_G = 1MΩ		0.2	–	0.7	
ANODE-TO-CATHODE ON-STATE VOLTAGE	V_F	I_F = 50mA	12	–	0.90	1.5	V
		I_F = 100mA		–	1	–	
PEAK OUTPUT VOLTAGE	V_{OM}	C = 0.22μF Anode Supply Voltage = 20V	13,23	–	10	–	V
PEAK-POINT CURRENT	I_P	V_S = 10V, R_G = 10kΩ	14,22[a]	–	0.55	1	μA
		V_S = 10V, R_G = 1MΩ	–	–	0.015	0.15	
VALLEY-POINT CURRENT	I_V	V_S = 10V, R_G = 10kΩ	17,15	4	40	–	μA
		V_S = 10V, R_G = 1MΩ	16	–	–	25	
GATE REVERSE CURRENT	I_{GAO}	V_S = 30V	22[c]	–	0.02	–	nA
GATE REVERSE CURRENT	I_{GKS}	Anode-To-Cathode Short, V_S, = 30V	22[d]	–	0.2	–	nA
OUTPUT PULSE RISE TIME	t_r	Anode-Supply Voltage = 20V C = 0.22 μF	23	–	60	–	ns
SILICON CONTROLLED RECTIFIER (SCR), Q2							
PEAK OFF-STATE CURRENT: FORWARD	I_{DXM}	V_{DRXM} = 30V, R_{GK} = 1kΩ	24	–	–	2	μA
REVERSE	I_{RXM}	V_{RRXM} = 30V, R_{GK} = 1kΩ	24	–	–	2	
FORWARD DC VOLTAGE DROP	V_T	I_T = 50 mA	18	–	0.90	1.5	V
GATE-TO-SOURCE TRIGGER CURRENT	I_{GS}	T_A = 25°C	26	–	33	100	μA
		T_A = −55°C	26	–	50	–	
DC GATE-TRIGGER VOLTAGE	V_{GT}	V_L = 10V, R_L = 100Ω	19	–	0.55	0.75	V
HOLDING CURRENT	I_{HO}	R_{GK} = 1kΩ	20,24	–	1.2	–	mA
CRITICAL RATE-OF-RISE OF OFF-STATE VOLTAGE	dv/dt	EXPONENTIAL RISE, R_{GK} = 1kΩ, V_{DRXM} = 30V	25	–	150	–	V/μs
GATE-CONTROLLED TURN-ON TIME	t_{gt}	See Fig. 33	33	–	50	–	ns
CIRCUIT-COMMUTATED TURN-OFF TIME	t_q	See Fig. 33	33	–	10	–	μs
ZENER DIODE, Z1							
ZENER VOLTAGE	V_Z	I_Z = 10mA	21	7.2	8	8.8	V
ZENER IMPEDANCE	Z_Z	I_Z = 10mA, f = 1kHz		–	15	25	Ω
ZENER VOLTAGE TEMPERATURE COEFFICIENT	$(\Delta V_Z/V_Z)/\Delta T$	I_Z = 10mA		–	+0.05	–	%/°C
	$\Delta V_Z/\Delta T$			–	+4	–	mV/°C
ZENER-TO-SUBSTRATE BREAKDOWN VOLTAGE	$V_{(BR)ZIO}$	I_Z = 100μA TERM. 5 TO SUBSTRATE		50	80	– –	V

* $V_T = V_P - V_S$ (Fig. 22)

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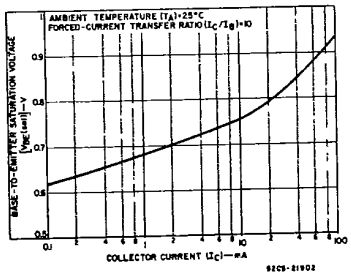

Fig. 2 – Base-to-emitter saturation voltage vs. collector current for n-p-n transistors Q3 & Q5.

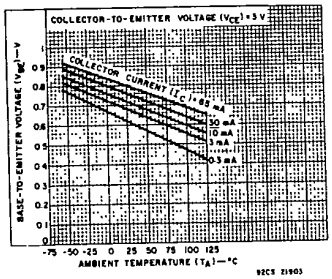

Fig. 3 – Base-to-emitter voltage vs. ambient temperature for n-p-n transistors Q3 & Q5.

TYPICAL CHARACTERISTICS

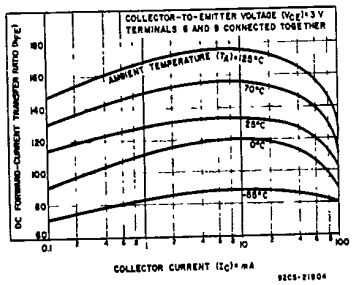

Fig. 4 – DC forward-current transfer ratio vs. collector current for n-p-n transistors Q3 & Q5.

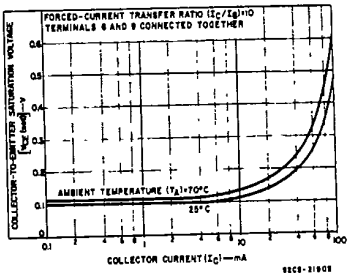

Fig. 5 – Collector-to-emitter saturation voltage vs. collector current for n-p-n transistors Q3 & Q5.

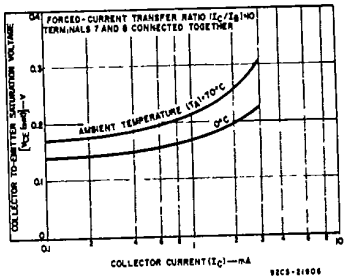

Fig. 6 – Collector-to-emitter saturation voltage vs. collector current for p-n-p transistor Q4.

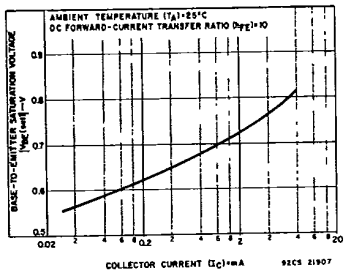

Fig. 7 – Base-to-emitter saturation voltage vs. collector current for p-n-p transistor Q4.

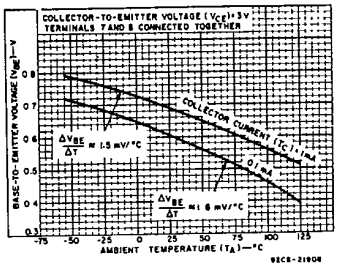

Fig. 8 – Base-to-emitter voltage vs. ambient temperature for p-n-p transistor Q4.

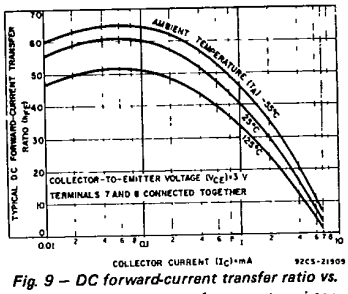

Fig. 9 – DC forward-current transfer ratio vs. collector current for p-n-p transistor Q4.

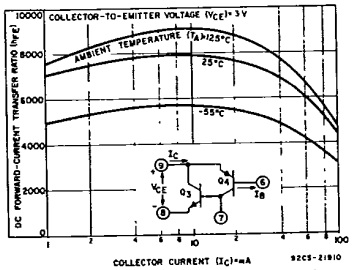

Fig. 10 – DC forward-current transfer ratio vs. collector current for transistor pair Q3, Q4.

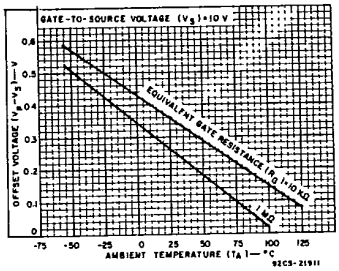

Fig. 11 – Offset voltage vs. ambient temperature for Q1 (PUT).

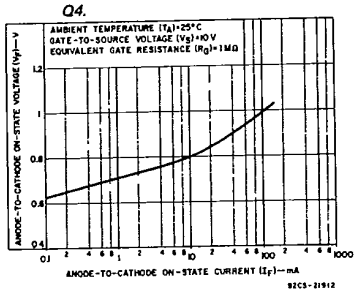

Fig. 12 – Anode-to-cathode on-state voltage vs. anode-to-cathode on-state current for Q1 (PUT).

TYPICAL CHARACTERISTICS (CONT'D)

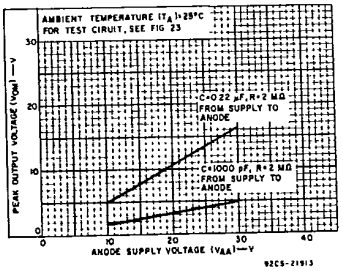

Fig. 13 – Peak output voltage vs. anode supply voltage for Q1 (PUT).

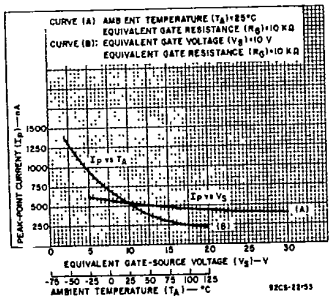

Fig.14 – Peak-point current vs. gate-source voltage and ambient temperature for Q1 (PUT).

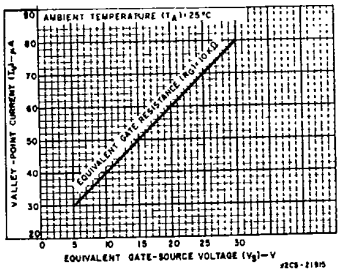

Fig.15 – Valley-point current vs. gate-source voltage for Q1 (PUT).

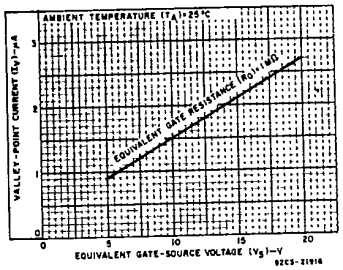

Fig.16 – Valley-point current vs. gate-source voltage for Q1 (PUT).

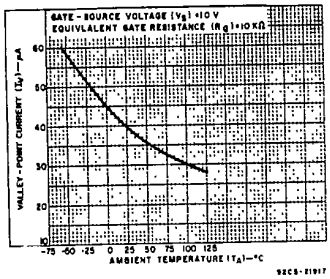

Fig. 17 – Valley-point current vs. ambient temperature for Q1 (PUT).

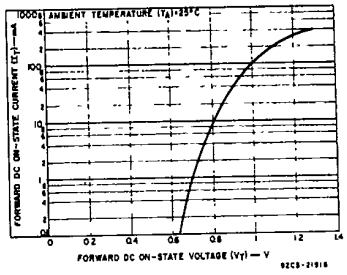

Fig. 18 – Forward DC on-state current vs. on-state voltage for Q2 (SCR).

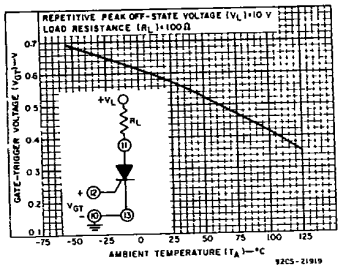

Fig. 19 – Gate-trigger voltage vs. ambient temperature for Q2 (SCR).

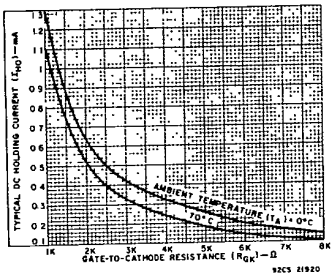

Fig. 20 – Typical DC holding current vs. gate-to-cathode resistance for Q2 (SCR).

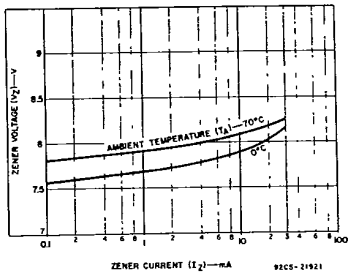

Fig. 21 – Zener voltage vs. zener current for Z1.

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OPERATING CONSIDERATIONS FOR CA3097

1. Composite p-n-p/n-p-n Transistors Q3, Q4 (See Fig. 3)

To use Q3 as an individual n-p-n transistor, join terminals no. 6 and no. 9 to disable p-n-p transistor Q4. .

The appropriate terminal connections are then:

Collector..... terminal 9
Base ..... terminal 7
Emitter..... terminal 8

To use Q4 as an individual p-n-p transistor, join terminals no. 7 and no. 8 to disable n-p-n transistor Q3.

The appropriate terminal connections are then:

Collector..... terminal 7
Base ..... terminal 6
Emitter..... terminal 9

To use Q3 and Q4 as a composite use terminals 6, 7, 8, and 9 as required.

2. Programmable Unijunction Transistor Q1 (PUT)

The programmable unijunction transistor is essentially an anode-gate SCR. The volt-ampere characteristic of the device is shown in Fig. 22. When an equivalent Thevenin source (V_S, R_G), as shown in Fig. 22, is applied to the gate terminal the device will be "off" if the anode-voltage is negative with respect to the gate voltage. Under this condition, any current flow is exclusively leakage current. When the anode voltage becomes more positive than the gate voltage by an increment equal to the threshold voltage (V_T = 0.4 V typ.), the device can turn "on" only if the current available at the anode terminal is greater than the specified peak-point current. The PUT will then switch through its negative-resistance region to the "on" state (low anode-to-gate voltage). It should be noted that I_P is not the maximum current allowed through the device, but is the current required at the peak of the V-I curve. I_P is typically a very low value of current.

After the PUT has switched to its low-impedance state, the device will remain "on" if the anode-current (I_A) exceeds the valley-point current (I_V). If $I_A < I_V$, the PUT will switch back to its high-impedance "off" state. Thus, the PUT can be made to "latch" or recover, depending on I_V. Since I_V is a function of the "on"-state gate current (which depends on R_G and V_S) a choice of R_G and/or V_S will determine the operating mode, i.e., "off" state→"on" state or "off" state → "on" state → "off" state. The value of I_V increases directly as a function of V_G and inversely with R_G. The PUT in the CA3097E has a low I_P.....I_P = 15 nA at V_S = 10 V, R_G = 1 MΩ. This low value of I_P indicates that an extremely large value of anode-supply resistor, e.g. 60 MΩ (typ.), can be used in timing circuits requiring long RC time constants. This becomes important when considering the size of the external

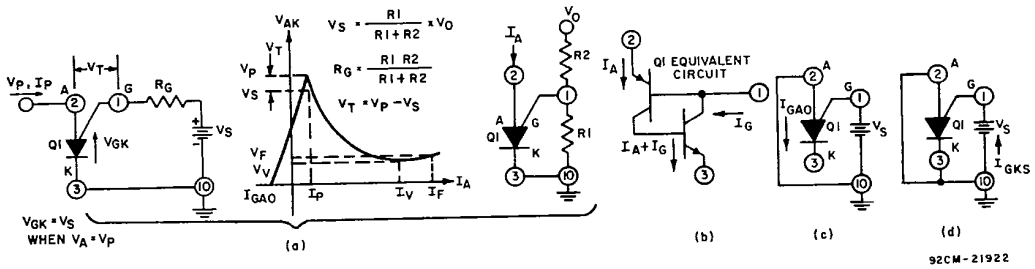


Fig. 22 – General anode characteristics for Q1 (PUT).

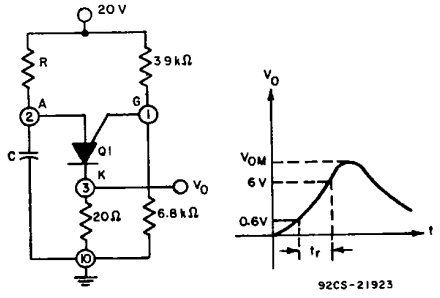


Fig. 23 – Output pulse characteristics for Q1 (PUT).

OPERATING CONSIDERATIONS (CONT'D)

timing capacitor to be used. Consequently, the use of the PUT in the CA3097E is advantageous since it has a lower I_P than most discrete PUT's.

Temperature Compensation of Switching Point

As described previously, the PUT will switch to its low-impedance state when its anode voltage is approximately a diode-drop above the gate voltage. Since the anode-to-gate threshold voltage vs. temperature characteristic is similar to that of a typical silicon-diode junction, a compensating series diode such as used in the circuit of Fig. 29 (Z1 connected as forward-biased diode) considerably reduces the effect of temperature on the switching point.

Bypassing Anode Current

If the PUT gate equivalent source is such that $I_A > I_V$, the PUT will remain "on". A method for turning the PUT off is by shunting current away from the anode until $I_A < I_V$. An example of this technique is the oscillator circuit of Fig. 29. Q3 transistor is turned "on" after the PUT fires and shunts current away from the anode, thereby forcing $I_A < I_V$. The PUT then turns "off" allowing C_T to recharge through R_T, to repeat the cycle.

Protecting The PUT Against Discharge Current Of The Capacitor

A current-limiting resistor in series with the PUT is normally required to dissipate capacitive discharge energy (see Figs. 23 and 29).

Silicon Controlled Rectifier, Q2 (SCR)

The SCR should be used with a 1 kΩ (or less) resistor connected between the cathode and gate terminals if the SCR is to be subjected to its maximum forward and reverse voltage ratings (V_{DXM} and V_{RXM}). Selecting a value for R_{GK} of 1 kΩ (or lower) increases the capability of the device to withstand greater dv/dt and increases the noise immunity of the SCR against false triggering at the gate. Practical considerations such as available current drive from the triggering devices (e.g., a PUT) will determine the lowest value of R_{GK} at which the SCR will fire with a $V_{GK} \approx 0.55$ V. With a value of 500Ω for R_{GK}, the trigger source must be capable of supplying 1.1 mA. R_{GK} should be non-inductive within the frequency band of the noise transients normally encountered in a particular application.

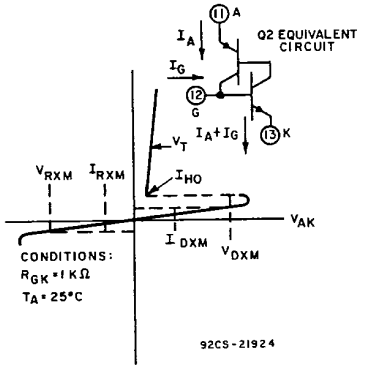


Fig. 24 – Principle voltage-current characteristics for Q2 (SCR).

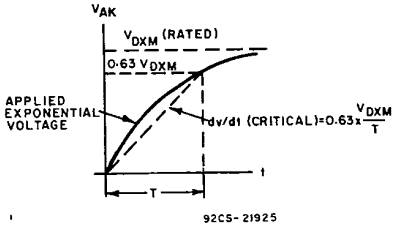
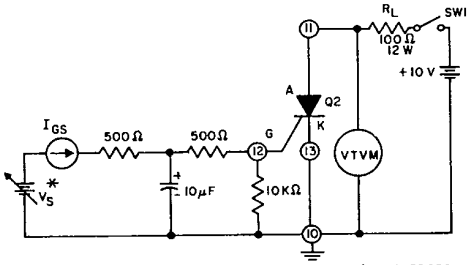


Fig. 25 – Definition of critical rate of rise of off-state voltage for Q2 (SCR).



WITH SW1 CLOSED, INCREASE V_S UNTIL SCR FIRES (VTVM DROPS FROM 10V TO APPROXIMATELY 1V). I_{GS} (TRIGGER) IS MEASURED JUST PRIOR TO THIS TRIGGERING POINT. NOTE THAT I_{GS} MAY DECREASE AS V_S IS INCREASED DUE TO CURRENT DRAWN OUT OF THE GATE TERMINAL OF THE SCR AS IT TURNS ON. TO UNLATCH THE SCR OPEN SW1.

* V_S SHOULD BE CAPABLE OF SUPPLYING MILLIVOLT INCREMENTS NEAR THE TRIGGER POINT

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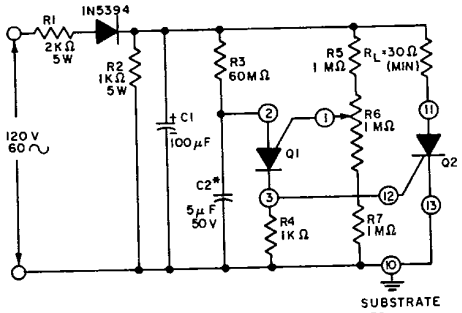
Fig. 26 – Test circuit for determining I_{GS} in Q2 (SCR).

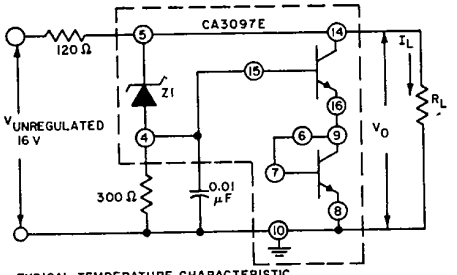
APPLICATIONS CIRCUITS



TIMING PERIOD ≈ 200 SEC WITH 1 MΩ POT CENTERED
TIMING CYCLE BEGINS WHEN AC IS APPLIED
* SPRAGUE TYPE 4308, 5 μF AT 50 V
SPRAGUE TYPE 6308, 5 μF AT 50 V
OR EQUIVALENT

92CS-21927

Fig. 27 – AC line-operated one-shot timer.



TYPICAL TEMPERATURE CHARACTERISTIC

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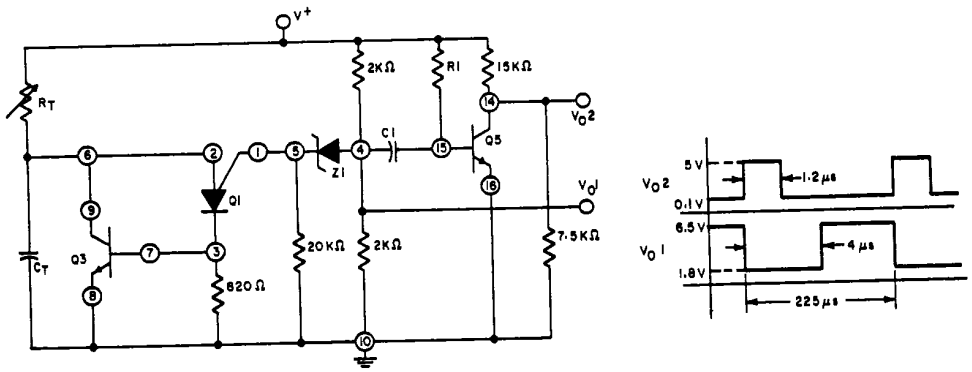
@ $R_L = 330\,\Omega$ $\frac{\Delta V_O/V_O}{\Delta T} \times 100 = \pm 0.01$ %/°C

TYP LOAD REGULATION @ $I_L = 0$ TO 40 mA, $(\Delta V_O/V_O) \times 100 = -3\%$ (NO LOAD TO FULL LOAD)

TYP. LINE REGULATION @ $R_L = 330\,\Omega$, $\frac{\Delta V_O/V_O}{\Delta V_{UNREG}} \times 100 = \pm 0.55\%/V$

Fig. 28 – Temperature-compensated shunt regulator.



PULSE RATE ADJUSTED BY VARYING R_T OR C_T
OUTPUT PULSE WIDTH ADJUSTED BY R_1C_1
DIFFERENTIATING TIME CONSTANT

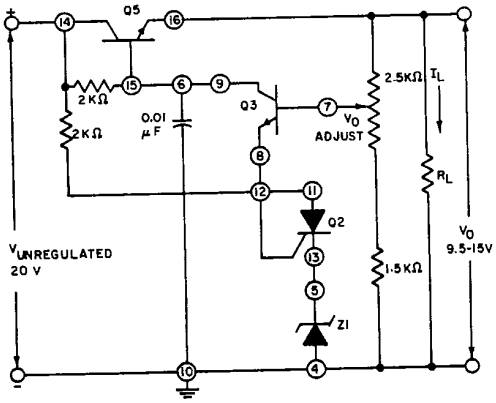
TYPICAL OPERATION FOR:
$V^+ = 15$ V, $C_T = 0.1\,\mu F$, $R_T = 4.3K\Omega$
$C_1 = 82$ pF, $R_1 = 60K\Omega$

92CM-21929

Fig. 29 – Pulse generator.

CA3097

APPLICATIONS CIRCUITS



TYPICAL LOAD REGULATION @ V_O = 12 V, I_L = 0 TO 40 mA

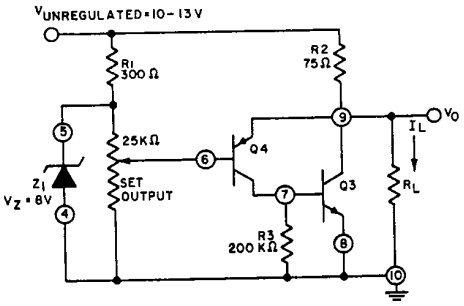
$\frac{\Delta V_O}{V_O} \times 100 = \pm 0.4\ \%$ (NO LOAD TO FULL LOAD)

TYPICAL LINE REGULATION @ V_O = 12 V

$\frac{\Delta V_O / V_O}{\Delta V_{UNREG}} \times 100 = \pm 0.45\ \%/V$

92CS-21930

Fig. 30 – Series voltage regulator.



TYPICAL LOAD REGULATION @ V_O = 7 V, I_L = 0 TO 40 mA

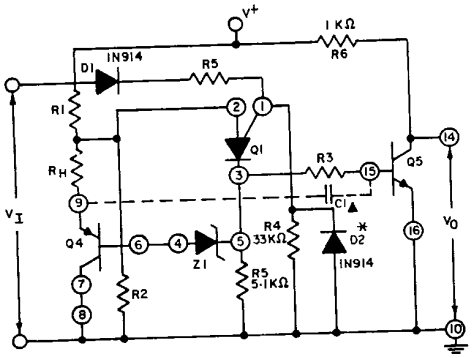
$\frac{\Delta V_O}{V_O} \times 100 = -1.1\ \%$

TYPICAL LINE REGULATION @ V_O = 7 V, I_L = 20 mA

$\frac{\frac{\Delta V_O}{V_O}}{\Delta V_{UNREGULATED}} = \pm 0.85\ \%$ / VOLT

92CS-21931

Fig. 31 – 5 to 7.5 V shunt regulator.



▲ OPTIONAL SPEED-UP CAPACITOR
* REQUIRED IF V_I SWINGS BELOW GROUND

TYPICAL OPERATING CONDITIONS:
FREQUENCY IN = 0–10 KHz
SUPPLY VOLTAGE (V^+) = 15 V
R1, R2, R_H = 5.1 KΩ
R3 = 6.2 KΩ, R_S = 300Ω
C_I = 820 pF
$V_{TH}U$ = 7.5 V, $V_{TH}L$ = 5 V
HYSTERESIS VOLTAGE = 2.5 V
UPPER THRESHOLD VOLTAGE $(V_{TH}U) \approx V^+ \frac{R2}{R1+R2}$

LOWER THRESHOLD VOLTAGE $(V_{TH}L) \approx \frac{(V^+)\left(\frac{R2\,R_H}{R2+R_H}\right)}{\frac{R2\,R_H}{R2+R_H} + R1}$

HYSTERESIS VOLTAGE = $V_{TH}U - V_{TH}L$

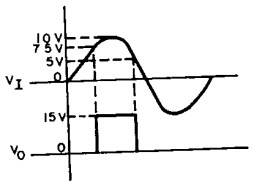


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Fig. 32 – Schmitt trigger.

CA3097

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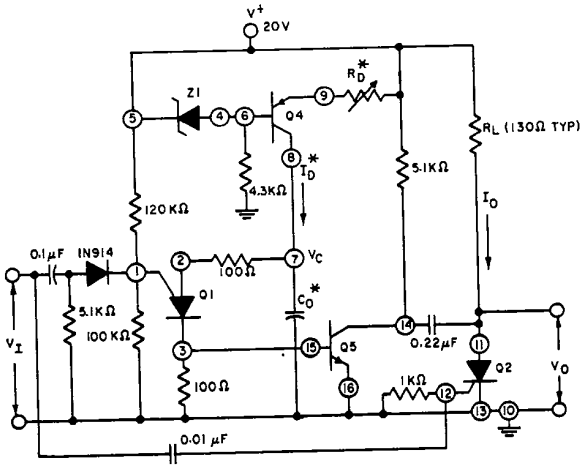
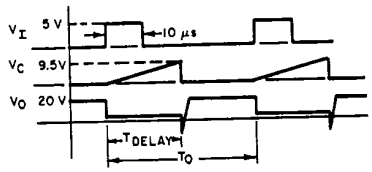
APPLICATIONS CIRCUITS (CONT'D)



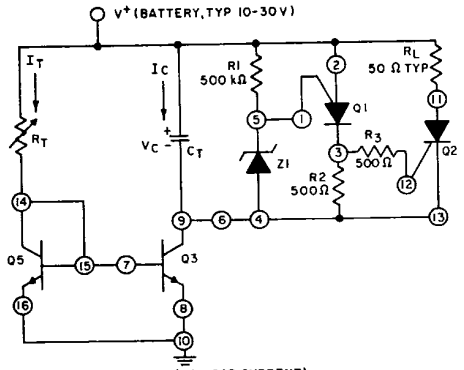


*MONOSTABLE DELAY TIME SET BY ADJUSTMENT OF I_D (VARY R_D) OR BY C_D. I_D MUST BE GREATER THAN I_V OF Q1 (PUT) FOR MONOSTABLE OPERATION.

Q2 (SCR) SWITCHING TIMES:
GATE-CONTROLLED TURN-ON TIME (t_{gt}) = 50 ns (TYP)
CIRCUIT-COMMUTATED TURN-OFF TIME (t_q) = 10 μs (TYP)

92CM-21933

Fig. 33 – Monostable multivibrator with variable delay.



T_{OFF} = TIMING PERIOD (NO LOAD CURRENT)
PUT FIRES WHEN $V_C \approx 8$ V

$V_C = \frac{I_C (T_{OFF})}{C_T}$, $I_C \approx I_T$ (Q3, Q5 MATCHED)

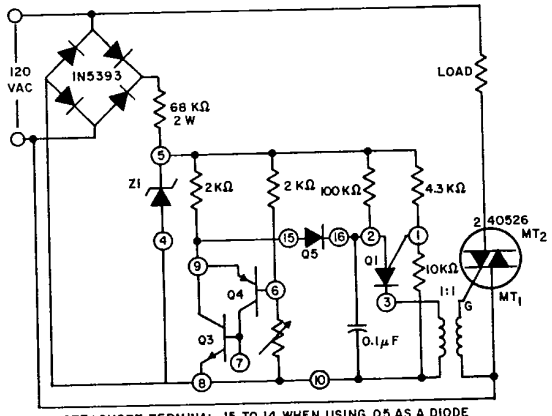
I_T SET BY ADJUSTING R_T, $I_T \approx \frac{V^+ - 0.7}{R_T}$

T_{ON} = CAPACITOR DISCHARGE TIME THROUGH LOAD. LOAD TURNS OFF WHEN SCR ANODE CURRENT FALLS BELOW HOLDING CURRENT (I_{HO}). TYPICAL $I_{HO} = 1.2$ mA

EXAMPLE: FOR TIMING PERIOD OF 8 3 MIN
$C_T = 1000\,\mu F$, $I_T = 16\,\mu A$
$R_T = \frac{V^+ - 0.7}{I_T}$ (FOR $V^+ = 16$ V, $R_T \approx 1M\Omega$)

92CS-21934

Fig.34 – Low-current-drain battery-operated long interval astable timer.



NOTE: SHORT TERMINAL 15 TO 14 WHEN USING Q5 AS A DIODE

92CS-22178

Fig.35 – Phase control circuit.