OV8610 Color CMOS SVGA (800 x 600) CAMERACHIP™

General Description

The OV8610 CMOS image sensor is a single-chip video/imaging camera device designed to provide a high level of functionality in a single, small-footprint package. The device incorporates an 800 x 600 image array capable of operating at up to 15 frames per second (fps) in full resolution. Proprietary sensor technology utilizes advanced algorithms to cancel Fixed Pattern Noise (FPN), eliminate smearing, and drastically reduce blooming. All required camera functions including exposure control, gamma, gain, white balance, color matrix, color saturation, hue control, windowing, and more, are programmable through the serial SCCB interface. The device can be programmed to provide image output in different 8-bit or 16-bit digital formats.

Features

- 480,000 pixels, 1/3" lens, SVGA/QSVGA format
- Data output formats include:
  - ITU-601
  - ITU-656
- Choice of progressive scan/interlaced read
- Wide dynamic range, anti-blooming, zero smearing
- Electronic exposure/gain/white balance control
- Image quality controls - brightness, contrast, gamma, saturation, sharpness, windowing, hue, etc.
- Internal and external synchronization
- Line exposure option
- 3.3-Volt operation, low power dissipation
  - < 30 mA active power at 30 fps with 10 mA load
  - < 10 µA in power-down mode
- Built in Gamma correction (0.45/1.00)
- SCCB programmable:
  - Color saturation, brightness, hue, white balance, exposure time, gain, etc.

Ordering Information

Product	Package
OV8610 (Color, SVGA, QSVGA, QQSVGA)	CLCC-48

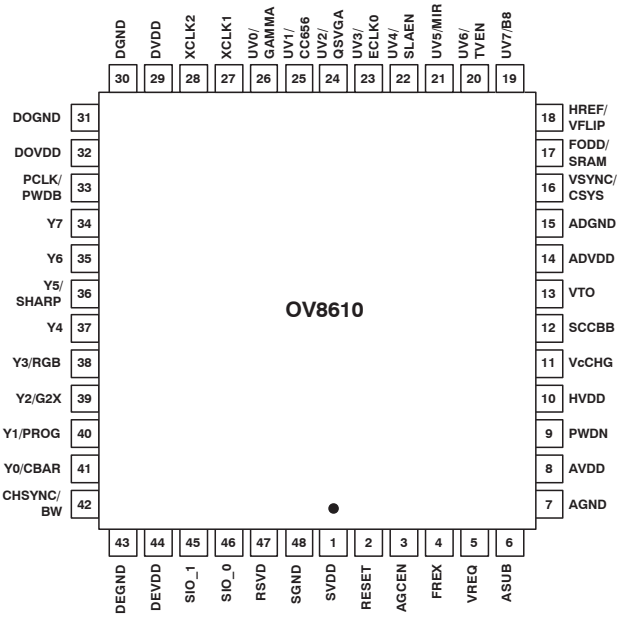
Applications

- Cellular phones
- Digital still cameras
- PC Multimedia
- PDAs
- Machine vision

Key Specifications

Array Size	**SVGA**	800 x 600
	QSVGA	400 x 300
Power Supply		3.0 - 3.6 VDC
Power Requirements	**Active**	< 30 mA (with 10 mA load)
	Standby	< 10 µA
Electronics Exposure		Up to 648:1 (for selected fps)
Output Format		10-bit digital raw RGB data
Lens Size		1/3"
Max. Image Transfer Rate	**SVGA**	15 fps
	QSVGA	30 fps
Min. Illumination (3000K)		< 3 lux @ f1.2
S/N Ratio		> 48 dB (AGC off,Gamma=1)
Dynamic Range		> 72 dB
Scan Mode		Progressive or Interlaced
Gamma Correction		On/Off 0.45/1.0
Pixel Size		6.2 µm x 6.2 µm
Dark Current		< 0.2 nA/cm^2
Fixed Pattern Noise		< 0.03% of $V_{PEAK-TO-PEAK}$
Image Area		4.96 mm x 3.72 mm
Package Dimensions		.560 in. x .560 in.

Figure 1 OV8610 Pin Diagram



Functional Description

Figure 2 shows the functional block diagram of the OV8610 image sensor. The OV8610 includes:

- Image Sensor Array (824 x 615 resolution)
- Analog Signal Processor
- Dual 10-Bit Analog-to-Digital Converters
- Digital Data Formatter
- Video Port
- SCCB Interface

Figure 2 Functional Block Diagram

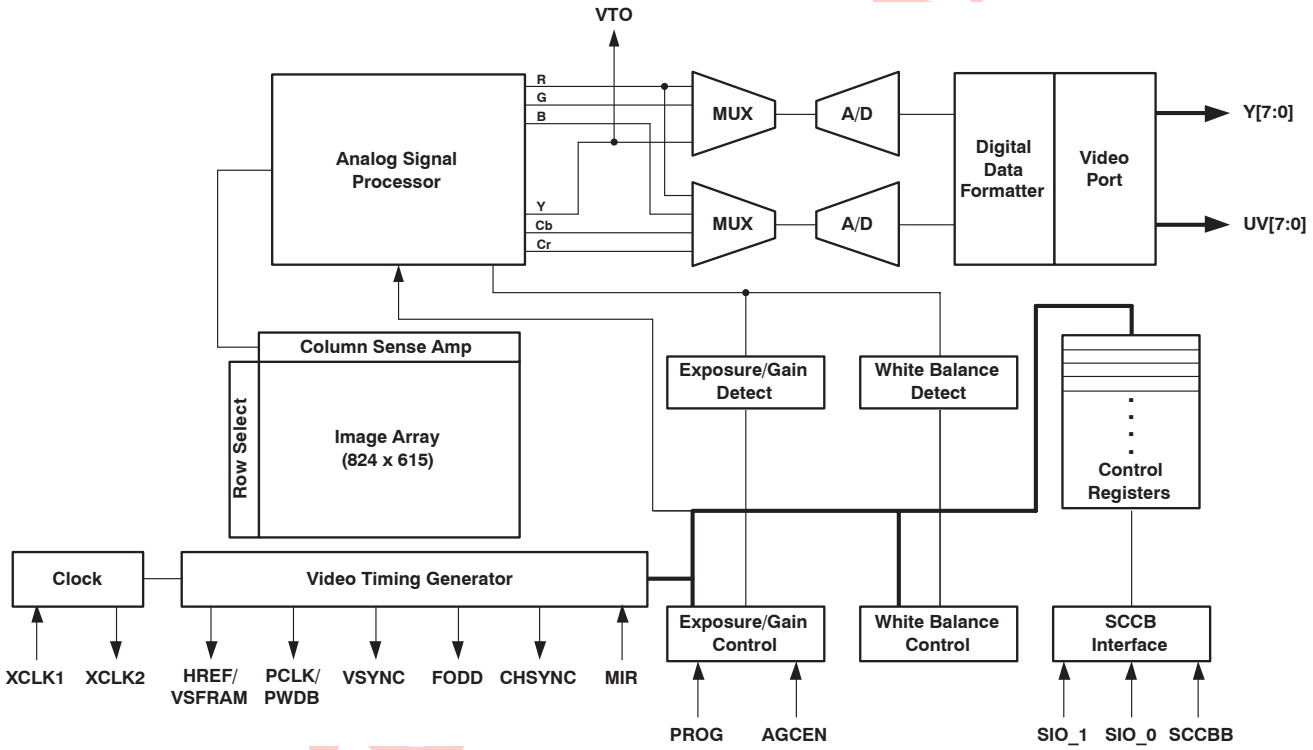


Image Sensor Array

The OV8610 sensor is a 1/3" CMOS imaging device. The sensor contains a total of 506,760 pixels (824 x 615). Its design is based on a field integration readout system with line-by-line transfer and an electronic rolling shutter with a synchronous pixel readout scheme. The color filter of the sensor consists of primary red, green, and blue filters arranged in the line-alternating Bayer pattern, RGRG/GBGB.

Analog Signal Processor

The image is captured by the 824 x 615 pixel image array and routed to the analog processing section where the majority of signal processing occurs. This block contains the circuitry that performs color separation, color correction, automatic gain control (AGC), gamma correction, color balance, black level calibration, aperture correction, controls for picture luminance and chrominance, and hue control for color. The analog video signals are based on the following formula:

Y = 0.59G + 0.31R + 0.11B
U = R - Y
V = B - Y

where R, G, B are the equivalent color components in each pixel.

YCbCr format is also supported, based on the following:

Y = 0.59G + 0.31R + 0.11B
Cr = 0.713 (R - Y)
Cb = 0.564 (B - Y)

Dual 10-Bit Analog-to-Digital Converters

The YCbCr or RGB data signal from the analog processing section is fed to two on-chip 10-bit analog-to-digital (A/D) converters: one for the Y/G channel and one shared by the CbCr/BR channels.

The on-chip 10-bit A/D operates at up to 20 MHz, and is fully synchronous to the pixel rate. Actual conversion rate is related to the frame rate. A/D black-level calibration circuitry ensures:

- Black level of Y/RGB is normalized to a value of 16
- Peak white level is limited to 240
- CbCr black level is 128
- CbCr Peak/bottom is 240/16
- RGB raw data output range is 16/240

NOTE: Values 0 and 255 are reserved for sync flag

Digital Data Formatter

The converted data stream is further conditioned in the digital formatter. The processed signal is delivered to the digital video port through the video multiplexer which routes the user-selected 8-, or 10-bit video data to the correct output pins.

Image Processing

The algorithm used for the electronic exposure control is based on the brightness of the full image. The exposure is optimized for a "normal" scene that assumes the subject is well lit relative to the background. In situations where the image is not well lit, the automatic exposure control (AEC) white/black ratio may be adjusted to suit the needs of the application.

Additional on-chip functions include:

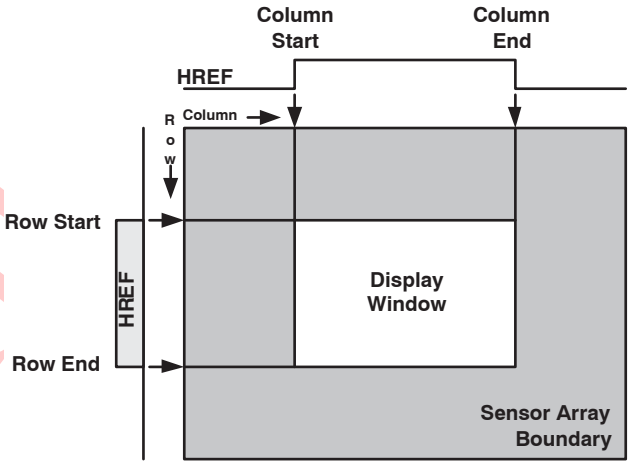
- AGC that provides a gain boost of up to 24 dB
- White balance control that enables setting of proper color temperature and can be programmed for automatic or manual operation.
- Separate saturation, brightness, hue, and sharpness adjustments allow for further fine-tuning of the picture quality and characteristics.

The OV8610 image sensor also provides control over the White Balance ratio for increasing/decreasing the image field Red/Blue component ratio. The sensor provides a default setting that may be sufficient for many applications.

Windowing

The windowing feature of the OV8610 image sensor allows user-definable window sizing as required by the application (see Figure 3). Window size setting (in pixels) ranges from 2 x 2 to 800 x 600, and can be positioned anywhere inside the 824 x 615 boundary. Note that modifying window size and/or position does not change frame or data rate. The OV8610 image sensor alters the assertion of the HREF signal to be consistent with the programmed horizontal and vertical region. The default output window is 800 x 600.

Figure 3 Windowing



Zoom Video (ZV)

The OV8610 image sensor includes a Zoom Video (ZV) function that supports standard ZV port interface timing. Signals available include VSYNC, CHSYNC, PCLK and 16-bit data bus: Y[7:0] and UV[7:0]. The rising edge of PCLK clocks data into the ZV port (see Figure 6).

QSVGA-Skip

A QSVGA mode is available for applications where higher resolution image capture is not required. Only half of the pixel rate is required when programmed in same frame rate with sub-sampling method. If retaining the same pixel rate with the skip method, the maximum frame rate is 120. Default resolution is 400 x 300 pixels and can be programmed for other resolutions. Refer to Table 6 and Table 7 for further information.

QQSVGA-Skip

A QQSVGA mode is available for further resolution decrease. Two methods are used to get this mode, sub-sampling and skip. Sub-sampling can get better quality than skip but skip can attain a higher frame rate. The maximum frame rate is 240 for QQSVGA and the default resolution is 200 x 150.

Video Port

The video output port of the OV8610 image sensor provides a number of output format/standard options to suit many different application requirements. Table 1 indicates the output formats available. These formats are user-programmable through the SCCB interface.

YUV Output

The OV8610 supports ITU-656 and ITU-601 output formats, providing VSYNC, HREF, and PCLK as standard output video timing signals.

ITU-601/ITU-656

The OV8610 image sensor supports both ITU-601 and ITU-656 output formats in the following configurations (see Table 3 and Figure 4 for further details):

16-bit, 4:2:2 Format

This mode complies with the 60/50 Hz ITU-601 timing standard (see Table 3).

8-bit data mode

In this mode, video information is output in Cb Y Cr Y order using the Y port only and running at twice the pixel rate during which the UV port is inactive (see Table 2).

The OV8610 image sensor provides VSYNC, HREF, PCLK, FODD, and CHSYNC as standard video timing signals.

In ITU-656 modes, the OV8610 image sensor asserts Start of Active Video (SAV) and End of Active Video (EAV) to indicate the beginning and ending of the HREF window. As a result, SAV and EAV change with the active pixel window.

The OV8610 image sensor offers flexibility in YUV output format. The device may be programmed to standard YUV 4:2:2. The device may also be configured to "swap" the UV sequence. When swapped, the UV channel output sequence in the 16-bit configuration becomes:

V U V U···

The 8-bit configuration becomes:

V Y U Y···.

The third format available in the 8-bit configuration is the Y/UV sequence swap:

Y U Y V···.

RGB Raw Data Output

The OV8610 image sensor can also be programmed to provide 8-bit RGB raw data output. The output sequence is matched to the OV8610 color filter pattern.

The video output appears in Y channel only and the UV channel is disabled in 8-bit RGB raw data. The output sequence is B G R G.

Table 1 Digital Output Formats

Resolution	Pixel Clock	800 x 600	400 x 300	200 x 150
YUV	16-bit	Y[a]	Y	Y
	8-bit	Y	Y	Y
	ITU-656	Y	Y	Y
RGB	16-bit	Y	Y	Y
	8-bit	Y	Y	Y
	ITU-656[b]	Y	Y	Y
Y/UV Swap[c]	16-bit			
	8-bit	Y	Y	Y
U/V Swap	YUV[d]	Y	Y	Y
	RGB[e]	Y	Y	Y
YG	16-bit	Y	Y	Y
	8-bit			
Single-Line RGB Raw Data	16-bit			
	8-bit	Y	Y	Y
MSB/LSB Swap		Y	Y	Y

a. "Y" indicates mode/combination is supported by the OV8610

b. Output is 8-bit in RGB ITU-656 format. SAV and EAV are inserted at the beginning and ending of HREF, which synchronizes the acquisition of VSYNC and HSYNC. 8-bit data bus configuration (without VSYNC and CHSYNC) can provide timing and data in this format.

c. Y/UV swap is valid in 8-bit format only. Y channel output sequence is Y U Y V.

d. U/V swap means UV channel output sequence swaps in YUV format (i.e., V U V U ... for 16-bit and V Y U Y ... for 8-bit).

e. U/V swap means neighbor row B R output sequence swaps in RGB format. Refer to RGB Raw Data Output for further details.

Table 2 4:2:2 8-bit Format

Data Bus	Pixel Byte Sequence							
Y7	U7	Y7	V7	Y7	U7	Y7	V7	Y7
Y6	U6	Y6	V6	Y6	U6	Y6	V6	Y6
Y5	U5	Y5	V5	Y5	U5	Y5	V5	Y5
Y4	U4	Y4	V4	Y4	U4	Y4	V4	Y4
Y3	U3	Y3	V3	Y3	U3	Y3	V3	Y3
Y2	U2	Y2	V2	Y2	U2	Y2	V2	Y2
Y1	U1	Y1	V1	Y1	U1	Y1	V1	Y1
Y0	U0	Y0	V0	Y0	U0	Y0	V0	Y0
Y Frame	0		1		2		3	
UV Frame	0 1				2 3			

Table 3 4:2:2 16-bit Format

Data Bus	Pixel Byte Sequence					
Y7	Y7	Y7	Y7	Y7	Y7	Y7
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y0	Y0	Y0	Y0	Y0	Y0	Y0
UV7	UV7	UV7	UV7	UV7	UV7	UV7
UV6	UV6	UV6	UV6	UV6	UV6	UV6
UV5	UV5	UV5	UV5	UV5	UV5	UV5
UV4	UV4	UV4	UV4	UV4	UV4	UV4
UV3	UV3	UV3	UV3	UV3	UV3	UV3
UV2	UV2	UV2	UV2	UV2	UV2	UV2
UV1	UV1	UV1	UV1	UV1	UV1	UV1
UV0	UV0	UV0	UV0	UV0	UV0	UV0
Y Frame	0	1	2	3	4	5
UV Frame	0 1		2 3		4 5	

Table 4 shows the default Y/UV channel output port relationship before an MSB/LSB swap.

Table 4 Default Output Sequence

	MSB							LSB
Output port	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
Internal output data	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

Table 5 and Table 6 shows the relationship after an MSB/LSB swap changes.

Table 5 Swapped MSB/LSB Output Sequence

	MSB							LSB
Output port	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
Internal output data	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7

Table 6 QSVGA Digital Output Format (YUV Beginning-of-Line)

Pixel No.	1	2	3	4	5	6	7	8
Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
UV	U0, V0	U1, V1	U2, V2	U3, V3	U4, V4	U5, V5	U6, V6	U7, V7

Y channel output U2Y2V3 Y3U6 Y6V7 Y7 U10Y10 V11Y11...
Every other pixel (total 400 pixels) and every other line (total 300 lines) is output in each frame.

The pixel pattern for the RGB raw data format is shown in Table 7.

Table 7 RGB Raw Data Format

R/C	1	2	3	4	. . .	821	822	823	824
1	$B_{1,1}$	$G_{1,2}$	$B_{1,3}$	$G_{1,4}$	. . .	$B_{1,821}$	$G_{1,822}$	$B_{1,823}$	$G_{1,824}$
2	$G_{2,1}$	$R_{2,2}$	$G_{2,3}$	$R_{2,4}$	. . .	$G_{2,821}$	$R_{2,822}$	$G_{2,823}$	$R_{2,824}$
3	$B_{3,1}$	$G_{3,2}$	$B_{3,3}$	$G_{3,4}$	. . .	$B_{3,821}$	$G_{3,822}$	$B_{3,823}$	$G_{3,824}$
4	$G_{4,1}$	$R_{4,2}$	$G_{4,3}$	$R_{4,4}$	. . .	$G_{4,821}$	$R_{4,822}$	$G_{4,823}$	$R_{4,824}$
613	$B_{613,1}$	$G_{613,2}$	$B_{613,3}$	$G_{613,4}$	. . .	$B_{613,821}$	$G_{613,822}$	$B_{613,823}$	$G_{613,824}$
614	$G_{614,1}$	$R_{614,2}$	$G_{614,3}$	$R_{614,4}$	. . .	$G_{614,821}$	$R_{614,822}$	$G_{614,823}$	$R_{614,824}$
615	$B_{615,1}$	$G_{615,2}$	$B_{615,3}$	$G_{615,4}$	. . .	$B_{615,821}$	$G_{615,822}$	$B_{615,823}$	$G_{615,824}$

- RGB full resolution progressive scan mode (total 614 HREFs)
  - First HREF Y channel output unstable data
  - Second HREF Y channel output $B_{11}G_{21}$ R_{22} G_{12} $B_{13}G_{23}$ R_{24} G_{14} . . .
  - Third HREF Y channel output B_{31} G_{21} R_{22} G_{32} B_{33} G_{23} R_{24} G_{34} . . .
  - Every line of data is output twice for each frame
  - PCLK is double
- RGB QSVGA resolution progressive scan mode (total 300 HREFs)
  - First HREF Y channel output $B_{11}G_{21}$ R_{22} G_{12} $B_{15}G_{25}$ R_{26} G_{16} . . .
  - Second HREF Y channel output $B_{31}G_{41}$ R_{42} G_{32} $B_{35}G_{45}$ R_{46} G_{36} . . .
  - Third HREF Y channel output B_{51} G_{61} R_{62} G_{52} B_{55} G_{65} R_{66} G_{56} . . .
  - Every line of data is output once for each frame
  - Maximum frame rate is 60 fps
- RGB full resolution raw data one line format (total 600 HREFs)
  - First HREF Y channel output B_{11} G_{12} B_{13} G_{14} . . .
  - Second HREF Y channel output G_{21} R_{22} G_{23} R_{24} . . .
  - Third HREF Y channel output B_{31} G_{32} B_{33} G_{34} . . .
  - PCLK rising edge latch data bus
- RGB QSVGA resolution raw data one line format (total 300 HREFs)
  - First HREF Y channel output B_{11} G_{12} B_{15} G_{16} . . .
  - Second HREF Y channel output G_{21} R_{22} G_{25} R_{26} . . .
  - Third HREF Y channel output B_{51} G_{52} B_{55} G_{56} . . .
  - Third HREF Y channel output G_{61} R_{62} G_{65} R_{66} . . .
  - PCLK rising edge latch data bus

Frame Exposure Mode

OV8610 supports frame exposure mode. In this mode, FREX (pin 4 - see “FREX” on page 9) is asserted by an external master device to set exposure time. The pixel array is quickly pre-charged when FREX is set to "1". OV8610 captures the image during the time period when FREX remains high. The video data stream is delivered to the output port in a line-by-line manner after FREX switches to "0".

It should be noted that FREX must remain high long enough to ensure the entire image array has been pre-charged.

When data is being output from OV8610, care must be taken so as not to expose the image array to light. This may affect the integrity of the image data captured. A mechanical shutter synchronized with the frame exposure rate can be used to minimize this situation. The timing of frame exposure mode is shown in Figure 7.

Reset

The OV8610 includes a RESET pin (pin 2 - see “RESET” on page 9) that forces a complete hardware reset when it is pulled high (VCC). The OV8610 clears all registers and resets to their default values when a hardware reset occurs. Reset can also be initiated through the SCCB interface.

Power-Down Mode

Two methods are available to place the OV8610 into power-down mode: hardware power-down and SCCB software power-down.

To initiate hardware power-down, the PWDN pin (pin 9 - see “PWDN” on page 9) must be tied to high (+3.3 VDC). When this occurs, the OV8610 internal device clock is halted and all internal counters are reset. The current draw is less than 10 µA in this standby mode.

Executing a software power-down through the SCCB interface suspends internal circuit activity, but does not halt the device clock. The current requirements drop to less than 1 mA in this mode.

SCCB Interface

The method to configure OV8610 is to use its on-chip SCCB register programming capability. The SCCB interface provides access to all of the device's programmable internal registers.

Pin Description

Table 8 Pin Description

Pin Number	Name	Pin Type	Function/Description
01	SVDD	V_{IN}	Array power (+3.3 VDC) - bypass to ground using a 0.1 µF capacitor
02	RESET	Function (default = 0)	Chip reset, active high. Resets all control registers to factory defaults.
03	AGCEN	Function (default = 0)	Automatic Gain Control (AGC) Selection 0: Disable AGC 1: Enable AGC ***Note:*** *This function is disabled when OV8610 sensor is configured in SCCB low mode. In SCCB low mode, this pin is an SCCB chip select.*
04	FREX	Function (default = 0)	Frame Exposure Control 0: Disables frame exposure control 1: Enables frame exposure control
05	VREQ	V_{REF} (1.5V)	Array reference - connect to ground using a 0.1 µF capacitor
06	ASUB	V_{IN}	Analog substrate voltage
07	AGND	V_{IN}	Analog ground
08	AVDD	V_{IN}	Analog power supply (+3.3 VDC) - bypass to ground using a 0.1 µF capacitor
09	PWDN	Function (default = 0)	Power-down Mode Selection 0: Operating mode 1: Power down mode
10	HVDD	V_{REF} (1.5V)	Charge pump out voltage. Doubler must be enabled.
11	VcCHG	V_{REF} (2.7V)	Internal voltage reference - bypass to ground using a 0.1 µF capacitor
12	SCCBB[a]	Function (default = 0)	SCCB Enable Selection 0: Selects internal register setting control and enables SCCB interface 1: Enables I/O input pin power on latch setting control
13	VTO	Output	CCIR analog composite signal output - for test purposes only
14	ADVDD	V_{IN}	Analog power supply (+3.3 VDC) - bypass to ground using a 0.1 µF capacitor
15	ADGND	V_{IN}	Analog signal ground
16	VSYNC/CSYS	Output	Vertical sync output. At power-up, read as CSYS.
17	FODD/SRAM	Output	Field ID FODD output. At power-up, read as SRAM.
18	HREF/VFLIP	Output	HREF output. At power-up, read as VFLIP.
19	UV7/B8[b]	Output	U video component output bit[7]. At power-up, sampled as B8.
20	UV6/TVEN[b]	Output	U video component output bit[6]. At power-up, sampled as TVEN.
21	UV5/MIR[b]	Output	U video component output bit[5]. At power-up, sampled as MIR.
22	UV4/SLAEN[b]	Output	U video component output bit[4]. At power-up, sampled as SLAEN.
23	UV3/ECLKO[b]	Output	U video component output bit[3]. At power-up, sampled as ECLKO.

Table 8 Pin Description (Continued)

Pin Number	Name	Pin Type	Function/Description
24	UV2/QSVGA[b]	Output	U video component output bit[2]. At power-up, sampled as QSVGA.
25	UV1/CC656[b]	Output	U video component output bit[1]. At power-up, sampled as CC656.
26	UV0/GAMMA[b]	Output	U video component output bit[0]. At power-up, sampled as GAMMA.
27	XCLK1	Input	Crystal clock input
28	XCLK2	Output	Crystal clock output
29	DVDD	V_{IN}	Digital power supply (+3.3 VDC) - bypass to ground using a 0.1 µF capacitor
30	DGND	V_{IN}	Digital ground
31	DOGND	V_{IN}	Digital interface output buffer ground
32	DOVDD	V_{IN}	Digital output buffer supply (+3.3 VDC) - bypass to ground using a 0.1 µF capacitor
33	PCLK/PWDB	Output	PCLK output. At power-up, sampled as charge pump enable.
34	Y7	Output	Y video component output bit[7]
35	Y6	Output	Y video component output bit[6]
36	Y5/SHARP	Output	Y video component output bit[5]. At power-up, sampled as SHARP.
37	Y4	Output	Y video component output bit[4]
38	Y3/RGB	Output	Y video component output bit[3]. At power-up, sampled as RGB.
39	Y2/G2X	Output	Y video component output bit[2]. At power-up, sampled as G2X.
40	Y1/PROG	Output	Y video component output bit[1]. At power-up, sampled as PROG.
41	Y0/CBAR	Output	Y video component output bit[0]. At power-up, sampled as CBAR.
42	CHSYNC/RSVD	Output	CHSYNC output.
43	DEGND	V_{IN}	Decoder ground
44	DEVDD	V_{IN}	Decoder power supply (+3.3 VDC) - bypass to ground using a 0.1 µF capacitor
45	SIO_1	Input	SCCB serial interface clock input
46	SIO_0	I/O	SCCB serial interface data I/O
47	RSVD	–	Reserved - DO NOT connect
48	SGND	V_{IN}	Array ground

a. All I/O latch input pins are effective only when pin 12 (SCCBB) is high. Otherwise, all pin functions are regulated by the register settings.

b. Output is not available in one-port mode.

Electrical Characteristics

Table 9 Operating Conditions

Parameter	Min	Max	Unit
Operating temperature	0	40	°C
Storage temperature	-40	125	°C
Operating humidity	TBD	TBD	
Storage humidity	TBD	TBD	

Table 10 DC Characteristics (0°C < T_A < 85°C, Voltages referenced to GND)

Symbol	Parameter	Min	Typ	Max	Unit
Supply					
V_{DD1}	Supply voltage (DEVDD, ADVDD, AVDD, DVDD, DOVDD)	3.0	3.3	3.6	V
I_{DD1}	Supply current (at 30 fps and 3.3 V digital I/O plus 1 TTL loading on 16-bit data bus)		30	35	mA
I_{DD2}	Standby supply current		8	10	µA
Digital Inputs					
V_{IL}	Input voltage LOW			0.8	V
V_{IH}	Input voltage HIGH	2			V
C_{IN}	Input capacitor			10	pF
Digital Outputs (standard loading 25 pF, 1.2 KΩ to 3 V)					
V_{OH}	Output voltage HIGH	2.4			V
V_{OL}	Output voltage LOW			0.6	V
SCCB Inputs					
V_{IL}	SIO_0 and SIO_1 (DOVDD = 5V)	-0.5		1.5	V
V_{IH}	SIO_0 and SIO_1 (DOVDD = 5V)	3.0	3.3	V_{DD} + 0.5	V
V_{IL}	SIO_0 and SIO_1 (DOVDD = 3V)	-0.5	0	1	V
V_{IH}	SIO_0 and SIO_1 (DOVDD = 3V)	2.5	3.3	V_{DD} + 0.5	V

Table 11 AC Characteristics (T_A = 25°C, V_{DD} = 3V)

Symbol	Parameter	Min	Typ	Max	Unit
RGB/YCbCr Output					
I_{SO}	Maximum sourcing current		15		mA
V_Y	DC level at zero signal		1.2		V
	Y_{PP} 100% amplitude (without sync)		1		V
	Sync amplitude		0.4		V
ADC Parameters					
B	Analog bandwidth		TBD		MHz
Φ_{DIFF}					
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		1		LSB

Table 12 Timing Characteristics

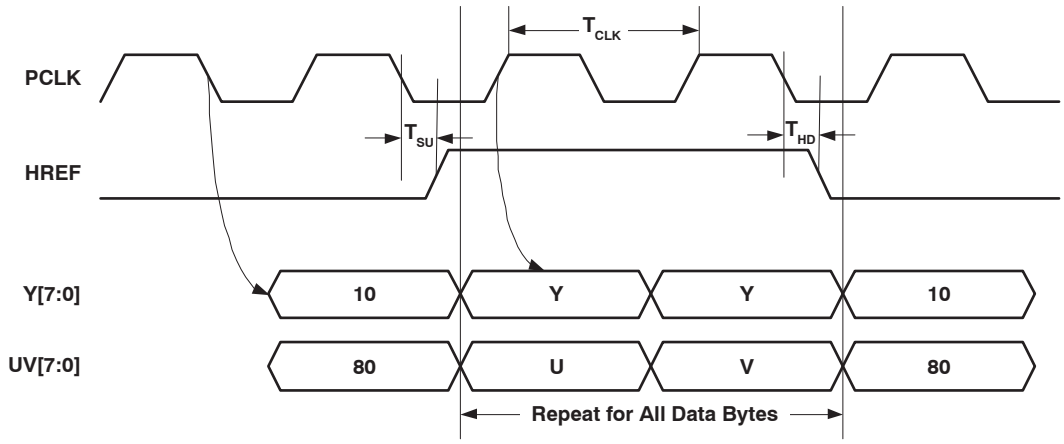
Symbol	Parameter	Min	Typ	Max	Unit
Oscillator and Clock Input					
f_{OSC}	Frequency (XCLK1 and XCLK2)	10	20	40	MHz
t_r, t_f	Clock input rise/fall time			5	ns
	Clock input duty cycle	45	50	55	%
SCCB Timing (400 Kbps) (see Figure 8)					
f_{SIO_C}	Clock Frequency			400	KHz
t_{LOW}	Clock Low Period	1.3			µs
t_{HIGH}	Clock High Period	600			ns
t_{AA}	SIO_C low to Data Out valid	100		900	ns
t_{BUF}	Bus free time before new START	1.3			µs
$t_{HD:STA}$	START condition Hold time	600			ns
$t_{SU:STA}$	START condition Setup time	600			ns
$t_{HD:DAT}$	Data-in Hold time	0			µs
$t_{SU:DAT}$	Data-in Setup time	100			ns
$t_{SU:STO}$	STOP condition Setup time	600			ns
t_R, t_F	SCCB Rise/Fall times			300	ns
t_{DH}	Data-out Hold time	50			ns

Table 12 Timing Characteristics (Continued)

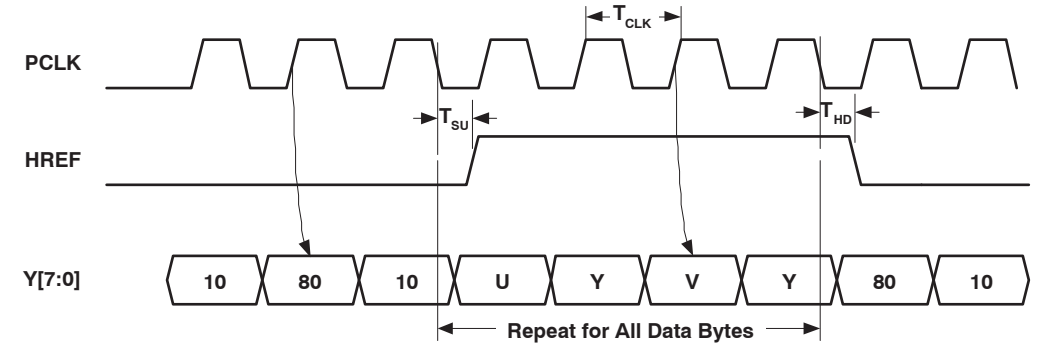
Symbol	Parameter	Min	Typ	Max	Unit
Digital Timing					
t_{PCLK}	PCLK cycle time (16-bit operation)		50		ns
t_{PCLK}	PCLK cycle time (8-bit operation)		50		ns
t_r, t_f	PCLK rise/fall time			5	ns
t_{PDD}	PCLK to data valid			5	ns
t_{PHD}	PCLK to HREF delay	5	10	20	ns
Zoom Video Port AC Parameters (see Figure 6)					
t1	PCLK fall time	4		8	ns
t2	PCLK low time	21			ns
t3	PCLK rise time	4		8	ns
t4	PCLK high time	21			ns
t5	PCLK period	50			ns
t6	Y/UV/HREF setup time	5			ns
t7	Y/UV/HREF hold time	20			ns
t8	VSYNC setup/hold time to HREF	1			µs

Timing Specifications

Figure 4 Pixel Data Bus (YUV Output) Timing



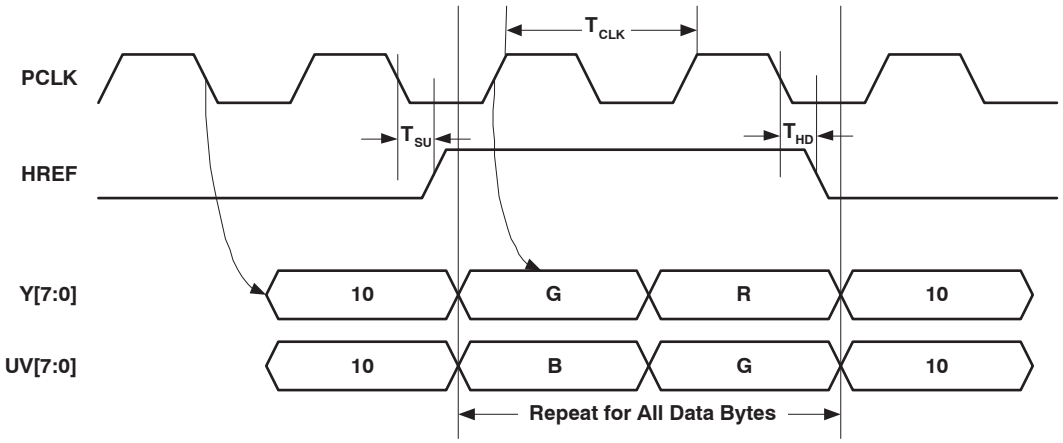
Pixel Data 16-bit Timing
(PCLK rising edge latches data bus)



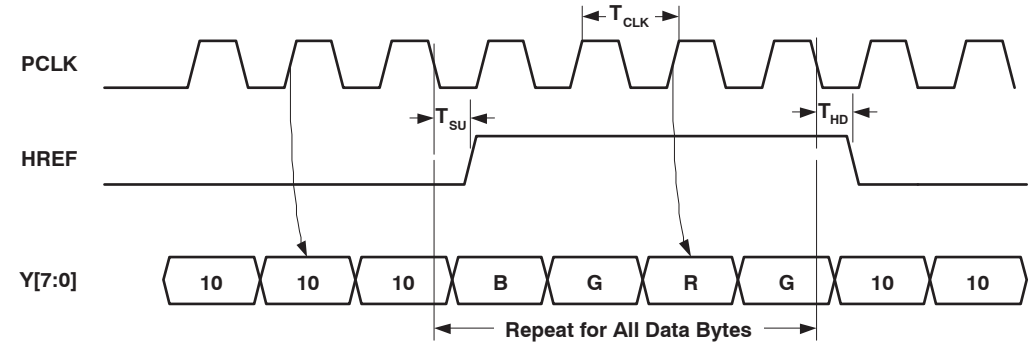
Pixel Data 8-bit Timing
(PCLK rising edge latches data bus)

NOTES:
1. T_{CLK} is the pixel clock period. T_{CLK} = 50 ns for 16-bit output and T_{CLK} = 25 ns for 8-bit output if the system clock is 20 MHz with on-chip 2x PLL.
2. T_{SU} is the setup time for HREF with a maximum time of 15 ns.
3. T_{HD} is the hold time for HREF with a maximum time of 15 ns.

Figure 5 Pixel Data Bus (RGB Output) Timing



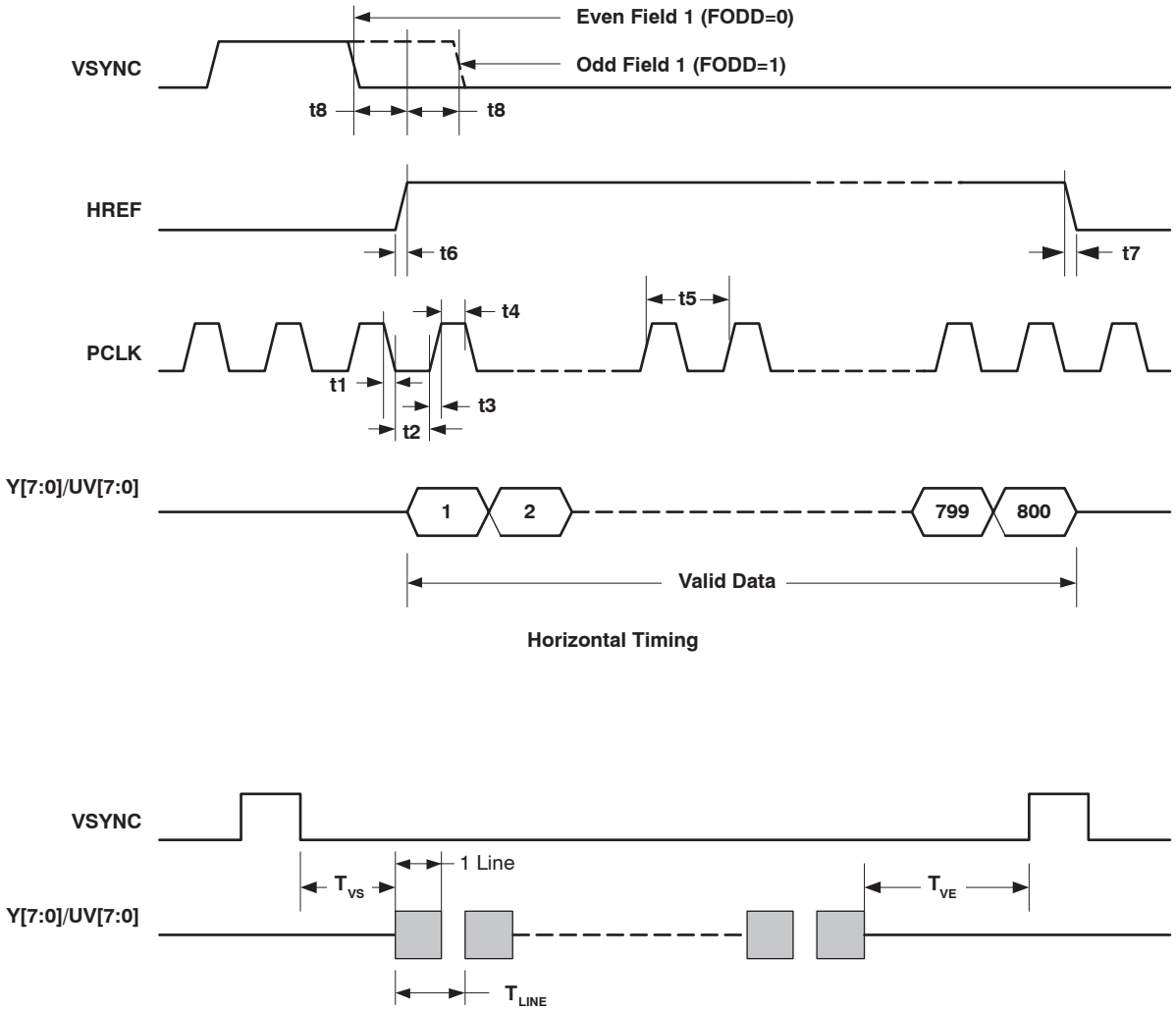
Pixel Data 16-bit Timing
(PCLK rising edge latches data bus)



Pixel Data 8-bit Timing
(PCLK rising edge latches data bus)

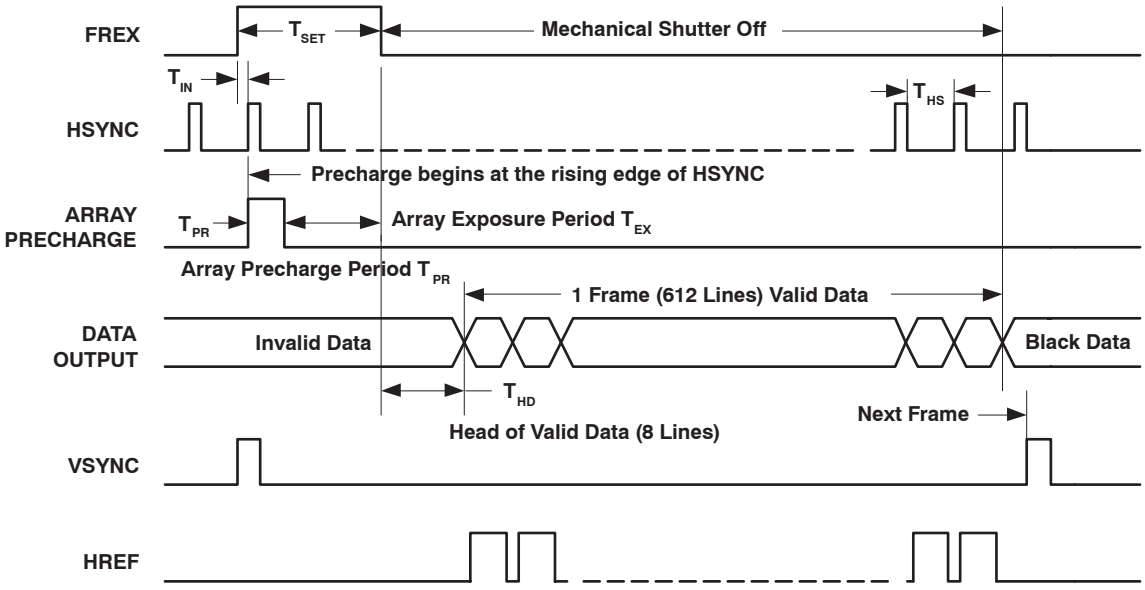
NOTES:
1. T_{CLK} is the pixel clock period. T_{CLK} = 50 ns for 16-bit output and T_{CLK} = 25 ns for 8-bit output if the system clock is 20 MHz with on-chip 2x PLL.
2. T_{SU} is the setup time for HREF with a maximum time of 15 ns.
3. T_{HD} is the hold time for HREF with a maximum time of 15 ns.

Figure 6 Zoom Video Port Timing



NOTE: Zoom Video Port format output signal includes:
VSYNC: Vertical sync pulse
HREF: Horizontal valid data output window
PCLK: Pixel clock used to clock valid data and CHSYNC into Zoom Video Port. Default frequency is 20 MHz when using 20 MHz as system clock plus 2x PLL implemented on the chip. Rising edge of PCLK is used to clock 16-bit data.
Y[7:0]: 8-bit luminance data bus
UV[7:0]: 8-bit chrominance data bus

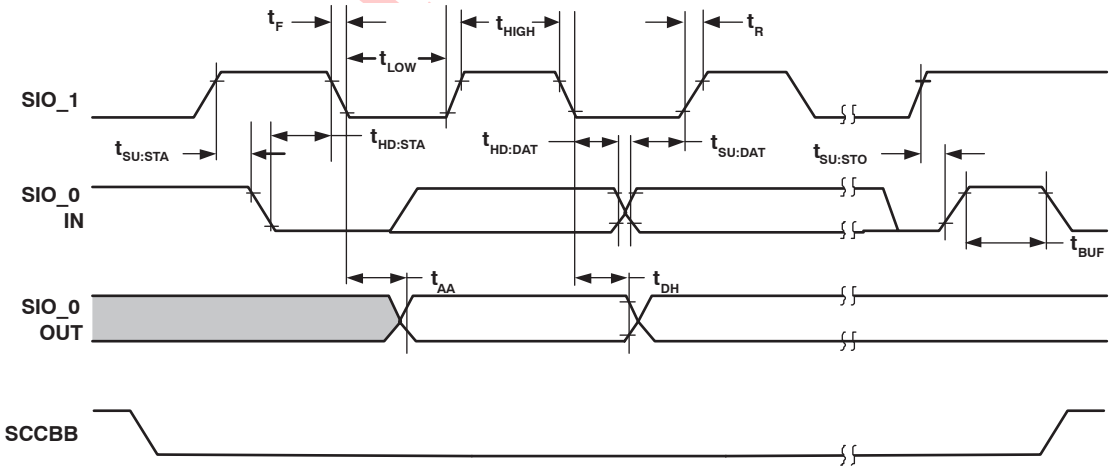
Figure 7 Frame Exposure Timing



NOTES:

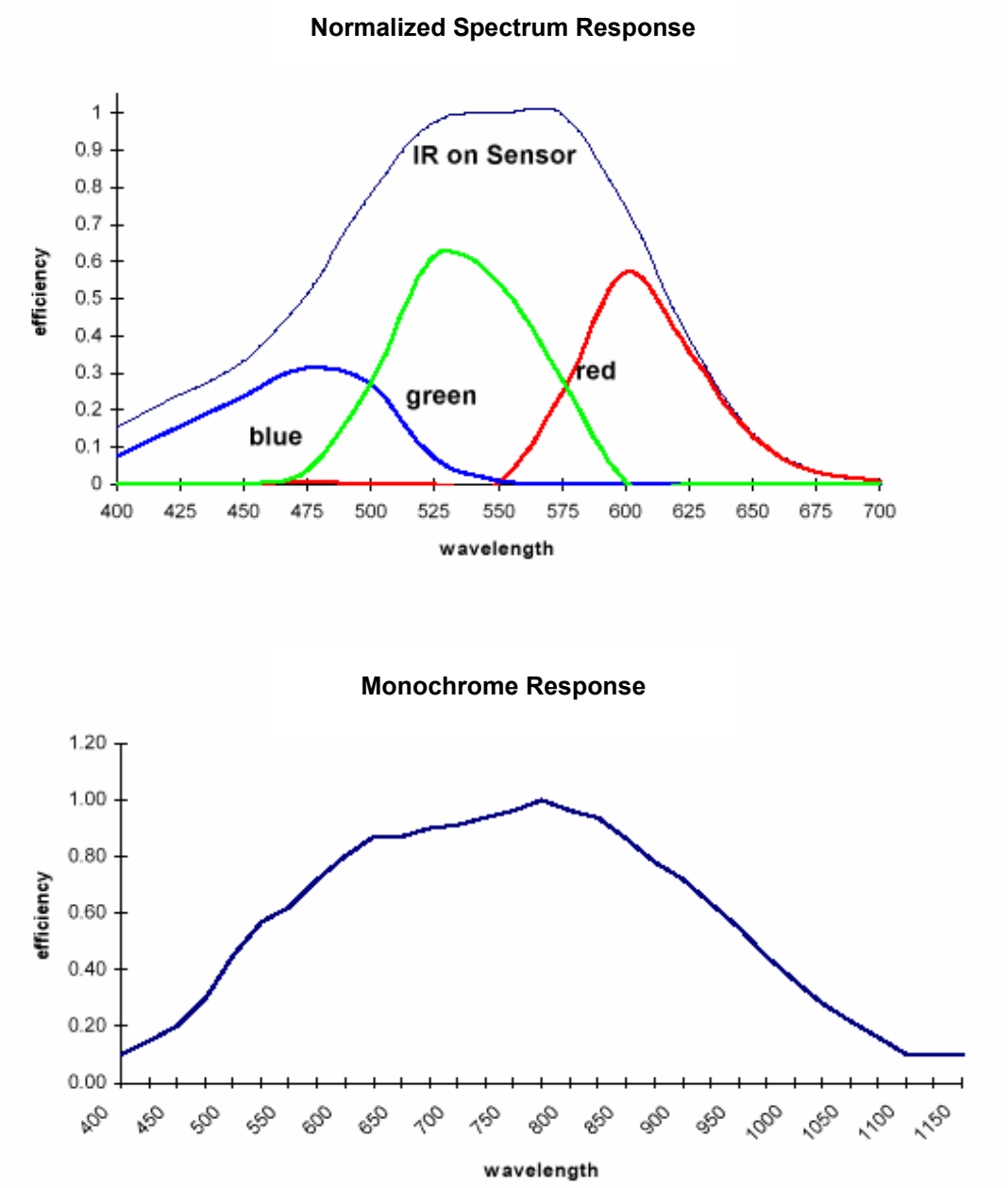
1. T_{PR}=612 x 4 x T_{CLK} or T_{PR}=858xT_{clk} depends on mode selecton. T_{CLK} is internal pixel period. T_{CLK}=74ns if the system clock is 27MHz . T_{CLK} will increase with the clock divider CLK[5:0].
2. T_{EX} is array exposure time which is decided by external master device.
3. T_{IN} is uncertain time due to the using of HSYNC rising edge to synchronize FREX. $T_{IN} < T_{HS}$.
4. There are 8 lines data output before valid data after FREX=0. T_{HD}=4 THS. Valid data is output when HREF=1.
5. $T_{SET}=T_{IN} + T_{PR} + T_{EX}$. $T_{SET} > T_{PR} + T_{IN}$. The exposure time setting resolution is T_{HS} (one line) due to the uncertainty of T_{IN}.

Figure 8 SCCB Timing Diagram



OV8610 Light Response

Figure 9 OV8610 Light Response



Register Set

Table 13 provides a list and description of the Device Control registers contained in the OV8610. The device slave addresses for the OV8610 are A0 for write and A1 for read.

Table 13 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC Gain Control Bit[7:6]: Reserved Bit[5:0]: Current gain setting ***Note:*** *This register is updated automatically if AGC is enabled. The internal controller stores the optimal gain value in this register. The current value is stored in this register if AGC is not enabled.*
01	BLUE	80	RW	Blue Gain Control Bit[7:0]: Blue channel gain balance value • Range: [00] to [FF]
02	RED	80	RW	Red Gain Control Bit[7:0]: Red channel gain balance value • Range: [00] to [FF]
03	SAT	80	RW	Color Saturation Control Bit[7:4]: Saturation adjustment • Range: [00] to [F8] Bit[3:0]: Reserved
04	HUE	10	RW	Color Hue Control Bit[7:6]: Reserved Bit[5]: Enable hue control Bit[4:0]: Hue control • Range: -30° to 30°
05	RSVD	XX	–	Reserved
06	BRT	80	RW	Brightness Control Bit[7:0]: Brightness adjustment • Range: [00] to [FF]
07-09	RSVD	XX	–	Reserved
0A	PID	86	R	Product ID Number (Read only)
0B	VER	B0	R	Product Version Number (Read only)
0C	ABLU	20	RW	White Balance Background - Blue Channel Bit[7:6]: Reserved Bit[5:0]: White balance blue ratio adjustment • Range: [3F] is most blue
0D	ARED	20	RW	White Balance Background - Red Channel Bit[7:6]: Reserved Bit[5:0]: White balance red ratio adjustment • Range: [3F] is most red

Table 13 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0E-0F	RSVD	XX	–	Reserved
10	AEC	A2	RW	Automatic Exposure Control Bit[7:0]: Set exposure time $T_{EX} = 4 \times T_{LINE} \times AEC[7:0]$
11	CLKRC	00	RW	Clock Rate Control Bit[7:6]: Sync output polarity selection 00: HSYNC = Neg, CHSYNC = Neg, VSYNC = Pos 01: HSYNC = Neg, CHSYNC = Neg, VSYNC = Neg 10: HSYNC = Pos, CHSYNC = Neg, VSYNC = Pos 11: HSYNC = Pos, CHSYNC = Pos, VSYNC = Pos Bit[5:0]: Clock pre-scalar CLK = (MAIN_CLOCK / (CLKRC[5:0] + 1) x 2) / n where n = 1, if COMD[5] = 1 (see "COMD" on page 22) and n = 2 otherwise.
12	COMA	24	RW	Common Control A Bit[7]: SRST 1: Initiates soft reset. All register are set to factory default values after which the chip resumes normal operation Bit[6]: MIRR 1: Selects mirror image Bit[5]: AGC enable 1: Enables AGC Bit[4]: Digital output format 0: U Y V Y U Y V Y (8-bit) 1: Y U Y V Y U Y V (8-bit) Bit[3]: Select video data output 0: YCbCr 1: RGB Bit[2]: Auto White Balance (AWB) 0: Disable AWB 1: Enable AWB Bit[1]: Color bar test pattern 1: Enable color bar test pattern Bit[0]: ADC BLC method 0: More stable but less precise 1: Precise

Table 13 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
13	COMB	01	RW	Common Control B Bit[7]: VSYNC output selection 0: VSYNC always output 1: No VSYNC output when no valid data Bit[6]: AGC/AWB register SCCB update option 0: Updated after VSYNC 1: Updated immediately after SCCB input Bit[5]: Select data format 0: Select 16-bit format 1: Select 8-bit format, YCbCr and RGB is multiplexed to 8-bit Y bus, UV bus is tri-stated Bit[4]: Digital output 1: Enable digital output in ITU-656 format Bit[3]: CHSYNC output 0: Horizontal sync 1: Composite sync Bit[2]: Y and UV buses 0: Enable both buses 1: Tri-state Y and UV buses Bit[1]: Frame transfer 1: Initiate single frame transfer Bit[0]: Auto adjust mode enable 0: Disable auto adjust mode 1: Enable auto adjust mode
14	COMC	00	RW	Common Control C Bit[7]: AWB threshold selection 0: More accurate but less stable 1: More stable but less accurate Bit[6]: UV option 0: Normal color mode 1: UV always zero Bit[5]: QSVGA digital output format selection 0: 800 x 600 1: 400 x 300 Bit[4]: Field/Frame vertical sync output in VSYNC port selection 0: Field vertical sync, effective in interlaced mode 1: Frame sync, only ODD field vertical sync Bit[3]: HREF polarity selection 0: HREF positive 1: HREF negative Bit[2]: Gamma selection 0: RGB gamma is 1 1: RGB gamma ON Bit[1:0]: Reserved

Table 13 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
15	COMD	01	RW	Common Control D Bit[7]: ADC clock 50% duty cycle selection 0: Non-50% duty cycle 1: 50% duty cycle Bit[6]: PCLK polarity selection 0: OV8610 output data at PCLK falling edge and data bus will be stable at PCLK rising edge 1: Rising edge output data and stable at PCLK falling edge Bit[5]: Digital 2x PLL disable 0: Enable 1: Disable Bit[4]: Array vertical second stage skip mode enable. Frame rate will double and only effective in progressive scan mode, while first stage sub-sampling is disabled. Bit[3]: AGCEN pin option 0: Normal AGCEN pin 1: AGCEN as data output enable/disable pin control Bit[2]: Reserved Bit[1]: Enable NTSC timing - only part of full resolution output Bit[0]: UV digital output sequence exchange control 0: V U V U (for 16-bit) and V Y U Y (for 8-bit) 1: UV UV (for 16-bit) and U Y V Y (for 8-bit)
16	FSD	03	RW	Field Slot Division Bit[7:2]: Field interval selection It is functional in EVEN and ODD mode defined by FSD[1:0]. It is disabled in OFF and FRAME modes. The purpose of FSD[7:2] is to divide the video signal into programmed number of time slots and allow HREF to be active for only one field in every FSD[7:2] fields. It does not affect the video data or pixel rate. FSD[7:2] disables digital data output. There is only black reference level at the output. FSD[7:2] = 1 outputs every field. FSD[7:2] outputs one field and disables one field, etc. Bit[1:0]: Field mode selection Each frame consists of two fields, odd and even. FSD[1:0] defines the assertion of HREF in relation to the two fields. 00: OFF mode - HREF is not asserted in both fields, one exception is the single frame transfer operation (see “COMB” on page 21). 01: ODD mode - HREF is asserted in odd fields only 10: EVEN mode - HREF is asserted in even fields only 11: FRAME mode - HREF is asserted in both odd and even fields. FSD[7:2] is disabled.

Table 13 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
17	HREFST	38	RW	Horizontal HREF Start Bit[7:0]: Selects the starting point of the HREF window. Each LSB represents four pixels in SVGA resolution mode, two pixels in QSVGA resolution mode, and one pixel for QCIF resolution mode. This value is set based on an internal column counter. The default value corresponds to a window size 800 pixels wide. Maximum window size is 824 pixels. • HREFST[7:0] should be less than HREFEND[7:0] (see "HREFEND" on page 23)
18	HREFEND	EA	RW	Horizontal HREF End Bit[7:0]: Selects the ending point of the HREF window. Each LSB represents four pixels in full resolution, two pixels in QSVGA mode, and one pixel for QCIF resolution mode. This value is set based on an internal column counter. The default value corresponds to the last available pixel. • HREFEND[7:0] should be larger than HREFST[7:0] (see "HREFST" on page 23)
19	VSTRT	03	RW	Vertical Line Start Bit[7:0]: Selects the starting row of the vertical window. In full resolution mode, each LSB represents two scan lines in one field in interlaced scan mode and four scan lines in one frame in progressive scan mode. In QSVGA mode, each LSB represents one scan line in one field in interlaced mode and two scan lines in one frame for progressive scan mode. • Range: [02] to [98] and VSTRT[7:0] should be less than VEND[7:0] (see "VEND" on page 23)
1A	VEND	92	RW	Vertical Line End Bit[7:0]: Selects the ending row of the vertical window. In full resolution mode, each LSB represents two scan lines in one field in interlaced scan mode and four scan lines in one frame in progressive scan mode. In QSVGA mode, each LSB represents one scan line in one field in interlaced mode and two scan lines in one frame for progressive scan mode. • Range: [03] to [98] and VEND[7:0] should be larger than VSTRT[7:0] (see "VSTRT" on page 23)
1B	PSHFT	00	RW	Pixel Shift Bit[7:0]: Provides a way to fine tune the output timing of the pixel data relative to that of HREF. It physically shifts the video data output time late in unit of pixel clock. This function is different from changing the size of the window as defined by HREFST[7:0] (see "HREFST" on page 23) and HREFEND[7:0] (see "HREFEND" on page 23). It just delays the pixel output relative to HREF and does not change the window size. The highest number is [FF] and the maximum shift number is a delay of 256 pixels.
1C	MIDH	7F	R	Manufacturer ID Byte – High (Read only = 0x7F)
1D	MIDL	A2	R	Manufacturer ID Byte – Low (Read only = 0xA2)
1E-1F	RSVD	XX	–	Reserved

Table 13 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
20	COME	00	RW	Common Control E Bit[7]: Reserved Bit[6]: Enables field/frame luminance average value calculations. Values are stored in AVG[7:0] (see "AVG" on page 33) Bit[5]: PCLK output option 0: Disables PCLK output during Sleep mode 1: Enables PCLK output during Sleep mode Bit[4]: Aperture correction 0: Disable 1: Enable (correction strength and threshold value will be decided by COMF[7:6] for threshold and COMF[5:4] for strength (see "COMF" on page 27) Bit[3]: AWB smart mode enable 0: Count all pixels to get AWB result. Valid only when COMB[0] = 1 (see "COMB" on page 21) and COMA[2] = 1 (see "COMA" on page 20) 1: Do not count pixels whose luminance and level are not in the range defined in AWBC[7:6] and AWBC[5:4] (see "AWBC" on page 31) Bit[2]: Aperture correction mode selection 0: Correction always in whole range luminance 1: Correction only when luminance average level is larger than present level Bit[1]: AWB fast/slow mode selection 0: AWB is in slow mode where BLUE[7:0] and RED[1:0] changes every 16/64 field decided by COMK[1] (see "COMK" on page 31). When AWB is enabled (COMA[2] = 1, see "COMA" on page 20), AWB works in fast mode until it becomes stable, then it works in slow mode. 1: AWB is always in fast mode where BLUE[7:0] and RED[7:0] is changed every field Bit[0]: Digital output driver capability increase selection 0: Low output driver current status 1: Double digit output driver current
21	YOFF	80	RW	Y Channel Offset Adjustment Bit[7]: Offset adjustment direction 0: Add YOFF[6:0] 1: Subtract YOFF[6:0] Bit[6:0]: Y channel digital output offset adjustment If COMG[2] = 0 (see "COMG" on page 27), this register will updated by internal circuit. Writing a value to this register through the SCCB interface will have no affect. If COMG[2] = 1, Y channel offset adjustment will use the stored value which can be changed through the SCCB interface. This register has no affect on ADC output data if COMF[1] = 0 (see "COMF" on page 27). If output is RGB raw data, this register will adjust G channel data. • Range: -127 to 127

Table 13 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
22	UOFF	80	RW	U Channel Offset Adjustment Bit[7]: Offset adjustment direction 0: Add UOFF[6:0] 1: Subtract UOFF[6:0] Bit[6:0]: U channel digital output offset adjustment If COMG[2] = 0 (see "COMG" on page 27), this register will updated by internal circuit. Writing a value to this register through the SCCB interface will have no affect. If COMG[2] = 1, U channel offset adjustment will use the stored value which can be changed through the SCCB interface. This register has no affect on ADC output data if COMF[1] = 1 (see "COMF" on page 27). If output is RGB raw data, this register will adjust B channel data. • Range: -128 to 128
23	CLKC	04	RW	Oscillator Circuit Control Bit[7:6]: Select different crystal circuit power level • [11] minimum Bit[5]: ADC current control 0: Full current 1: Half current Bit[4]: Output data polarity selection 0: Positive 1: Negative Bit[3]: Horizontal array skip mode 0: Full pixel readout 1: Only read out half of horizontal pixels (400) and frame rate will double Bit[2]: Vertical array first stage skip mode 1: Only read out half of vertical lines (200) and frame rate will double Bit[1]: System clock output selection 0: System clock. Only effective when FODD is set to output system clock 1: Half frequency of system clock Bit[0]: Aperture correction mode selection 0: Disable aperture correction mode 1: Enable threshold relative to current gain faction

Table 13 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
24	AEW	33	RW	Automatic Exposure Control (AEC) - Bright Pixel Ratio Adjustment Bit[7:0]: Used to calculate bright pixel ratio. The OV8610 AEC algorithm is a count of the whole field/frame bright pixel ratio (pixels whose luminance level is higher than a fixed level) and black pixel ratio (pixels whose luminance level is lower than a fixed level). When the bright/black pixel ratio in the range of the ratio defined by the registers AEW[7:0] and AEB[7:0] (see "AEB" on page 26), the image is stable. This register is used to define bright pixel ratio, default is 25%. Each LSB represents step: 1.3% for interlaced and 0.7% for progressive scan. Change range is [01] to [65]. Increasing AEW[7:0] will increase the bright pixel ratio. For same light condition, the image brightness will increase if AEW[7:0] increases. ***Note:*** *AEW[7:0] must combine with register AEB[7:0]. The relationship must be as follows:* *AEW[7:0] + AEB[7:0] > [65]*
25	AEB	97	RW	Automatic Exposure Control (AEC) - Black Pixel Ratio Adjustment Bit[7:0]: Used to calculate black pixel ratio. The OV7630/OV7130 algorithm is a count of the whole field/frame bright pixel ratio (pixels whose luminance level is higher than a fixed level) and black pixel ratio (pixels whose luminance level is lower than a fixed level). When the bright/black pixel ratio in the range of the ratio defined by the registers AEW[7:0] (see "AEW" on page 26) and AEB[7:0], the image is stable. This register is used to define black pixel ratio, default is 75%. Each LSB represents step: 1.3% for interlaced and 0.7% for progressive scan. Change range is [01] to [65]. Increasing AEB[7:0] will increase the black pixel ratio. For same light condition, the image brightness will decrease if AEB[7:0] increases. ***Note:*** *AEW[7:0] must combine with register AEB[7:0]. The relationship must be as follows:* *AEW[7:0] + AEB[7:0] > [65]*

Table 13 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
26	COMF	B0	RW	Common Control F Bit[7:6]: Aperture correction threshold selection • Range: 1% to 6.4% of the difference of neighbor pixel luminance Bit[5:4]: Aperture correction strength selection • Range: 0% to 200% of the difference of neighbor pixel luminance Bit[3]: Reserved Bit[2]: Digital data MSB/LSB swap 0: Normal 1: LSB to bit[7] and MSB to bit[0] Bit[1]: Digital offset adjustment enable 0: Disable 1: Enable Bit[0]: Black level output selection 0: No black level output 1: Output first 4/8 lines black level before valid data output for interlaced/progressive scan mode, respectively. HREF number will increase 4/8 lines relatively
27	COMG	A0	RW	Common Control G Bit[7:6]: Reserved Bit[5]: Select smart AWB algorithm control condition 0: If strong color component is more than 40%, stop AWB 1: If strong color component is more than 60%, stop AWB Bit[4]: Reserved Bit[3]: Enable ADC black level calibration offset defined by registers Bit[2]: Digital data offset adjustment manual mode enable 0: Digital data will be added/subtracted by a value defined in registers YOFF (see "YOFF" on page 24), UOFF (see "UOFF" on page 25), and VCOFF (see "VCOFF" on page 29) which are updated by internal circuit. 1: Digital data will be added/subtracted by a value defined in registers YOFF (see "YOFF" on page 24), UOFF (see "UOFF" on page 25), and VCOFF (see "VCOFF" on page 29) of which the contents can be programmed through the SCCB interface. Bit[1]: Digital output full range selection 0: Output range is [10] to [F0] 1: Output range is [01] to [FE] Bit[0]: Reserved

Table 13 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
28	COMH	01	RW	Common Control H Bit[7]: RGB raw data output select 0: Normal two-line RGB raw data output format 1: One-line RGB raw data output format Bit[6]: Reserved Bit[5]: Scan mode selection 0: Interlaced mode 1: Progressive mode Bit[4]: Freeze AEC/AGC value (effective only when COMB[0] = 1 (see "COMB" on page 21) 0: AEC/AGC normal working status 1: Registers GAIN[7:0] (see "GAIN" on page 19) and AEC[7:0] (see "AEC" on page 20) will not be updated and will hold latest value Bit[3]: AGC disable 0: When COMB[0] = 1 (see "COMB" on page 21) and COMA[5] = 1 (see "COMA" on page 20), GAIN[7:0] (see "GAIN" on page 19) will be updated by the internal algorithm. 1: When COMB[0] = 1 and COMA[5] = 1, internal circuit will not update register GAIN[7:0]. Register GAIN[7:0] will keep latest updated value. Bit[2]: RGB raw data output YG format 0: Y channel G R G R 1: UV channel B G B G Bit[1]: Gain control bit 0: No change to channel gain 1: Channel gain increases 3 dB Bit[0]: Change AGCEN input pin to FSIN input when this register is "1"
29	COMI	00	RW	Common Control I Bit[7]: AEC disable 0: If COMB[0] = 1 (see "COMB" on page 21), AEC[7:0] value (see "AEC" on page 20) will be updated by internal circuit 1: If COMB[0] = 1, AEC stops and register AEC[7:0] value will be held at last AEC value and NOT be updated by internal circuit Bit[6]: Slave mode selection 0: Master mode 1: Slave mode, use external SYNC and VSYNC Bit[5]: ADC data latch 10 ns delay option Bit[4]: Reserved Bit[3]: Image area used to calculate AEC/AGC 0: Whole image 1: Central 1/4 image area Bit[2]: Reserved Bit[1:0]: Version flag. For version A, value is [00]. These two bits are Read-only.

Table 13 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
2A	FRARH	84	RW	Frame Rate Adjust High Bit[7]: Frame rate adjustment enable 0: Disable 1: Enable Bit[6:5]: Highest 2 bits of frame rate adjust control byte Bit[4]: Output range selection 0: [00] to [FF] 1: [01] to [FE] Bit[3]: Y brightness manual adjustment. Effective only if COMF[1] = 1 (see "COMF" on page 27) Bit[2]: Enable HSYNC latched by PCLK Bit[1]: Data output 1: One frame data output. Only when in Frame Exposure mode Bit[0]: Fast AGC mode 0: Smooth but slow AGC mode 1: Speed double
2B	FRARL	5E	RW	Frame Rate Adjust Low Bit[7:0]: Frame rate adjust control byte. Frame rate adjustment resolution is 0.12%. Control byte is 10 bits. Every LSB equals a decrease frame rate of 0.12%. • Range: 0.12% to 112%
2C	RSVD	XX	–	Reserved
2D	COMJ	80	RW	Common Control J Bit[7:5]: Reserved Bit[4]: Enable auto black expanding mode Bit[3]: Reserved Bit[2]: Band filter enable - this bit enables a different exposure algorithm to cut light band induced by fluorescent light Bit[1]: Reverse output frame division 1: Change drop frame to output frame Bit[0]: Reserved
2E	VCOFF	80	RW	V Channel Offset Adjustment Bit[7]: Offset adjustment direction 0: Add VCOFF[6:0] 1: Subtract VCOFF[6:0] Bit[6:0]: V channel digital output offset adjustment If COMG[2] = 0 (see "COMG" on page 27), this register will be updated by internal circuit. Writing to this register through the SCCB interface has no effect. If COMG[2] = 1, V channel offset adjustment will use the stored value which can be changed through the SCCB interface. If COMF[1] (see "COMF" on page 27), this register has no effect on the digital output data. If output is RGB raw data, this register will adjust R/G/B data. • Range: -128 to +128
2F	REF1	19	RW	Internal Voltage Reference Control

Table 13 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
30-4B	RSVD	XX	–	Reserved
4C	MEDC	00	RW	Medium Filter Option Control Bit[7]: AWB step and range x 1.5 when this register is "1" Bit[6:0]: Reserved
4D	ADDC	10	RW	ADC Converter Option Control Bit[7:4]: Reserved Bit[3:2]: UV delay selection 00: No delay 01: No delay 10: 2tp delay 11: 4tp delay Bit[1:0]: Reserved
4E-5F	RSVD	XX	–	Reserved
60	SPCA	20	RW	Signal Process Control A Bit[7]: Channel 1.5x preamplifier gain enable (3 dB) Bit[6]: Analog half current selection Bit[5]: Gev/God switch instead of average for G in RGB and UV channel Bit[4]: Gev/God switch instead of average for Y channel in YUV mode Bit[3:2]: Red channel preamplifier gain selection 00: 1x 01: 1.2x 10: 1.4x 11: 1.6x Bit[1:0]: Blue channel preamplifier gain selection 00: 1x 01: 1.2x 10: 1.4x 11: 1.6x
61	SPCB	80	RW	Signal Process Control B Bit[7]: AGC/AEC feedback loop using Y channel. RGB output must set it to "0" Bit[6:5]: Reserved Bit[4]: Anti-aliasing 2x option Bit[3]: Enable RGB brightness control Bit[2]: Brightness control BRT[7:0] (see "BRT" on page 19) range and step half Bit[1:0]: Auto brightness reference level 00: 0 IRE 01: 6 IRE 10: 10 IRE 11: 20 IRE
62-64	RSVD	XX	–	Reserved

Table 13 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
65	SPCC	02	RW	Signal Process Control C Bit[7:3]: Reserved for internal use Bit[2]: ADC mode selection - increases range by 1.5x Bit[1:0]: ADC reference selection (use recommended value only)
66	AWBC	55	RW	AWB Process Control Bit[7:6]: Select highest luminance level to be available in AWB control. This bit is only in effect if COME[3] = 1 (see "COME" on page 24) Bit[5:4]: Select lowest luminance level to be available in AWB control. This bit is only in effect if COMM[3] = 1 (see "COME" on page 24) Bit[3:2]: Select U level to be available in AWB control. This bit is only in effect if COMM[7] = 1 (see "COMM" on page 32) Bit[1:0]: Select V level to be available in AWB control. This bit is only in effect if COMM[7] = 1 (see "COMM" on page 32)
67	YMXB	55	RW	YUV Matrix Control Bit[7:6]: UV coefficient selection, u = B - Y, v = R - Y 00: U = u, V = v 01: U = 0.938u, V = 0.838v 10: U = 0.563u, V = 0.613v 11: U = 0.5u, V = 0.877v Bit[5]: Reserved Bit[4]: UV signal with 3 points average Bit[3:2]: Y delay selection • Range: 0tp to 3tp Bit[1:0]: Reserved
68	ARL	AC	RW	AEC/AGC Reference Level Bit[7:5]: Voltage reference selection (higher voltage equals brighter final stable image) • Range: [000] for lowest reference level to [111] for highest reference level Bit[4:0]: Reserved
69-6F	RSVD	XX	–	Reserved
70	COMK	80	RW	Common Control K Bit[7]: HREF edge latched by PCLK falling edge Bit[6]: Output port drive current 2x larger option Bit[5]: Aperture correction option Bit[4]: ZV port vertical timing selection 0: Normal TV vertical sync signal 1: VSYNC output ZV port vertical sync signal Bit[3]: Reserved Bit[2]: Double aperture correction strength Bit[1]: 4x stable time less when in AWB slow mode Bit[0]: Disable output pin internal 100KΩ pull-down resistor

Table 13 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
71	COMJ	00	RW	Common Control J Bit[7]: Auto brightness update rate selection 0: Fast 1: Slow Bit[6]: PCLK output gated by HREF Bit[5]: Change HREF output port to CHSYNC Bit[4]: Change CHSYNC output port to HREF Bit[3:2]: Highest 2-bit for HSYNC rising edge shift control (see "HSDY" on page 32) Bit[1:0]: Highest 2-bit for HSYNC falling edge shift control (see "HEDY" on page 32)
72	HSDY	14	RW	Horizontal SYNC Rising Edge Shift COMJ[3:2] (see "COMJ" on page 32) and HSDY[7:0] for HSYNC rising edge shift control • Range: [000] to [3FF] step 1 pixel
73	HEDY	54	RW	Horizontal SYNC Falling Edge Shift COMJ[1:0] (see "COMJ" on page 32) and HEDY[7:0] for HSYNC falling edge shift control • Range: [000] to [3FF]
74	COMM	20	RW	Common Control M Bit[7]: Enable UV smart AWB threshold controlled by COMG[5] (see "COMG" on page 27) Bit[6:5]: AGC maximum gain boost control 00: 6 dB 01: 12 dB 10: 6 dB 11: 18 dB Bit[4:0]: Reserved
75	COMN	0E	RW	Common Control N Bit[7]: AWB control mode selection 0: Always do AWB 1: Stop AWB when field/frame average level is less than threshold Bit[6:4]: Reserved for internal test mode Bit[3]: Drop one field/frame when exposure line change is bigger than a fixed number Bit[2]: Enable exposure to go down to less than 1/120" or 1/60" in smooth AEC mode Bit[1:0]: Reserved

Table 13 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
76	COMO	00	RW	Common Control K Bit[7]: Output main clock at FODD pin (see "FODD/SRAM" on page 9) Bit[6]: Reserved Bit[5]: Software power down mode Bit[4]: ITU-656 timing Bit[3]: Reserved Bit[2]: Tri-state all timing output except data line Bit[1]: SCCB writing bit synchronized by VSYNC Bit[0]: Reserved
77	RSVD	XX	–	Reserved
78	YBAS	80	RW	Y/G ADC Offset Bit[7:0]: Fixed offset to final Y/G data • Range: -128 to 128
79	UBAS	80	RW	U/B ADC Offset Bit[7:0]: Fixed offset to final U/B data • Range: -128 to 128
7A	VBAS	80	RW	V/R ADC Offset Bit[7:0]: Fixed offset to final V/R data • Range: -128 to 128
7B	REF2	D8	RW	Internal Reference Control
7C	AVG	00	RW	Field/Frame average level storage. Only effective if COME[6] = 1 (see "COME" on page 24)
7D	COMP	08	RW	Common Control P Bit[7]: 10-bit output in one port output, less 2-bit come from UV1 and UV0 Bit[6]: 10-bit output in one port output, less 2-bit come from FODD and HREF Bit[5]: Reserved Bit[4]: Flip vertical safe read out. Only in YUV mode. Bit[3]: ADC BLC level option 0: 10-bit ADC BLC level "40" (H) 1: 10-bit ADC BLC level "10" (H) Bit[2:0]: Reserved
7E-81	RSVD	XX	–	Reserved
82	VB	23	RW	AEC/AGC Fast Mode Low Threshold Control (same as AEB[7:0] (see "AEB" on page 26)
83	VW	0B	RW	AEC/AGC Fast Mode High Threshold Control (same as AEW[7:0] (see "AEW" on page 26)

Table 13 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
84	COMS	00	RW	Common Control S Bit[7]: Reserved Bit[6]: Average AGC/AEC algorithm Bit[5:3]: Reserved Bit[2]: One-line ADC option Bit[1:0]: Reserved
85-88	RSVD	XX	–	Reserved
89	COMV	00	RW	Common Control V Bit[7]: Auto frame rate adjustment selection 0: One time every 1 field/frame 1: One time every 2 fields/frames Bit[6]: Double output pixel clock Bit[5]: Output true black line Bit[4]: CIF one-line clock phase selection Bit[3]: Enable ZV timing HSYNC option Bit[2]: Bypass RGB matrix Bit[1]: Change highest bit AGC to clock down 2 Bit[0]: Reserved
8A	RAVE	00	RW	R Channel Average Value
8B	BAVE	00	RW	B Channel Average Value
NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.				

Package Specifications

The OV8610 uses a 48-pin ceramic package. Refer to Figure 10 for package information and Figure 11 for the array center on the chip.

Figure 10 OV8610 Package Specifications

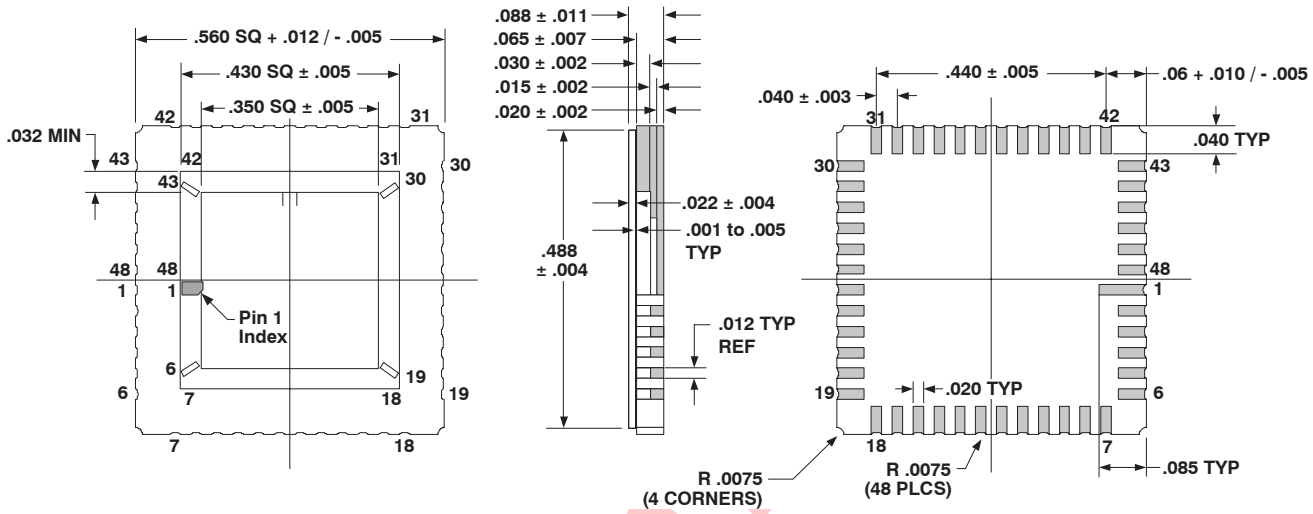
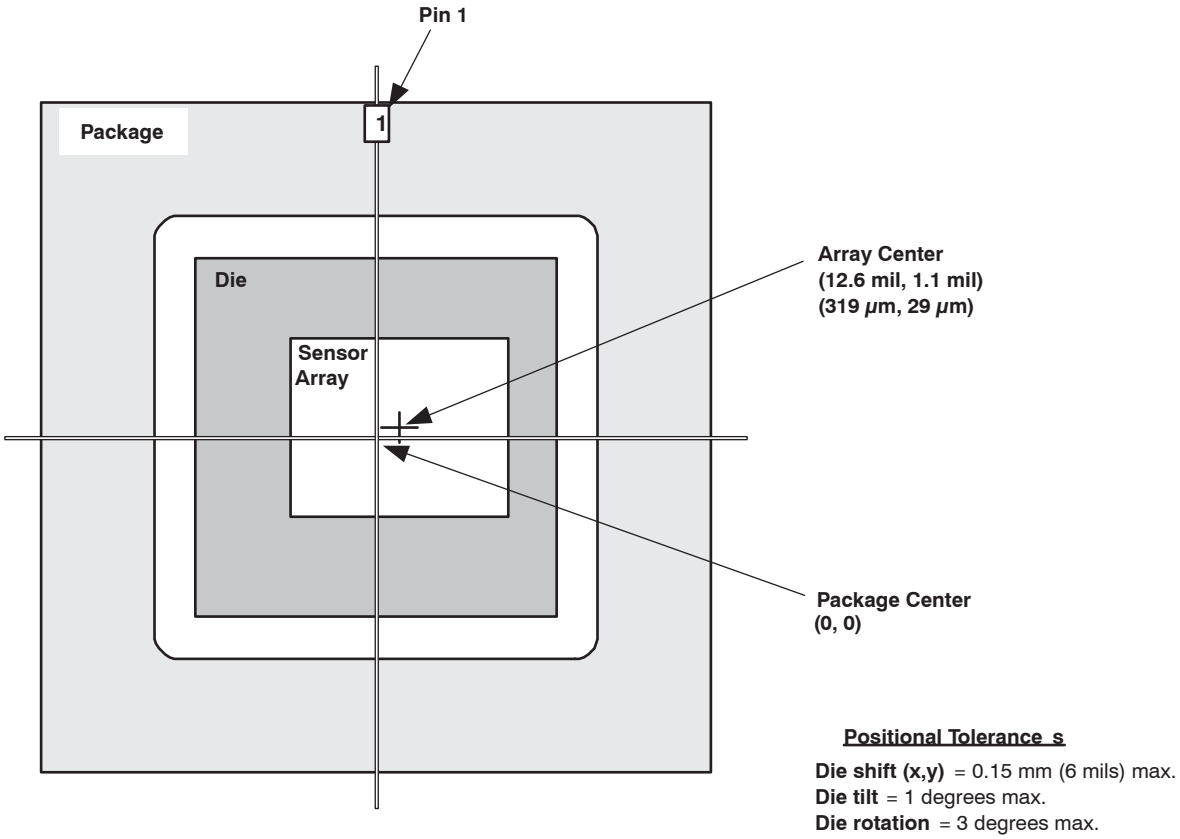


Table 14 OV8610 Package Dimensions

Dimensions	Millimeters (mm)	Inches (in.)
Package Size	14.22 + 0.30 / -0.13 SQ	.560 + .012 / - .005 SQ
Package Height	2.23 ± 0.28	.088 ± .011
Substrate Height	0.51 ± 0.05	.020 ± .002
Cavity Size	8.89 ± 0.13 SQ	.350 ± .005 SQ
Castellation Height	1.14 ± 0.13	.045 ± .005
Pin #1 Pad Size	0.51 x 2.16	.020 x .085
Pad Size	0.51 x 1.02	.020 x .040
Pad Pitch	1.02 ± 0.08	.040 ± .003
Package Edge to First Lead Center	1.524 + 0.25 / -0.13	.06 + .010 / - .005
End-to-End Pad Center-Center	11.18 ± 0.13	.440 ± .005
Glass Size	12.40 ± 0.10 SQ / 13.00 ± 0.10 SQ	.488 ± .004 SQ / .512 ± .004 SQ
Glass Height	0.55 ± 0.05	.022 ± .002

Sensor Array Center

Figure 11 OV8610 Sensor Array Center



Important: Most optical systems invert and mirror the image so the chip is usually mounted on the board with pin 1 (SVDD) down.

NOTE: Picture is for reference only, not to scale.

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

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