

# LH532100B-1

CMOS 2M (256K × 8) MROM

## FEATURES

- 262,144 words × 8 bit organization
- Access time: 120 ns (MAX.)
- Static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Power consumption:
  - Operating: 275 mW (MAX.)
  - Standby: 550 μW (MAX.)
- Mask-programmable control pin:
  - Pin 1 = OE<sub>1</sub>/OE<sub>1</sub>/DC
  - Pin 24 = OE/OE
- Packages:
  - 32-pin, 600-mil DIP
  - 32-pin, 525-mil SOP
  - 32-pin, 450-mil QFJ (PLCC)
  - 32-pin, 8 × 20 mm<sup>2</sup> TSOP (Type I)
  - 32-pin, 400-mil TSOP (Type II)

## DESCRIPTION

The LH532100B-1 is a CMOS 2M-bit mask-programmable ROM organized as 262,144 × 8 bits. It is fabricated using silicon-gate process technology.

## PIN CONNECTIONS

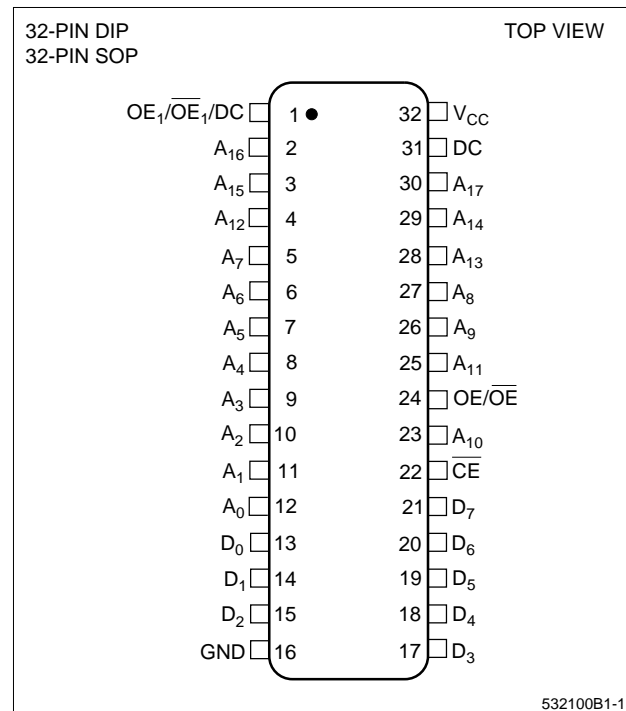


Figure 1. Pin Connections for DIP and SOP Packages

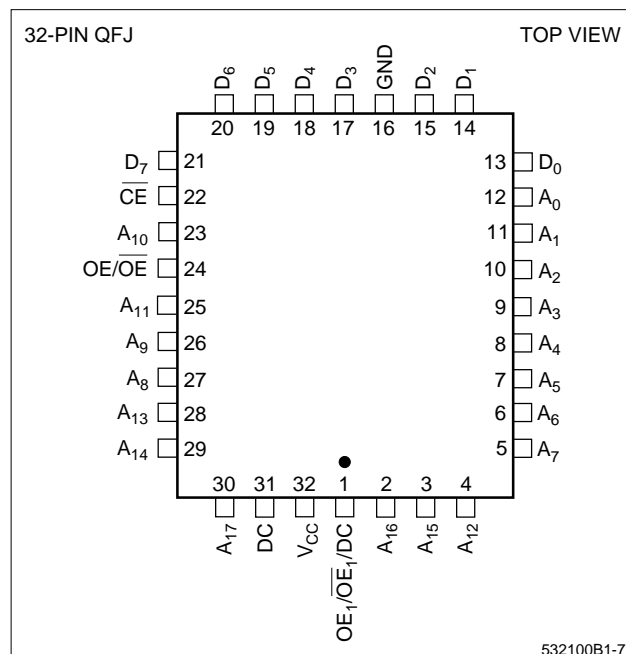


Figure 2. Pin Connections for QFJ (PLCC) Package

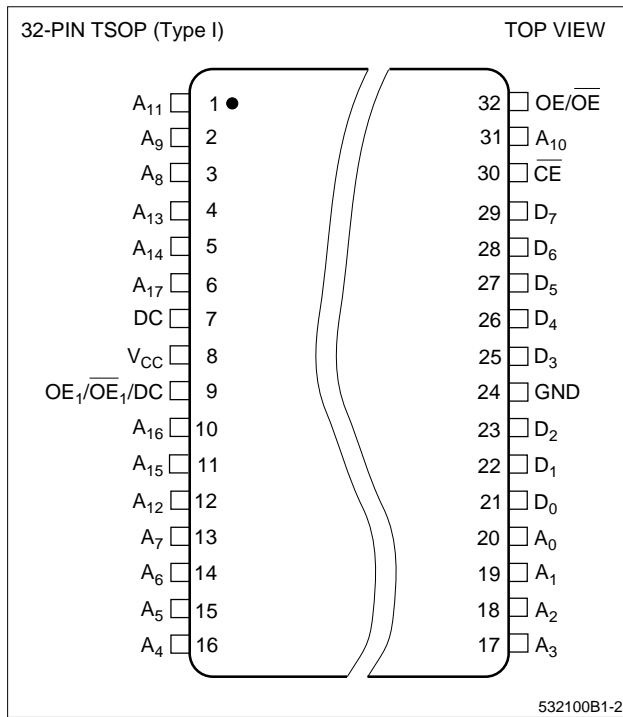


Figure 3. Pin Connections for TSOP (Type I) Package

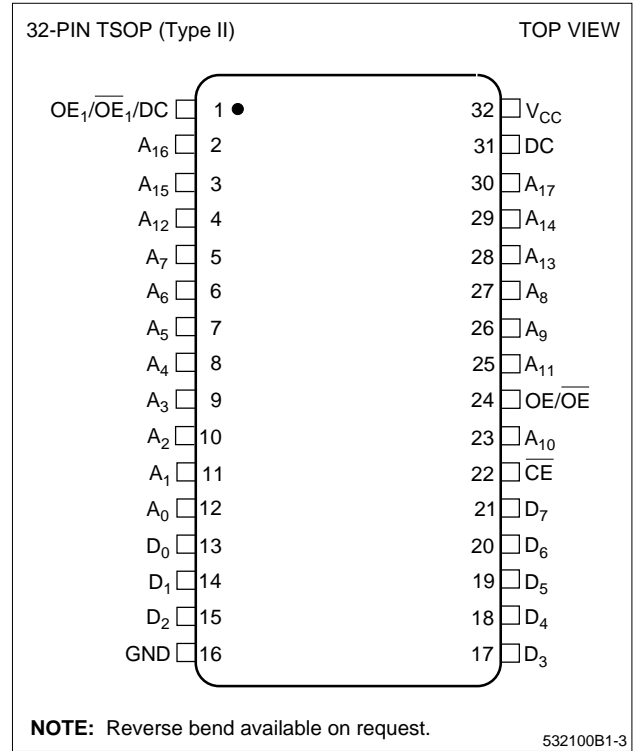


Figure 4. Pin Connections for TSOP (Type II) Package

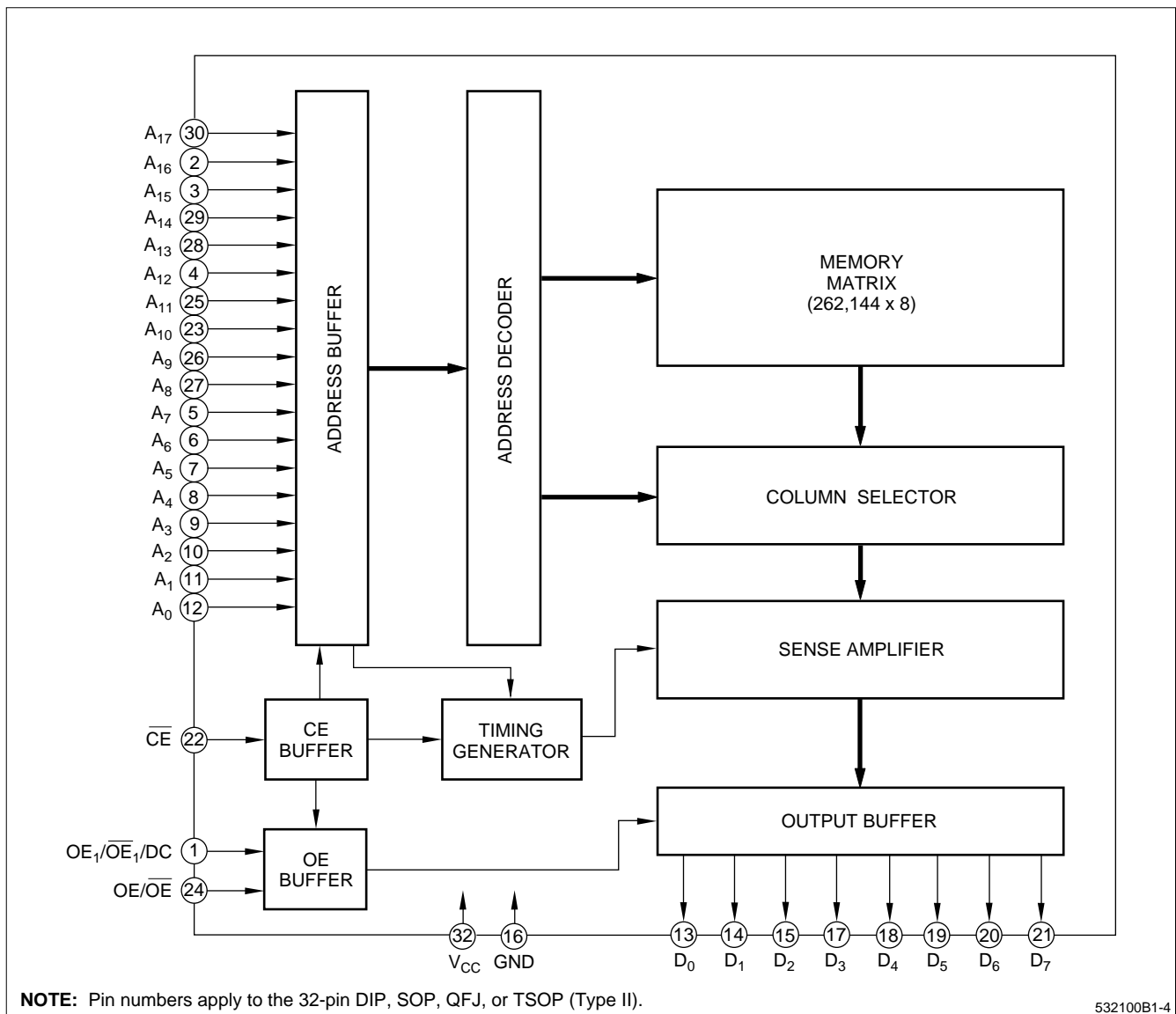


Figure 5. LH532100B-1 Block Diagram

**PIN DESCRIPTION**

SIGNAL	PIN NAME	NOTE
A <sub>0</sub> – A <sub>17</sub>	Address input	
D <sub>0</sub> – D <sub>7</sub>	Data output	
CE	Chip enable input	
OE/OE	Output enable input	1

SIGNAL	PIN NAME	NOTE
OE <sub>1</sub> /OE <sub>1</sub> /DC	Output enable input	1, 2
V <sub>CC</sub>	Power supply (+5 V)	
GND	Ground	

**NOTES:**

- Active levels of OE/OE and OE<sub>1</sub>/OE<sub>1</sub>/DC are mask-programmable. Selecting DC allows the outputs to be active for both high and low levels applied to this pin. It is recommended to apply either a HIGH or a LOW to the DC pin.
- DC = Don't care.

## TRUTH TABLE

$\overline{CE}$	OE/ $\overline{OE}$	OE <sub>1</sub> / $\overline{OE}_1$	DATA OUTPUT	SUPPLY CURRENT
H	X	X	High-Z	Standby
L	L/H	X	High-Z	Operating
L	X	L/H	High-Z	Operating
L	H/L	H/L	Output	Operating

## NOTE:

X = H or L, High-Z = High-impedance

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	$V_{CC}$	-0.3 to +7.0	V
Input voltage	$V_{IN}$	-0.3 to $V_{CC} + 0.3$	V
Output voltage	$V_{OUT}$	-0.3 to $V_{CC} + 0.3$	V
Operating temperature	$T_{opr}$	0 to +70	°C
Storage temperature	$T_{stg}$	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS ( $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V

DC CHARACTERISTICS ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	$V_{IH}$		2.2	$V_{CC} + 0.3$	V	
Input 'Low' voltage	$V_{IL}$		-0.3	0.8	V	
Output 'High' voltage	$V_{OH}$	$I_{OH} = -400\ \mu\text{A}$	2.4		V	
Output 'Low' voltage	$V_{OL}$	$I_{OL} = 2.0\ \text{mA}$		0.4	V	
Input leakage current	$ I_{LI} $	$V_{IN} = 0\ \text{V}$ to $V_{CC}$		10	$\mu\text{A}$	
Output leakage current	$ I_{LO} $	$V_{OUT} = 0\ \text{V}$ to $V_{CC}$		10	$\mu\text{A}$	1
Operating current	$I_{CC1}$	$t_{RC} = 120\ \text{ns}$		50	mA	2
	$I_{CC2}$	$t_{RC} = 1\ \mu\text{s}$		45	mA	2
	$I_{CC3}$	$t_{RC} = 120\ \text{ns}$		45	mA	3
	$I_{CC4}$	$t_{RC} = 1\ \mu\text{s}$		40	mA	3
Standby current	$I_{SB1}$	$CE = V_{IH}$		3	mA	
	$I_{SB2}$	$CE = V_{CC} - 0.2\ \text{V}$		100	$\mu\text{A}$	
Input capacitance	$C_{IN}$	$f = 1\ \text{MHz}$		10	pF	
Output capacitance	$C_{OUT}$	$T_A = 25^\circ\text{C}$		10	pF	

## NOTES:

- $CE/OE/OE_1 = V_{IH}$ ,  $OE/OE_1 = V_{IL}$
- $V_{IN} = V_{IH}$  or  $V_{IL}$ ,  $CE = V_{IL}$ , outputs open
- $V_{IN} = (V_{CC} - 0.2\ \text{V})$  or  $0.2\ \text{V}$ ,  $CE = 0.2\ \text{V}$ , outputs open

**AC CHARACTERISTICS ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )**

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	$t_{RC}$	120		ns	
Address access time	$t_{AA}$		120	ns	
Chip enable access time	$t_{ACE}$		120	ns	
Output enable delay time	$t_{OE}$		50	ns	
Output hold time	$t_{OH}$	10		ns	
CE to output in High-Z	$t_{CHZ}$		50	ns	1
OE to output in High-Z	$t_{OHZ}$				

**NOTE:**

1. This is the time required for the outputs to become high-impedance.

**AC TEST CONDITIONS**

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1 TTL + 100 pF

**CAUTION**

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the  $V_{CC}$  pin and the GND pin.

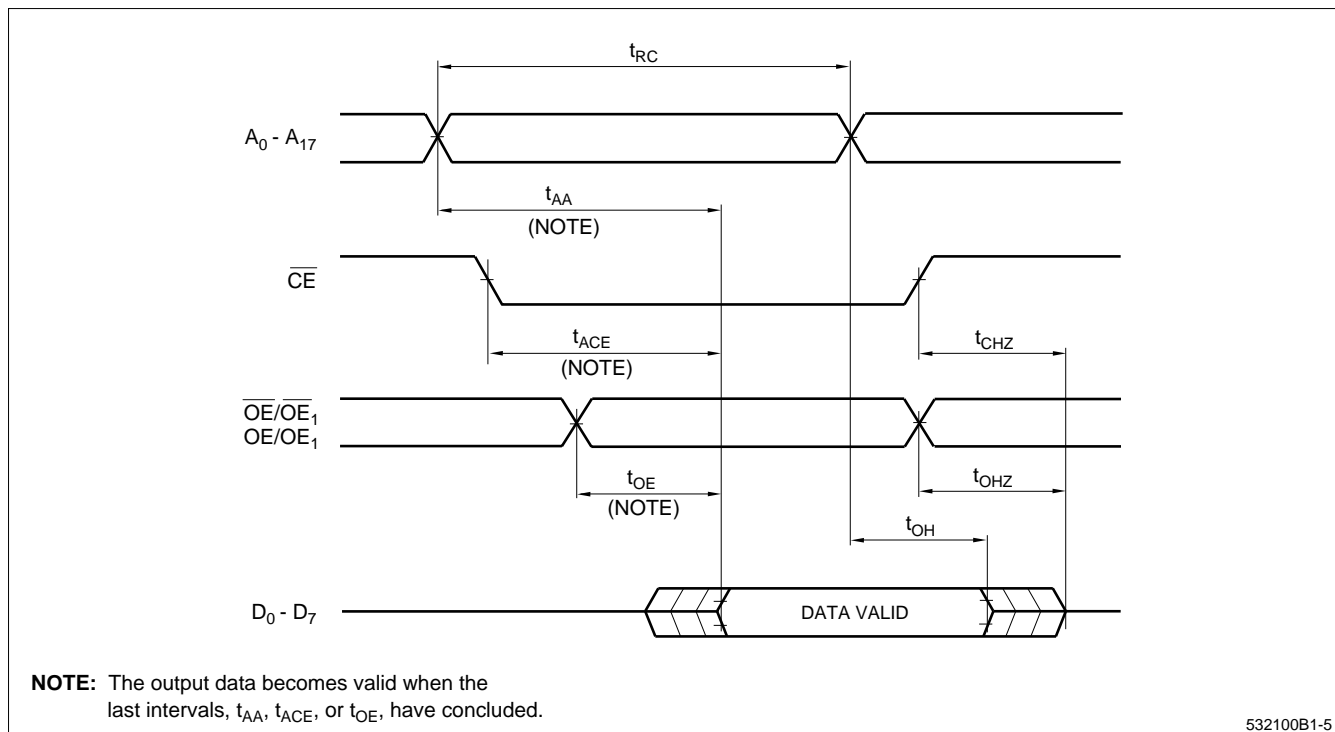
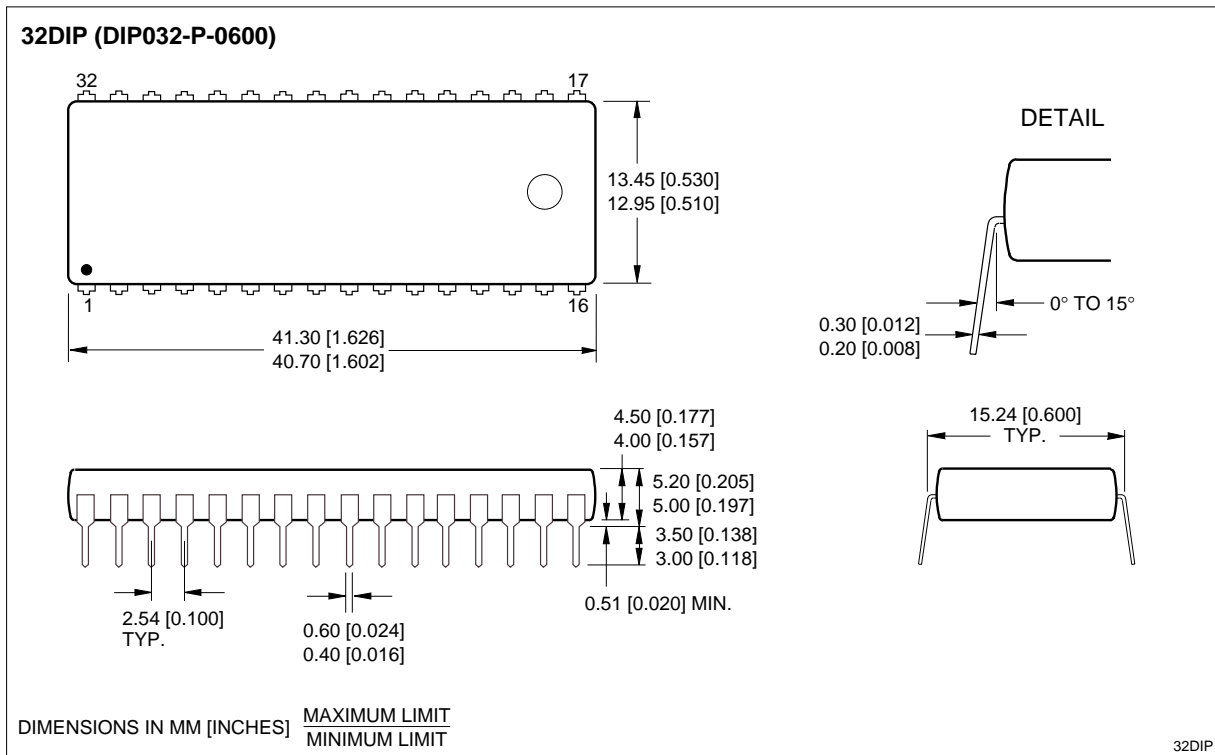
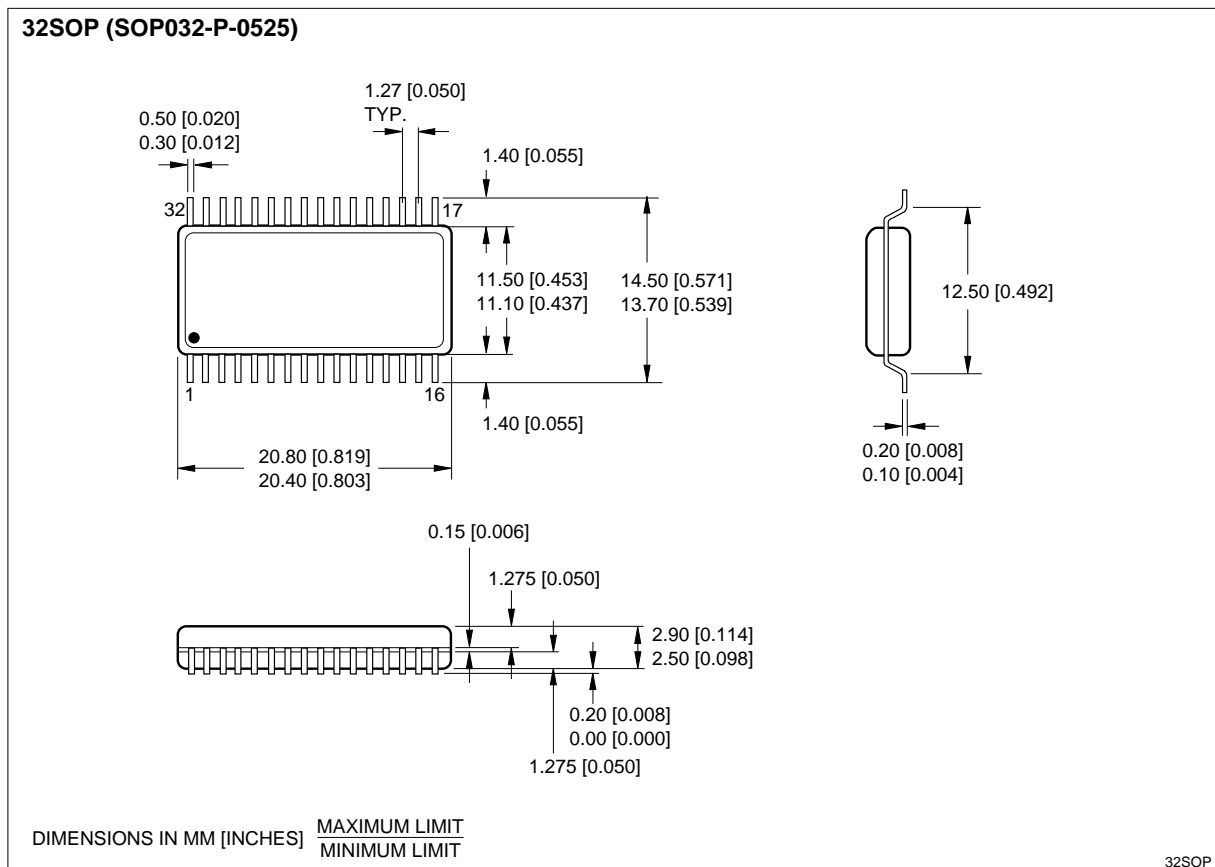


Figure 6. Timing Diagram

PACKAGE DIAGRAMS

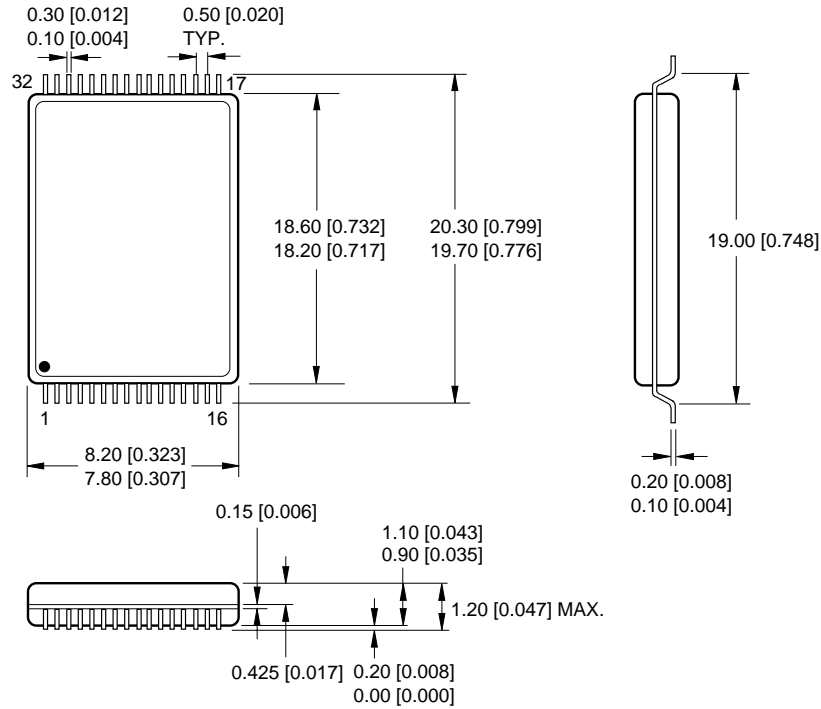


32-pin, 600-mil DIP



32-pin, 525-mil SOP

**32TSOP (Type I) (TSOP032-P-0820)**

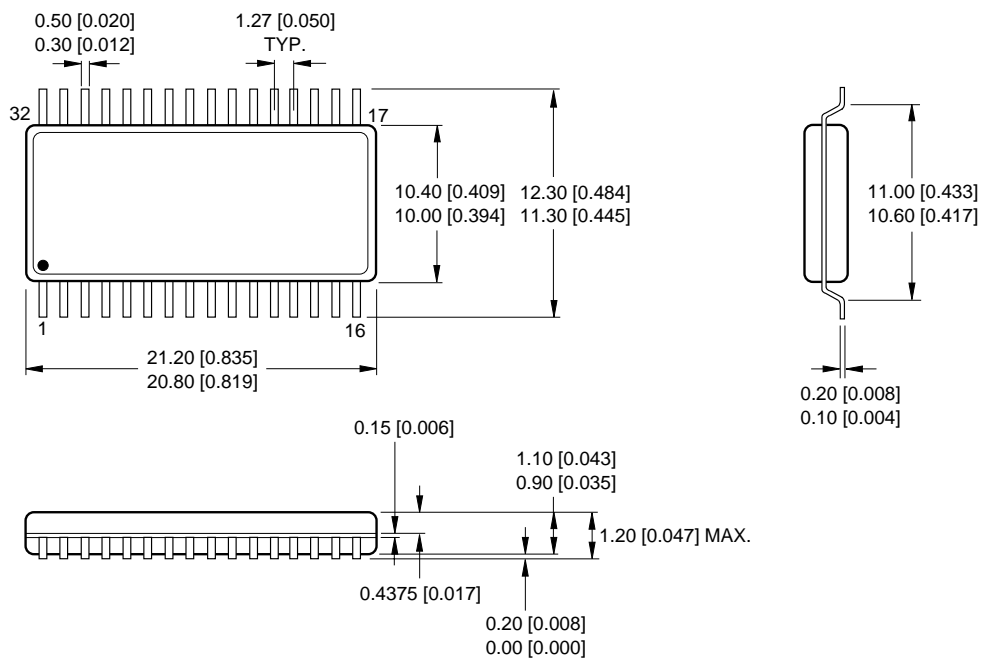


DIMENSIONS IN MM [INCHES]    MAXIMUM LIMIT  
MINIMUM LIMIT

32TSOP

**32-pin, 8 × 20 mm<sup>2</sup> TSOP (Type I)**

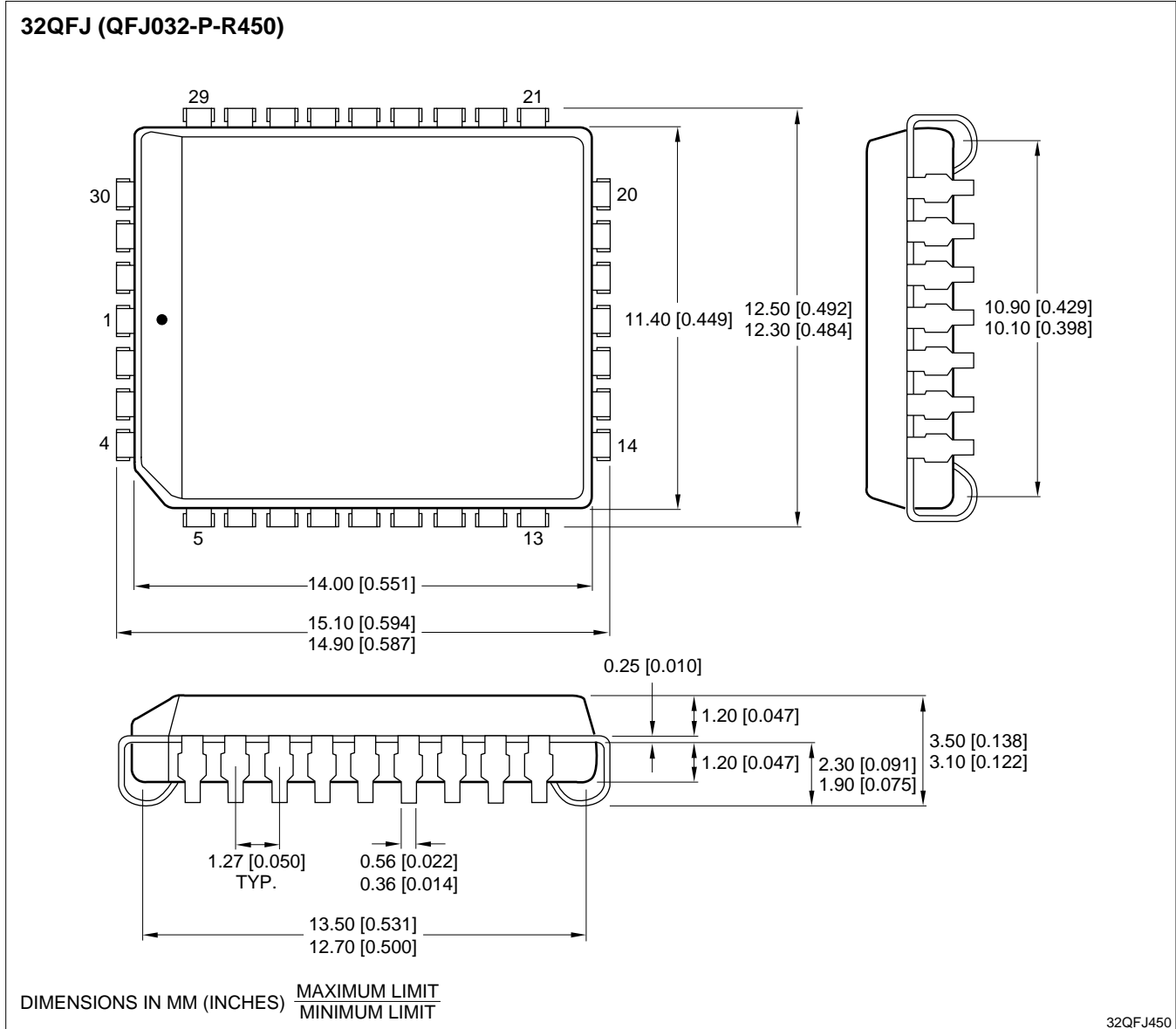
**32TSOP (Type II) (TSOP032-P-0400)**



DIMENSIONS IN MM [INCHES]    MAXIMUM LIMIT  
MINIMUM LIMIT

32TSOP400

**32-pin, 400-mil TSOP (Type II)**



**32-pin, 450-mil QFJ (PLCC)**

**ORDERING INFORMATION**

LH532100B	X	-1	
Device Type	Package	120 ns Version	
			<ul style="list-style-type: none"> <li>D 32-pin, 600-mil DIP (DIP032-P-0600)</li> <li>N 32-pin, 525-mil SOP (SOP032-P-0525)</li> <li>U 32-pin, 450-mil QFJ (PLCC) (QFJ032-P-R450)</li> <li>T 32-pin, 8 x 20 mm<sup>2</sup> TSOP (Type I) (TSOP032-P-0820)</li> <li>S 32-pin, 400-mil TSOP (Type II) (TSOP032-P-0400)</li> <li>SR 32-pin, 400-mil TSOP (Type II) Reverse bend (TSOP032-P-0400)</li> </ul>
			CMOS 2M (256K x 16) Mask-Programmable ROM
<b>Example:</b> LH532100BD-1 (CMOS 2M (256K x 8) Mask-Programmable ROM, 32-pin, 600-mil DIP)			

532100B1-6