KS0655

120 / 128 CHANNEL TFT-LCD GATE DRIVER

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Ver. 0.1

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KS0655 Specification Revision History		
Version	**Content**	**Date**
0.0	Original	Aug.1999
0.1	The contents of page 9, 10, 13 and 14 have been modified	Nov.1999

CONTENTS

INTRODUCTION

The KS0655 is a TFT-LCD gate driver having 120 / 128 outputs. It can drive TFT panel gate ON voltage up to 40 V. It can operate within the logic voltage 3.0 to 5.5 V.

FEATURES

- 120 / 128 outputs
- Maximum TFT panel gate ON voltage = 40 V
- Bi-directional shift register
- Logic supply voltage = 3.0 to 5.5 V
- TCP

BLOCK DIAGRAM

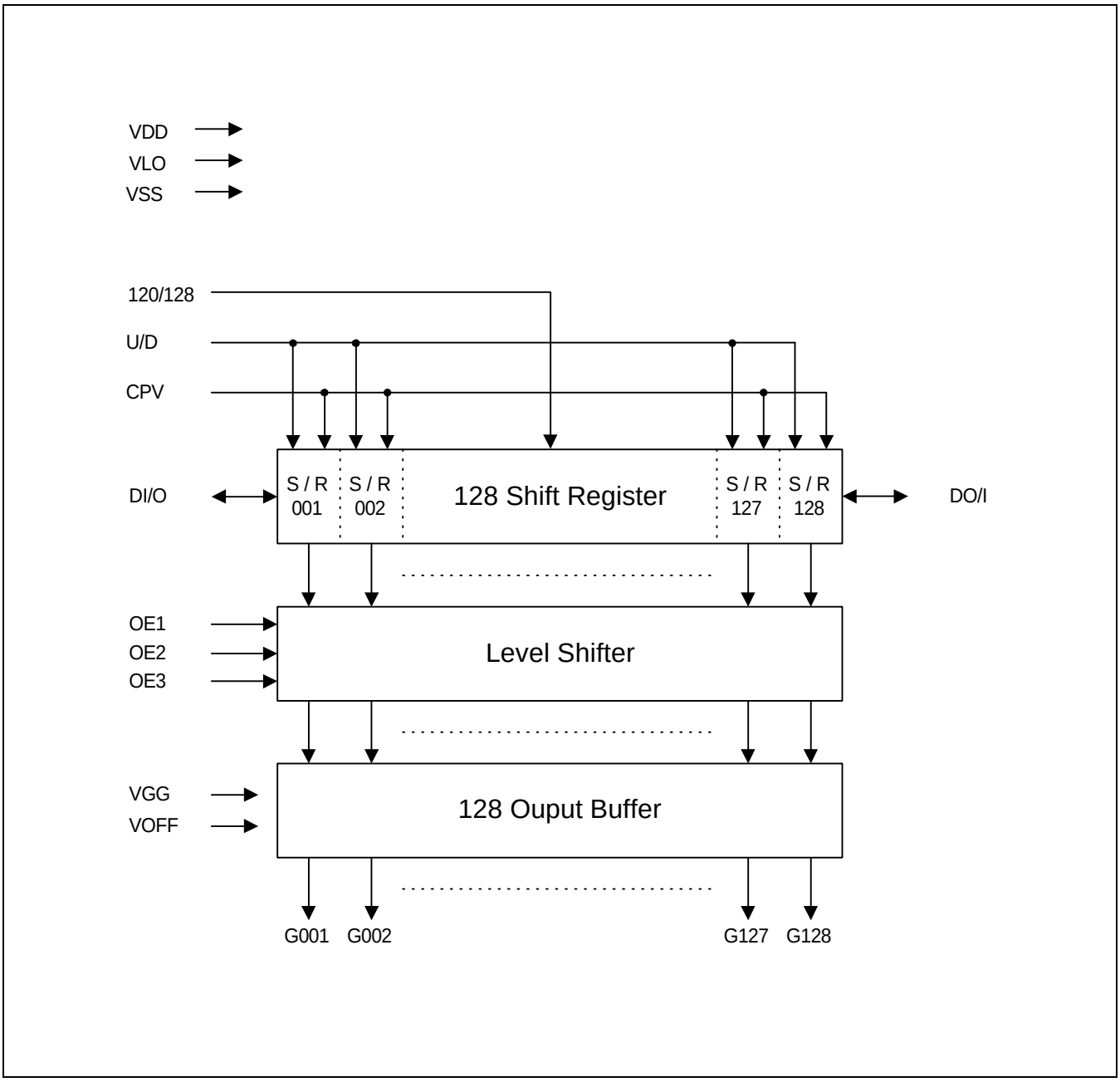

Figure 1. Block Diagram

PIN ASSIGNMENTS

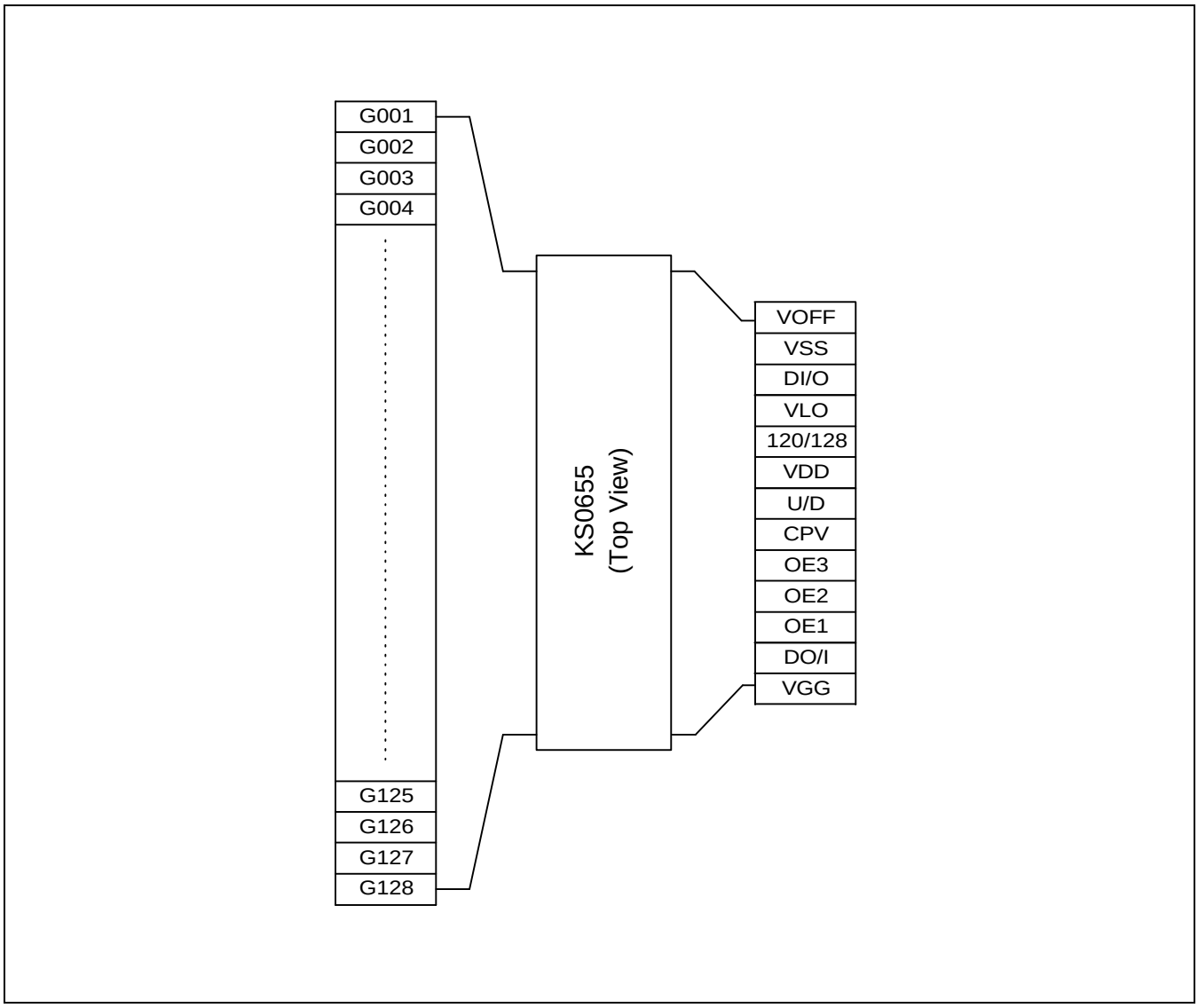

Figure 2. Pin Assignments

PIN DESCRIPTIONS

Symbol	Pin Name	I / O	Description
DI/O DO/I	Start pulse input/output	I / O	When these inputs operate as the input, the start pulse data is read at the rising edge of shift clock, CPV. When these inputs operate as the output, the start pulse output is the next chip's start pulse input. The output pulse is generated at the falling edge of the 128th shift clock, CPV. When U/D = H, the shift register does right shifting operation. (Input = DI/O and output = DO/I) When U/D = L, the shift register does left shifting operation. (Input = DO/I and output = DI/O)
U/D	Shift direction control input	I	When U/D = H, DI/O → G001 →……→ G128 → DO/I When U/D = L, DO/I → G128 →……→ G001 → DI/O
CPV	Shift clock input	I	The shift register operates in synchronization with the rising edge of this input
120/128	Output selection input	I	This input selects the number of available outputs When SEL = L, 128 output mode When SEL = H, 120 output mode(G61 - G68 are disabled)
OE1 OE2 OE3	Output enable input	I	This input controls the state of the driver outputs. When OE = H, the driver output is fixed to VOFF. When OE = L, the driver output is VGG or VOFF corresponding to the data.
G001 to G128	Driver output	O	The output signals change in synchronization with the rising edge of shift clock input, CPV. The amplitude of the driver output is VGG - VOFF.
VOFF	Gate off voltage	I	This input is TFT-LCD gate off voltage.
VLO	Logic input low voltage	I	This input operates as the reference to the level conversion of the other input. The other logic input range: VDD - VLO
VSS	Negative power supply	I	This input is logic and driver ground. Always, has negative potential.
VGG	Driver positive power supply	I	The TFT gate ON voltage is VGG - VOFF.
VDD	Logic positive power supply	I	This is the voltage source for internal logic operation.

ABSOLUTE MAXIMUM RATINGS (VSS = VOFF = 0 V)

Table 1. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Logic positive power supply	VDD	- 0.3 to 22.0	V
Driver positive power supply	VGG	- 0.3 to 45.0	V
Logic input low voltage	VLO	- 0.3 to VDD + 0.3	V
Input voltage	VIN	- 0.3 to VDD + 0.3	V
Operation temperature	Top	- 20 to 75	°C
Storage temperature	Tstg	- 55 to 150	°C

CAUTIONS

If the absolute maximum rating is exceeded momentarily, the quality of this product may be degraded.
It is desirable to use this product within the range of the absolute maximum ratings.
The power supplying order is as follows.
ON: VLO → VDD → VSS, VOFF → Control Input → VGG
OFF: VGG → Control Input → VSS, VOFF → VDD → VLO

RECOMMENDED OPERATION RATINGS (VLO = 0 V ≥ VSS = VOFF)

Table 2. Recommended Operation Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic positive power supply	VDD	3.0	-	5.5	V
Driver positive power supply	VGG	6	-	40	V
Logic negative power supply	VSS	- 15		0	V
Driver negative power supply	VOFF	- 15	-	0	V
Power supply voltage	VGG - VOFF	21	-	40	V
Operation frequency	fCPV	-	-	100	kHz
Output load	CL	-	-	500	pF

DC CHARACTERISTICS (VLO = 0 V ≥ VSS = VOFF)

Table 3. DC Characteristics
(Ta = - 20 to 75 °C, VGG - VOFF = 21 to 40 V, VLO - VSS = 15 to 0 V, VDD - VLO = 3.0 to 5.5 V)

Parameter	Symbol	Condition	Min.	Max.	Unit	Pin used
High input voltage	VIH	VX = VDD - VLO	VLO + 0.9VX	VDD	V	(1)
Low input voltage	VIL		VSS	VLO + 0.1VX	V	
High output voltage	VOH	IOH = - 40 μA	VDD - 0.4	VDD	V	(2)
Low output voltage	VOL	IOL = 40 μA	VSS	VSS + 0.4	V	
LCD driver output ON resistance	ROH	VOUT = VGG - 0.5 V, VGG = 40 V, VSS = VOFF = 0 V	-	500	Ω	G001 to G128
	ROL	VOUT = 0.5 V, VGG = 40 V, VSS = VOFF = 0 V	-	500	Ω	G001 to G128
High output current	IGG	Without output load	-	400	μA	VGG
Low output current	IDD	VDD - VSS = 3.3 V	-	400	μA	(1)
		VDD - VSS = 19 V	-	1000	μA	(3)
Input leak current	ILK	-	- 5	5	μA	(1)

NOTES:
1. DI/O, DO/I, CPV, OE1, OE2, OE3, U/D, 120/128 used.
2. When U/D = H, DO/I used, and when U/D = L, DI/O used.
3. Input swing voltage = VDD to VDD - 3.3 V

AC CHARACTERISTICS (VLO = 0 V ≥ VSS = VOFF)

Table 4. AC Characteristics
(Ta = - 20 to 75 °C, VGG - VOFF = 21 to 40 V, VLO - VSS = 15 to 0 V, VDD - VLO = 3.0 to 5.5 V)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock period	tCPV	-	10	-	µs
Clock pulse width	tCPVH, tCPVL	Duty = 50 %	4	-	
Output enable input width	twOE	-	1	-	
Data setup time	tsDI	-	700	-	ns
Data hold time	thDI	-	700	-	
Output delay time (1)	tpdDO	CL = 30 pF	-	800	
Output delay time (2)	tpdG	CL = 300 pF	-	800	
Output delay time (3)	tpdOE		-	800	

AC TIMING DIAGRAM

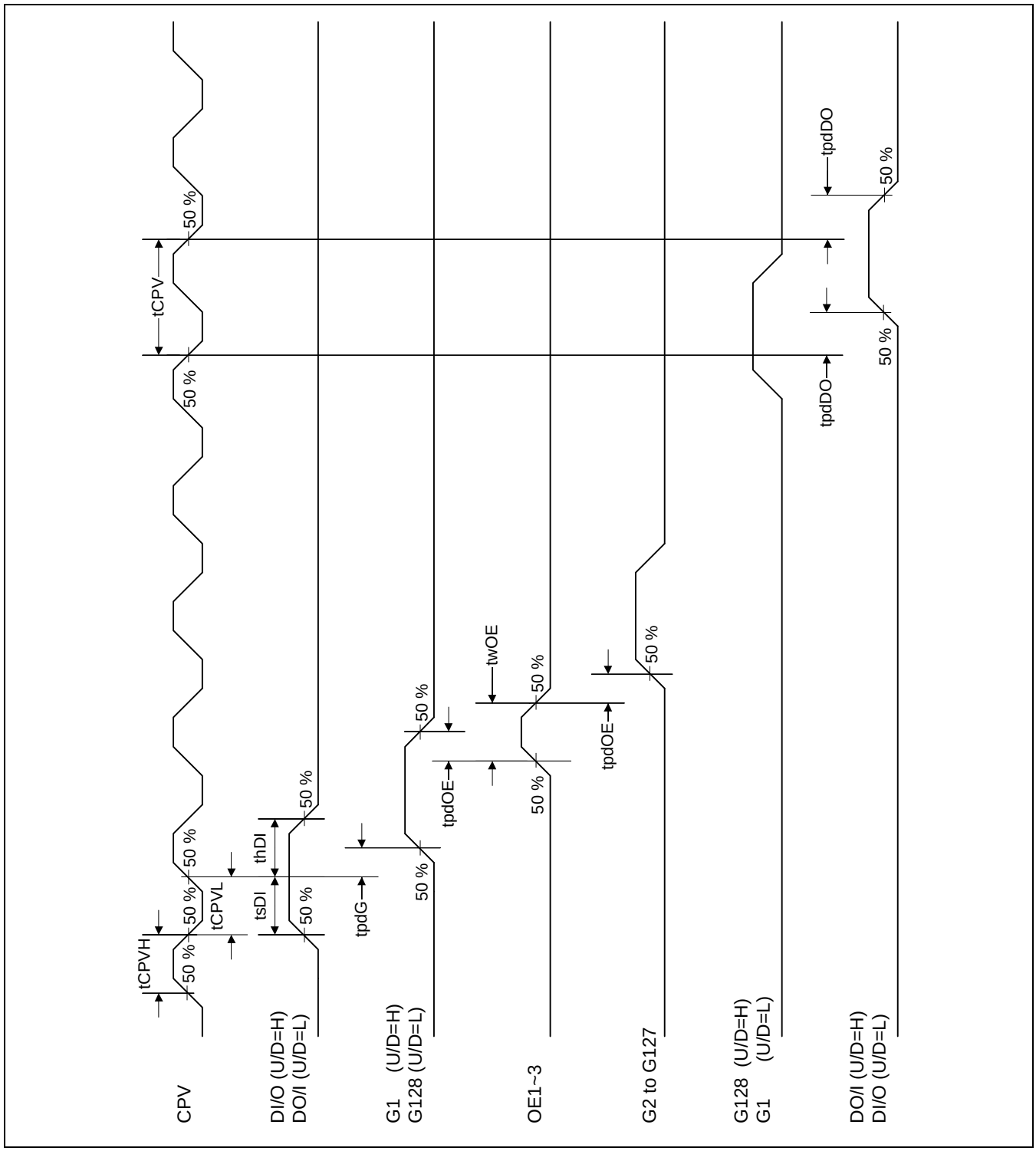

Figure 3. AC Timing Diagram

OPERATION DESCRIPTION

OPERATION METHOD

The start pulse input, DI/O (when U/D is “H”) or DO/I (when U/D = “L”), is synchronized with the rising edge of CPV and stored in the first shift register. While stored pulse is transferred to the next register at the next rising edge of CPV, a new pulse is stored simultaneously. Output pin (G1 to G128) supplies VGG voltage or VOFF voltage to the TFT-LCD panel depending on the pulse of the shift register.

The start pulse output, DO/I (when U/D is “H”) or DI/O (when U/D = “L”), is synchronized with the falling edge of CPV and the pulse of the last register (G1 or G128) is transferred to the next IC. The voltage level of the start pulse output is VDD with “H” data, VSS with “L” data

The relationship between U/D and shift data input / out pin is as follows:

Table 5. The Relationship between U/D and the Start Pulse Input / Output

Mode	U/D state	Shift data		Data transfer direction
		Input	Output	
128 output	“H”	DI/O	DO/I	G1 → G2 → G3 → G4 → G5 →……→ G128
	“L”	DO/I	DI/O	G128 → G127 → G126 → G125 →……→ G1
120 output	“H”	DI/O	DO/I	G1 → G2 →……→ G60 → G69 →……→ G127 → G128
	“L”	DO/I	DI/O	G128 → G127 →……→ G69 → G60 → ……→ G2 → G1

OUTPUT PIN (G1 TO G128)

If the data of the shift register to an output drive pin is “H”, the voltage level of the output is VGG and if the data is “L”, the level of the output is VOFF. But, when OE is “H”, the voltage level of the output is VOFF irrespective of the data of the shift register.

Table 6. The Relationship between OE and the Output Level

Condition		Mode	Output pin control	
Pin	State	120/128	Control relationship	Output level
OE1	“H”	120 Output	G1, G4, G7,……, G55, G58, G69, G72,……, G123, G126	VOFF
OE2			G2, G5, G8,……, G56, G59, G70, G73,……, G124, G127	
OE3			G3, G6, G9,……, G57, G60, G71, G74,……, G125, G128	
OE1	“L”		G1, G4, G7,……, G55, G58, G69, G72,……, G123, G126	Normal output (VGG / VOFF)
OE2			G2, G5, G8,……, G56, G59, G70, G73,……, G124, G127	
OE3			G3, G6, G9,……, G57, G60, G71, G74,……, G125, G128	
OE1	“H”	128 Output	G1, G4, G7,……, G124, G127	VOFF
OE2			G2, G5, G8,……, G125, G128	
OE3			G3, G6, G9,……, G126	
OE1	“L”		G1, G4, G7,……, G124, G127	Normal output (VGG / VOFF)
OE2			G2, G5, G8,……, G125, G128	
OE3			G3, G6, G9,……, G126	

VOLTAGE BIASING

The driver negative power supply, VSS, can be any value between VLO and VLO - 15V.

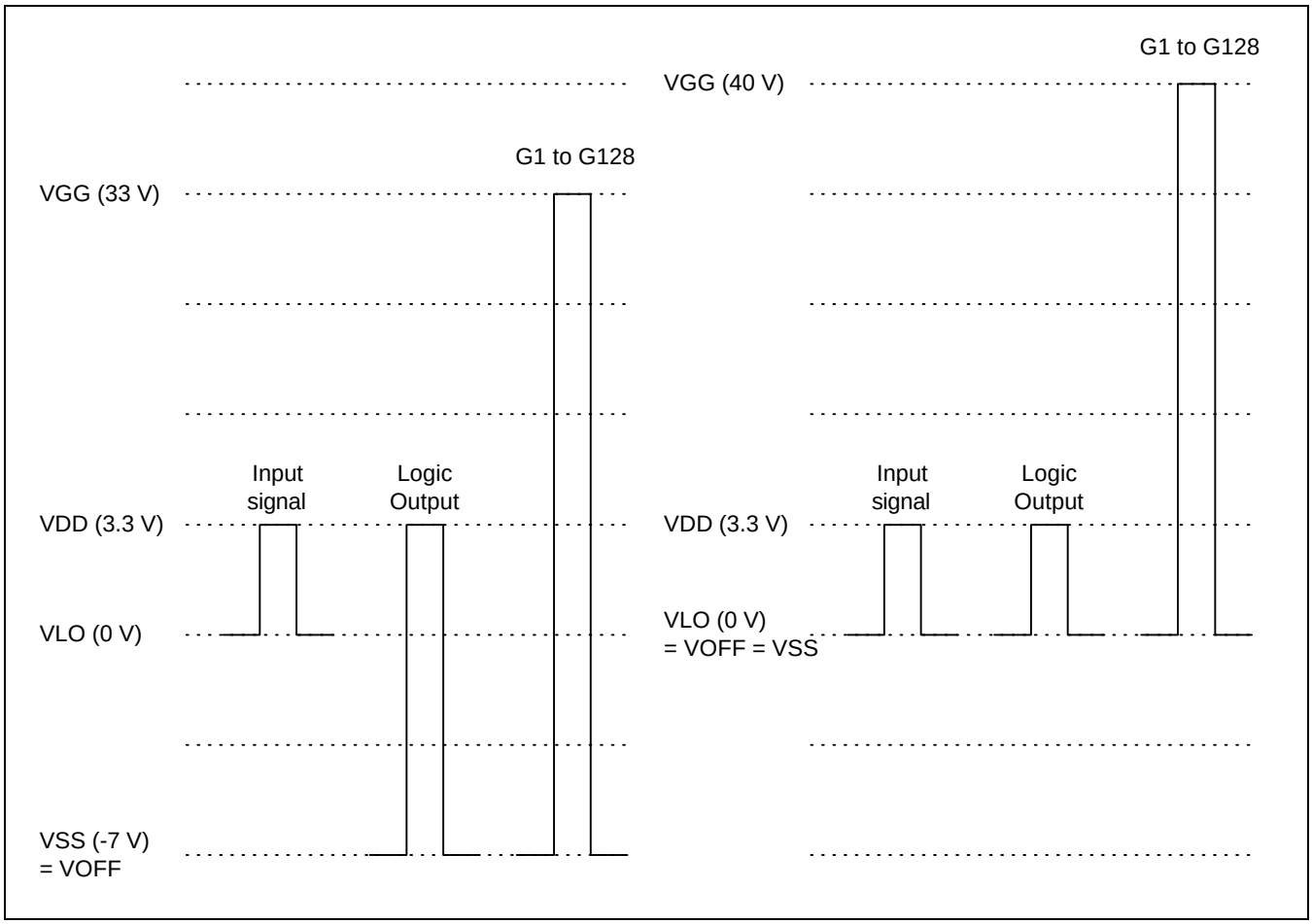

Figure 4. Example of Voltage Biasing

RECOMMENDED TIMING

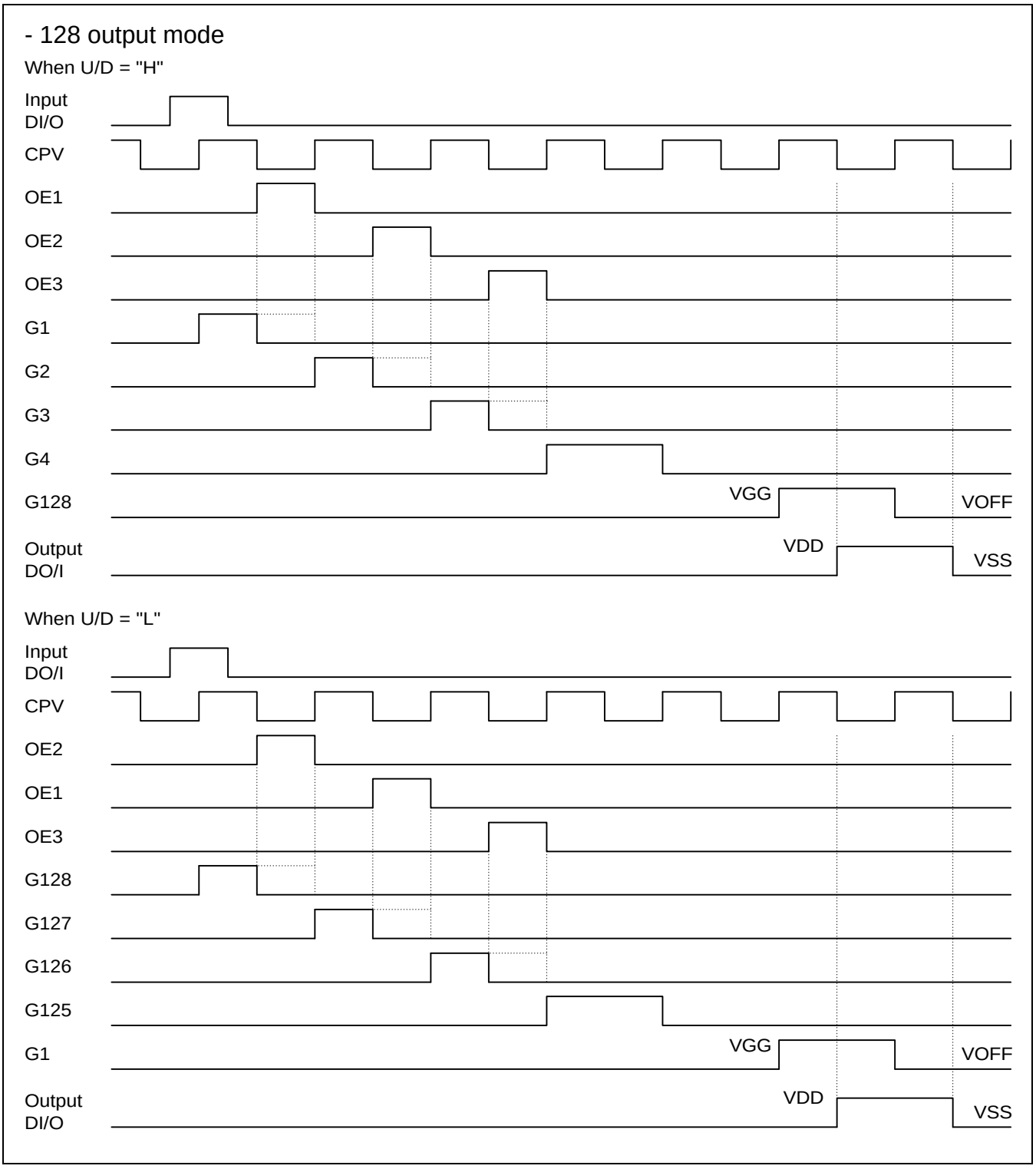

Figure 5. Recommended Timing

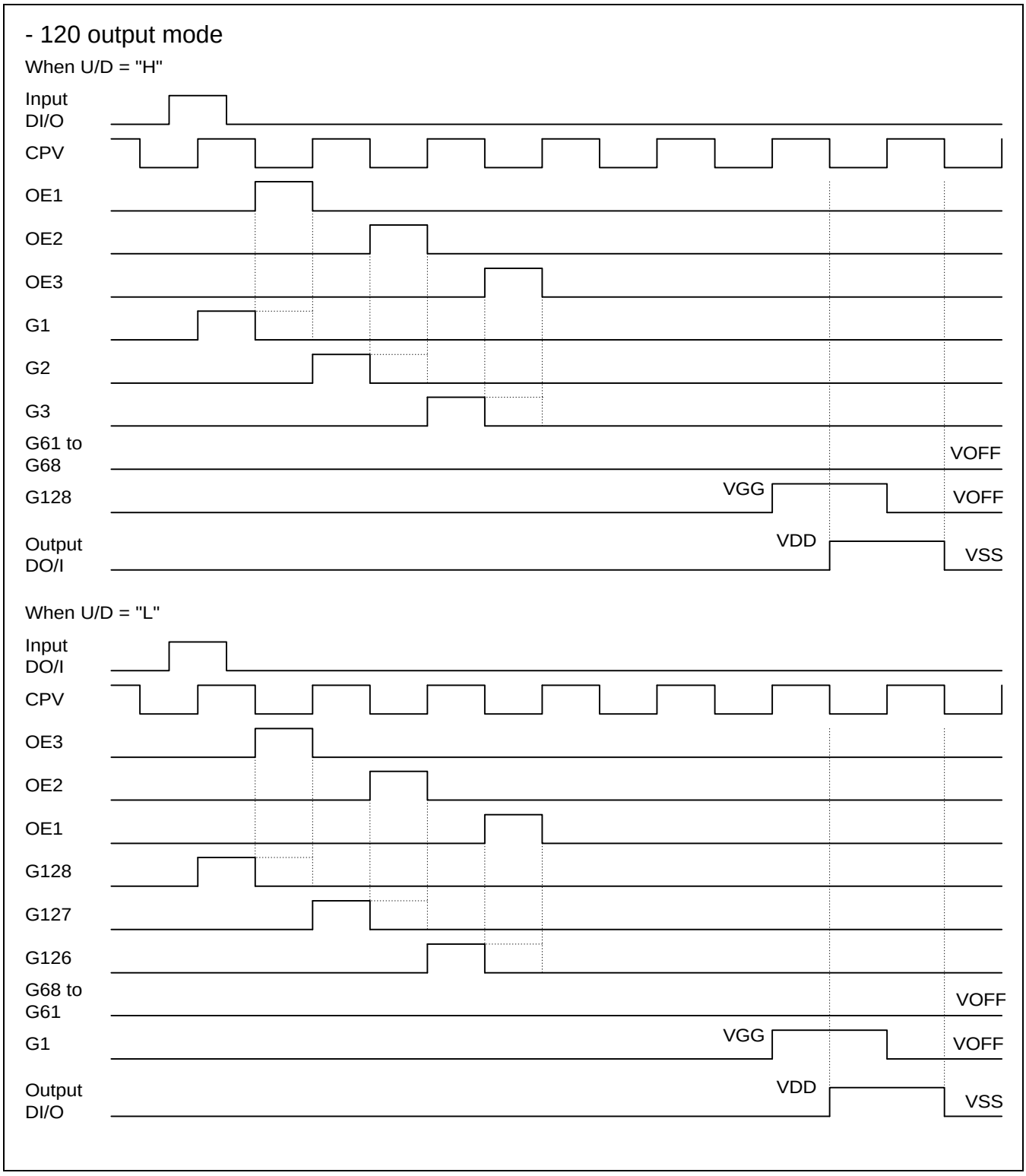

Figure 5. Recommended Timing (Continued)

NOTES