

## Features

- Operating voltage: 5.0V
- Long delay time
  - 0.8 seconds (SEL=VSS, 256K DRAM)
  - 0.2 seconds (SEL=VDD/open, 64K DRAM)
- 25kHz sampling rate
- Continuous variable delay time
- Built-in pre-amplifier
- Low distortion
- High S/N ratio
- Wide frequency response
- PCM 10-bit A/D and D/A converters
- 24-pin DIP package

## Applications

- Mixers
- Karaoke systems
- Echo generators
- Sound effect generators

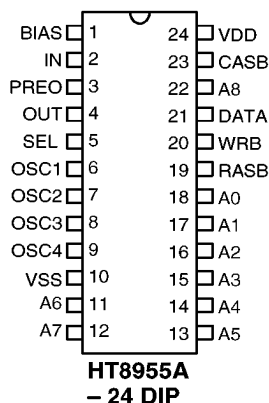
## General Description

The HT8955A is a CMOS LSI digital audio signal delay processor. It is designed for audio system applications including echo generators, karaoke systems, sound effect generators, etc.

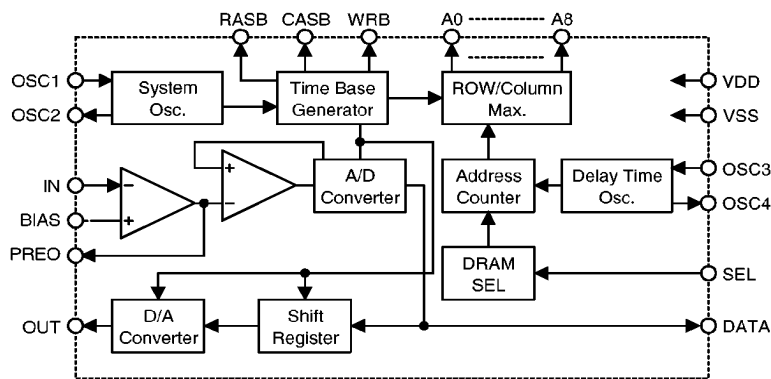
The chip consists of a built-in pre-amplifier, on-chip oscillator, DRAM interface, 10-bit A/D and D/A converters as well as control logic. It provides continuously adjustable delay time up to 0.8/0.2 seconds at a sampling rate of 25kHz.

when combined with an external DRAM (41256/4164). The HT8955A is superior to a conventional BBD delay unit in its low distortion, high S/N ratio and long delay time. Its sophisticated low pass filter will not end in the normal applications due to the high sampling rate (25~50kHz). Hence, the HT8955A is excellent for audio delay system applications. It is offered in a 24-pin dual-in-line package.

## Pin Assignment

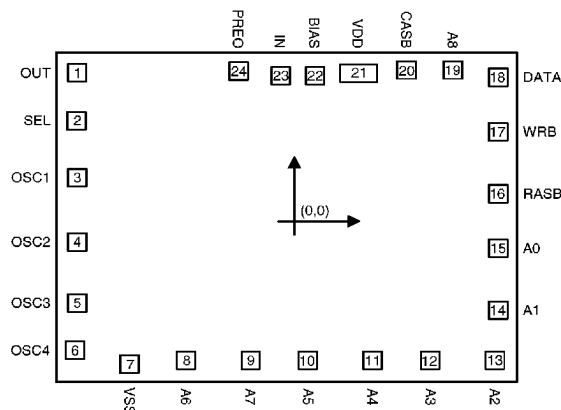


### Block Diagram



## Pad Coordinates

Unit:  $\mu\text{m}$



| Pad No. | X        | Y       | Pad No. | X       | Y       |
|---------|----------|---------|---------|---------|---------|
| 1       | -1138.00 | 796.50  | 14      | 1141.50 | -547.00 |
| 2       | -1141.00 | 523.50  | 15      | 1141.50 | -197.50 |
| 3       | -1136.50 | 201.50  | 16      | 1141.50 | 111.50  |
| 4       | -1136.50 | -163.00 | 17      | 1141.50 | 461.00  |
| 5       | -1137.00 | -507.00 | 18      | 1141.50 | 770.50  |
| 6       | -1149.00 | -774.00 | 19      | 896.00  | 811.00  |
| 7       | -854.50  | -853.50 | 20      | 645.00  | 810.50  |
| 8       | -548.00  | -831.50 | 21      | 435.00  | 794.00  |
| 9       | -198.50  | -831.50 | 21      | 335.00  | 794.00  |
| 10      | 111.50   | -831.50 | 22      | 150.00  | 779.00  |
| 11      | 461.00   | -831.50 | 23      | -35.00  | 779.00  |
| 12      | 773.00   | -831.50 | 25      | -264.00 | 806.00  |
| 13      | 1122.50  | -831.50 |         |         |         |

Chip size:  $2170 \times 2200 (\mu\text{m})^2$

\* The IC substrate should be connected to VSS in the PCB layout artwork.

## Pin Description

| Pin No. | Pin Name | I/O | Internal Connection | Description                                                       |
|---------|----------|-----|---------------------|-------------------------------------------------------------------|
| 1       | BIAS     | O   | OP Non-inverted     | Internal pre-amplifier bias<br>Connects to a decoupling capacitor |
| 2       | IN       | I   | OP Inverted         | Audio signal input pin (inverted)                                 |
| 3       | PREO     | O   | OP OUTPUT           | Pre-amplifier output pin                                          |
| 4       | OUT      | O   | —                   | Delayed audio signal output pin                                   |
| 5       | SEL      | I   | Pull-High           | DRAM type selection:<br>VDD or Open: 64Kb<br>VSS: 256Kb           |
| 6       | OSC1     | I   | —                   | System oscillator input                                           |
| 7       | OSC2     | O   | —                   | System oscillator output                                          |
| 8       | OSC3     | I   | —                   | Delay time control oscillator input                               |
| 9       | OSC4     | O   | —                   | Delay time control oscillator output                              |
| 10      | VSS      | I   | —                   | Negative power supply (GND)                                       |
| 11      | A6       | O   | CMOS OUT            | Connects to DRAM A6                                               |
| 12      | A7       | O   | CMOS OUT            | Connects to DRAM A7                                               |

| Pin No. | Pin Name | I/O | Internal Connection | Description           |
|---------|----------|-----|---------------------|-----------------------|
| 13      | A5       | O   | CMOS OUT            | Connects to DRAM A5   |
| 14      | A4       | O   | CMOS OUT            | Connects to DRAM A4   |
| 15      | A3       | O   | CMOS OUT            | Connects to DRAM A3   |
| 16      | A2       | O   | CMOS OUT            | Connects to DRAM A2   |
| 17      | A1       | O   | CMOS OUT            | Connects to DRAM A1   |
| 18      | A0       | O   | CMOS OUT            | Connects to DRAM A0   |
| 19      | RASB     | O   | CMOS OUT            | Connects to DRAM RASB |
| 20      | WRB      | O   | CMOS OUT            | Connects to DRAM WRB  |
| 21      | DATA     | I/O | CMOS I/O            | Data I/O pin          |
| 22      | A8       | O   | CMOS I/O            | Connects to DRAM A8   |
| 23      | CASB     | O   | CMOS I/O            | Connects to DRAM CASB |
| 24      | VDD      | I   | —                   | Positive power supply |

### Absolute Maximum Ratings\*

Supply Voltage ..... -0.3V to 6V      Storage Temperature ..... -50°C to 125°C  
Input Voltage .....  $V_{SS}-0.3V$  to  $V_{DD}+0.3V$       Operating Temperature ..... -20°C to 70°C

\*Note: These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

### Electrical Characteristics

(Ta=25°C)

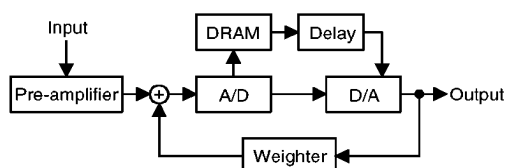
| Symbol          | Parameter                  | Test Conditions |                                      | Min. | Typ. | Max.               | Unit |
|-----------------|----------------------------|-----------------|--------------------------------------|------|------|--------------------|------|
|                 |                            | V <sub>DD</sub> | Conditions                           |      |      |                    |      |
| V <sub>DD</sub> | Operating Voltage          | —               | —                                    | 4.5  | 5.0  | 5.5                | V    |
| I <sub>OP</sub> | Operating Current          | 5V              | No load,<br>f <sub>OSC</sub> =640kHz | —    | 2.5  | 8                  | mA   |
| A <sub>v</sub>  | Pre-amplifier Voltage Gain | 5V              | R <sub>L</sub> >100kΩ<br>Open loop   | —    | 2000 | —                  | V/V  |
| A <sub>v</sub>  | Comparator Voltage Gain    | 5V              | R <sub>L</sub> >100kΩ<br>Open loop   | —    | 2000 | —                  | V/V  |
| V <sub>IL</sub> | “L” Input Voltage          | —               | —                                    | 0    | —    | 0.3V <sub>DD</sub> | V    |

| Symbol            | Parameter                 | Test Conditions |                                       | Min.               | Typ. | Max.            | Unit |
|-------------------|---------------------------|-----------------|---------------------------------------|--------------------|------|-----------------|------|
|                   |                           | V <sub>DD</sub> | Conditions                            |                    |      |                 |      |
| V <sub>IH</sub>   | “H” Input Voltage         | —               | —                                     | 0.7V <sub>DD</sub> | —    | V <sub>DD</sub> | V    |
| V <sub>OMAX</sub> | Maximum Output Voltage    | 5V              | R <sub>L</sub> >470kΩ                 | 1                  | 1.5  | —               | V    |
| T <sub>d</sub>    | Maximum Delay Time        | 5V              | SEL=open, 25kHz sampling rate         | 0.15               | 0.2  | —               | s    |
| T <sub>d</sub>    |                           | 5V              | SEL=VSS, 25kHz sampling rate          | 0.6                | 0.8  | —               | s    |
| S/N               | Signal to Noise Ratio     | 5V              | V <sub>O</sub> =1V, 400Hz<br>BW=10kHz | —                  | 55   | —               | dB   |
| THD               | Total Harmonic Distortion | 5V              | V <sub>O</sub> =1V, 400Hz<br>BW=7kHz  | —                  | 0.5  | —               | %    |

## Functional Description

The HT8955A is a single chip LSI with an external DRAM. It is designed for processing audio signal delay. The chip includes a built-in pre-amplifier, 10-bit A/D and D/A converters. The A/D and D/A converters ensure low distortion as well as high S/N ratio of the audio delay system. The chip also provides two sets of oscillation circuit for system sampling rate and audio echo delay time.

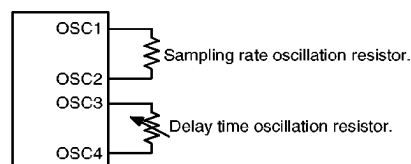
### Playing function block diagram



### System oscillator

The HT8955A provides two oscillators, one for the sampling rate and one for echo delay time. The sampling rate oscillator requires an external resistor between the OSC1 and OSC2 pins. A higher sampling rate (25~50kHz) can thus be derived by adjusting the oscillation resistor without having a sophisticated low pass filter. The delay time oscillator, on the other hand,

demands an external resistor between the OSC3 and OSC4 pins. By altering the oscillation resistor, its delay time can be continuously adjusted up to 0.8/0.2 seconds at a 25kHz sampling rate for DRAM of 256Kb/64Kb.



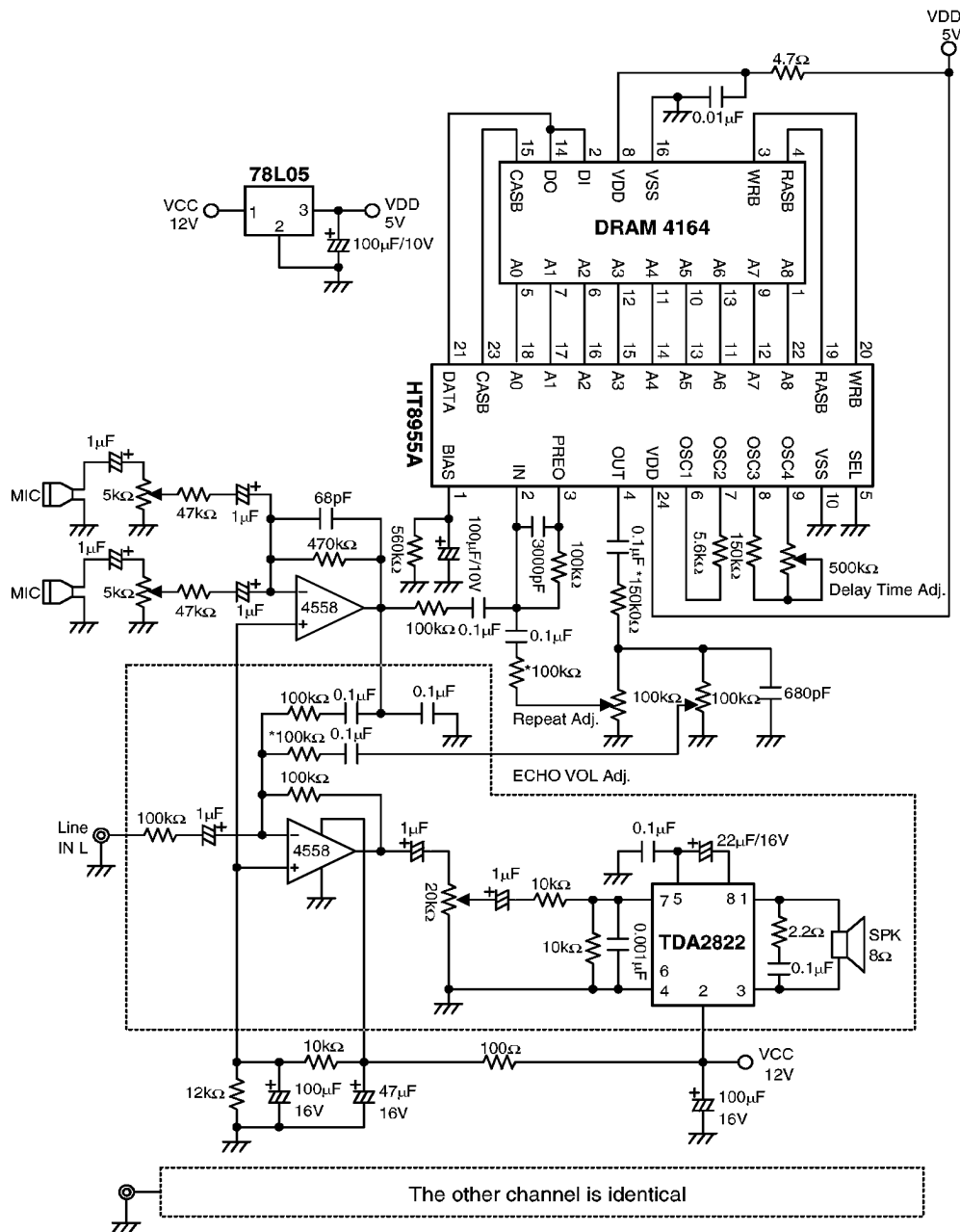
### DRAM selection

The HT8955A can interface with a DRAM for storing delay signals. The type along with the maximum delay time of DRAM is determined by the status of the SEL pin as shown:

| SEL Connection | DRAM Type | Delay Time  |
|----------------|-----------|-------------|
| VDD or Open    | 64Kb      | 0.2 seconds |
| VSS            | 256Kb     | 0.8 seconds |

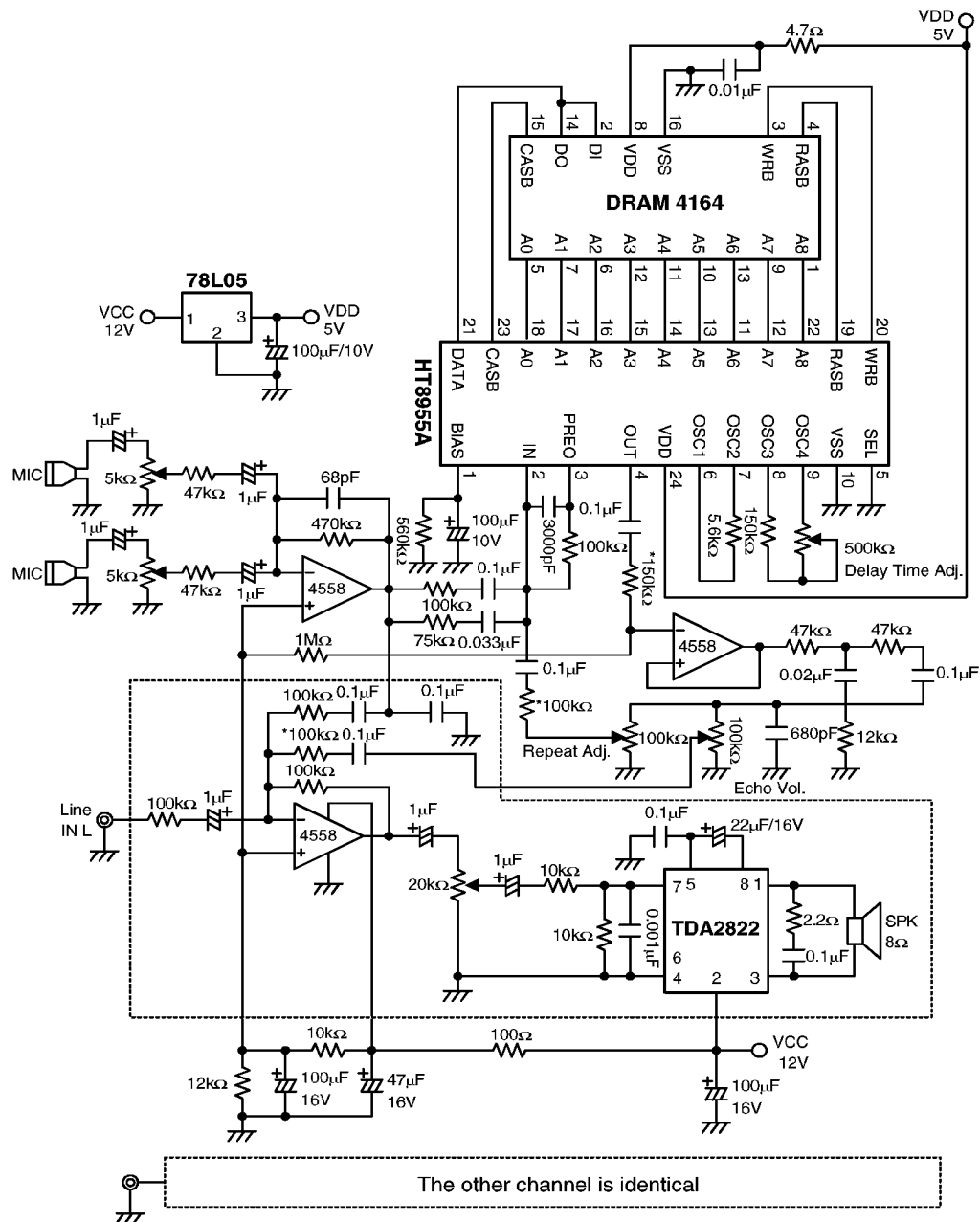


**Basic KARAOKE system**



\*Note: In practical applications, the value of the marked part may be adjusted to the desired effect

### Basic KARAOKE system with pre-emphasis



\*Note: In practical applications, the value of the marked part may be adjusted to the desired effect