
HM628127HB Series

131072-word × 8-bit High Speed CMOS Static RAM

HITACHI

ADE-203-350C (Z)
Rev. 3.0
Nov. 19, 1996

Description

The HM628127HB is an asynchronous high speed static RAM organized as 128-k word × 8-bit. It realize high speed access time (15/20 ns) with employing 0.8 μm shrink CMOS process and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. The HM628127HB is packaged in 400-mil 32-pin SOJ for high density surface mounting.

Features

- Single 5 V supply
- Access time 15/20 ns (max)
- Completely static memory
 - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible
 - All inputs and outputs
- 400-mil 32-pin SOJ package
- Center V_{CC} and V_{SS} type pinout

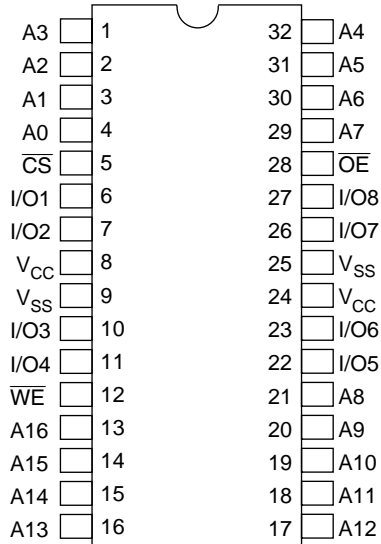
Ordering Information

Type No.	Access time	Package
HM628127HBJP-15	15 ns	400-mil 32-pin plastic SOJ (CP-32DB)
HM628127HBJP-20	20 ns	
HM628127HBLJP-15	15 ns	
HM628127HBLJP-20	20 ns	

HM628127HB Series

Pin Arrangement

HM628127HBJP/HBLJP Series

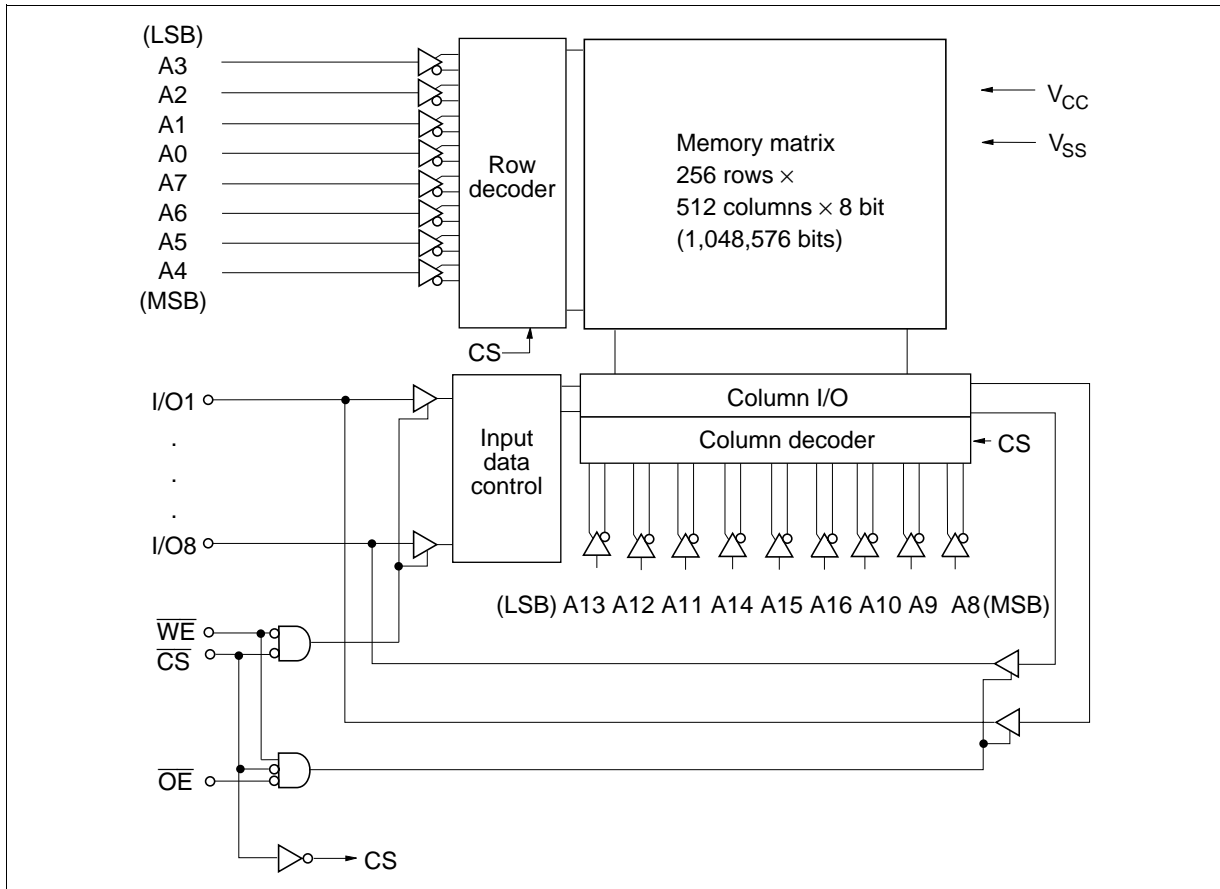


(Top view)

Pin Description

Pin Name	Function
A0 to A16	Address input
I/O1 to I/O8	Data input/output
CS	Chip select
OE	Output enable
WE	Write enable
V _{CC}	Power supply
V _{SS}	Ground

Block Diagram



Function Table

\overline{CS}	\overline{OE}	\overline{WE}	Mode	V _{CC} current	I/O	Ref. cycle
H	x	x	Standby	I _{SB} , I _{SB1}	High-Z	—
L	H	H	Output disable	I _{CC}	High-Z	—
L	L	H	Read	I _{CC}	Dout	Read cycle (1) to (3)
L	H	L	Write	I _{CC}	Din	Write cycle (1)
L	L	L	Write	I _{CC}	Din	Write cycle (2)

Note: x: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	-0.5 to +7.0	V
Voltage on any pin relative to V_{SS}	V_T	-0.5*1 to $V_{CC}+0.5$	V
Power dissipation	P_T	$1.0^{*2}/1.5^{*3}$	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C
Storage temperature under bias	T_{bias}	-10 to +85	°C

- Notes: 1. V_T min = -2.5 V for pulse width (under shoot) \leq 10 ns
2. At still air condition
3. At air flow \geq 1.0 m/s

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}^{*2}	4.5	5.0	5.5	V
	V_{SS}^{*3}	0	0	0	V
Input voltage	V_{IH}	2.2	—	$V_{CC} + 0.5$	V
	V_{IL}	-0.5*1	—	0.8	V

- Notes: 1. V_{IL} min = -2.0 V for pulse width (under shoot) \leq 10 ns
2. The supply voltage with all V_{CC} pins must be on the same level.
3. The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$)

Parameter		Symbol	Min	Typ* ¹	Max	Unit	Test conditions
Input leakage current		$ I_{LI} $	—	—	2	μA	$V_{in} = V_{SS}$ to V_{CC}
Output leakage current		$ I_{LO} $	—	—	2	μA	$V_{in} = V_{SS}$ to V_{CC}
Operation power supply current	15 ns cycle	I_{CC}	—	120	180	mA	$\overline{CS} = V_{IL}$, $I_{out} = 0$ mA Other inputs = V_{IH}/V_{IL}
	20 ns cycle	I_{CC}	—	100	150		
Standby power supply current	15 ns cycle	I_{SB}	—	55	100	mA	$\overline{CS} = V_{IH}$, Other inputs = V_{IH}/V_{IL}
	20 ns cycle	I_{SB}	—	45	80		
		I_{SB1}	—	—	2	mA	$V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2\text{V}$, (1) $0\text{V} \leq V_{in} \leq 0.2\text{V}$ or (2) $V_{CC} \geq V_{in} \geq V_{CC} - 0.2\text{V}$
			—* ²	—* ²	0.2* ²		
Output voltage		V_{OL}	—	—	0.4	V	$I_{OL} = 8$ mA
		V_{OH}	2.4	—	—	V	$I_{OH} = -4$ mA

- Notes: 1. Typical values are at $V_{CC} = 5.0\text{V}$, $T_a = +25^\circ\text{C}$ and not guaranteed.
 2. This characteristics is guaranteed only for L-version.

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance* ¹		C_{in}	—	—	6	pF	$V_{in} = 0\text{V}$
Input/output capacitance* ¹		$C_{I/O}$	—	—	8	pF	$V_{I/O} = 0\text{V}$

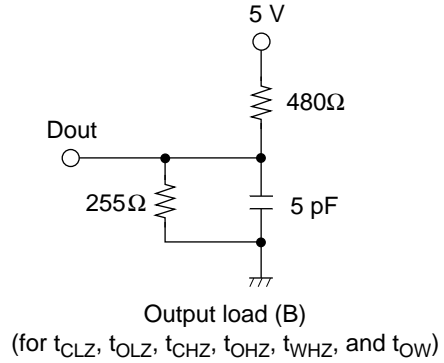
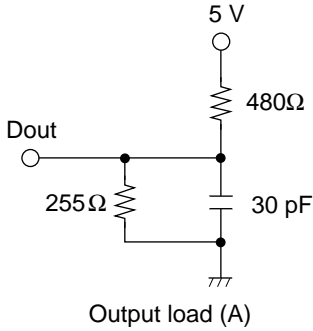
- Note: 1. This parameter is sampled and not 100% tested.

HM628127HB Series

AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0 V to 3.0 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.5V
- Output load: See figures (Including scope and jig)



Read Cycle

Parameter	Symbol	HM628127HB-15		HM628127HB-20		Unit	Notes
		Min	Max	Min	Max		
Read cycle time	t_{RC}	15	—	20	—	ns	
Address access time	t_{AA}	—	15	—	20	ns	
Chip select access time	t_{ACS}	—	15	—	20	ns	
Output enable to output valid	t_{OE}	—	8	—	10	ns	
Output hold from address change	t_{OH}	5	—	5	—	ns	
Chip select to output in low-Z	t_{CLZ}	3	—	3	—	ns	1
Output enable to output in low-Z	t_{OLZ}	1	—	1	—	ns	1
Chip deselect to output in high-Z	t_{CHZ}	—	7	—	7	ns	1
Output disable to output in high-Z	t_{OHZ}	—	7	—	7	ns	1
Chip selection to power up time	t_{PU}	0	—	0	—	ns	
Chip selection to power down time	t_{PD}	—	15	—	20	ns	

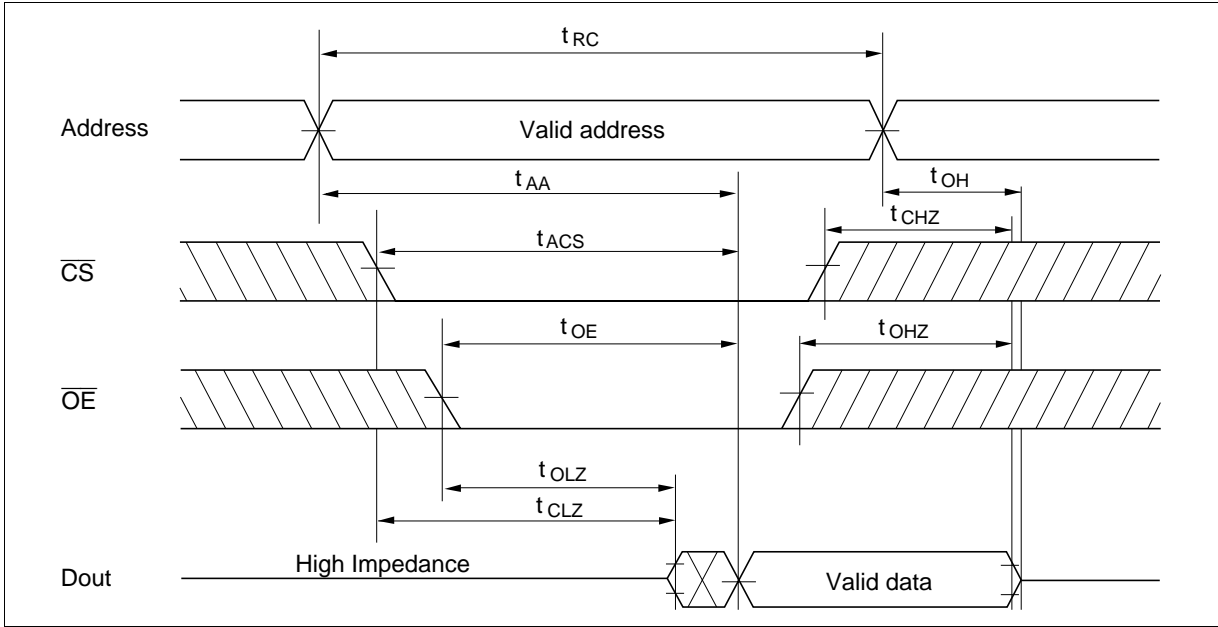
Write Cycle

Parameter	Symbol	HM628127HB-15		HM628127HB-20		Unit	Notes
		Min	Max	Min	Max		
Write cycle time	t_{WC}	15	—	20	—	ns	
Address valid to end of write	t_{AW}	12	—	15	—	ns	
Chip select to end of write	t_{CW}	10	—	12	—	ns	9
Write pulse width	t_{WP}	10	—	12	—	ns	8
Address setup time	t_{AS}	0	—	0	—	ns	6
Write recovery time	t_{WR}	0	—	0	—	ns	7
Data to write time overlap	t_{DW}	8	—	10	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	ns	
Write disable to output in low-Z	t_{OW}	3	—	3	—	ns	1
Output disable to output in high-Z	t_{OHZ}	—	7	—	7	ns	1
Write enable to output in high-Z	t_{WHZ}	—	7	—	7	ns	1

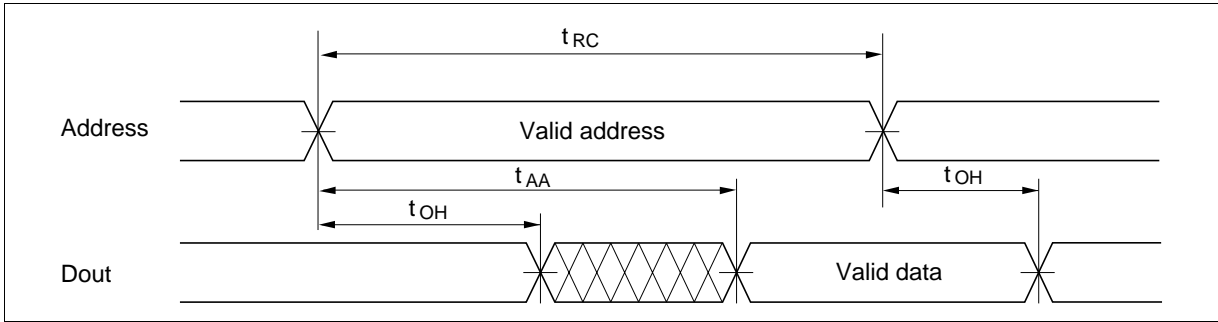
- Note:
1. Transition is measured ± 200 mV from steady voltage with Load (B). This parameter is sampled and not 100% tested.
 2. Address should be valid prior to or coincident with \overline{CS} transition low.
 3. \overline{WE} and/or \overline{CS} must be high during address transition time.
 4. if \overline{CS} and \overline{OE} are low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
 5. If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} transition, output remains a high impedance state.
 6. t_{AS} is measured from the latest address transition to the later of \overline{CS} or \overline{WE} going low.
 7. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the first address transition.
 8. A write occurs during the overlap of a low \overline{CS} and a low \overline{WE} . A write begins at the latest transition among \overline{CS} going low and \overline{WE} going low. A write ends at the earliest transition among \overline{CS} going high and \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
 9. t_{CW} is measured from the later of \overline{CS} going low to the the end of write.

Timing Waveforms

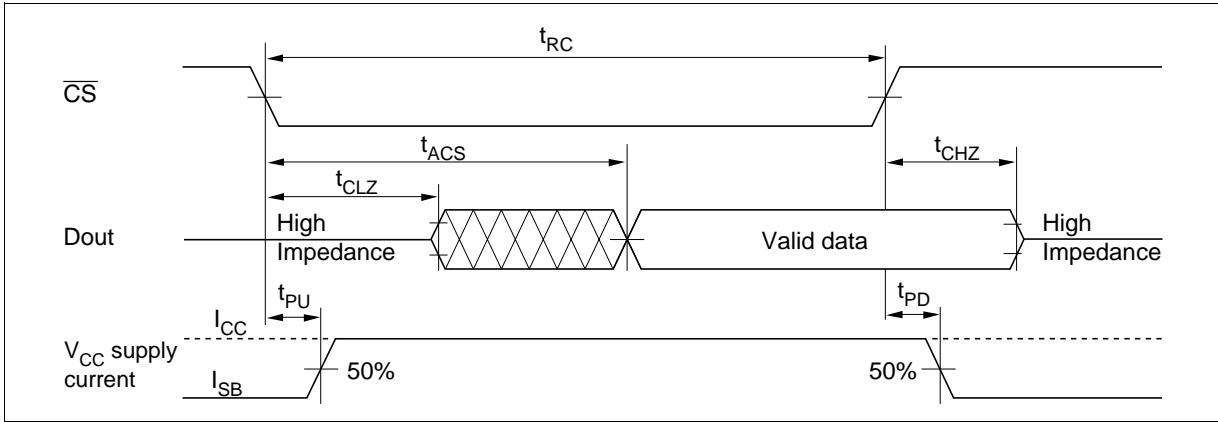
Read Timing Waveform (1) ($\overline{WE} = V_{IH}$)



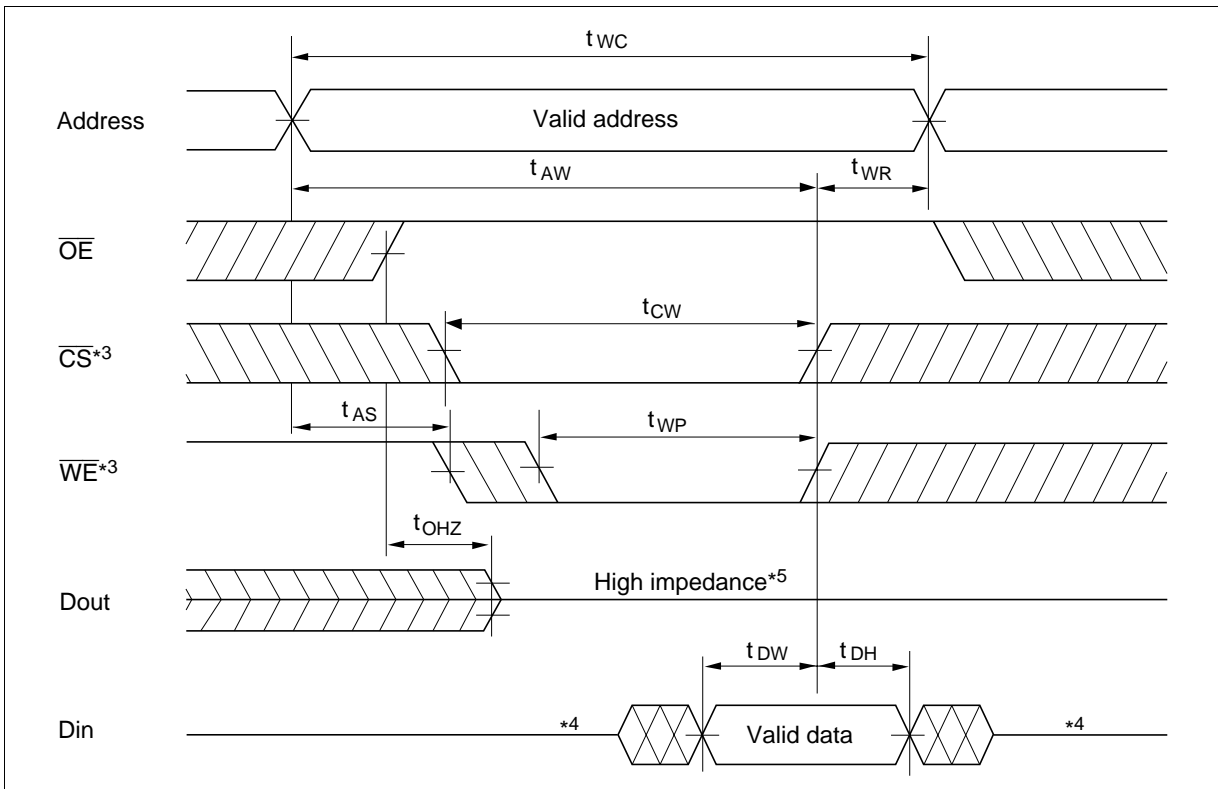
Read Timing Waveform (2) ($\overline{WE} = V_{IH}$, $\overline{CS} = V_{IL}$, $\overline{OE} = V_{IL}$)



Read Timing Waveform (3) ($\overline{WE} = V_{IH}, \overline{CS} = V_{IL}, \overline{OE} = V_{IL}$)*2

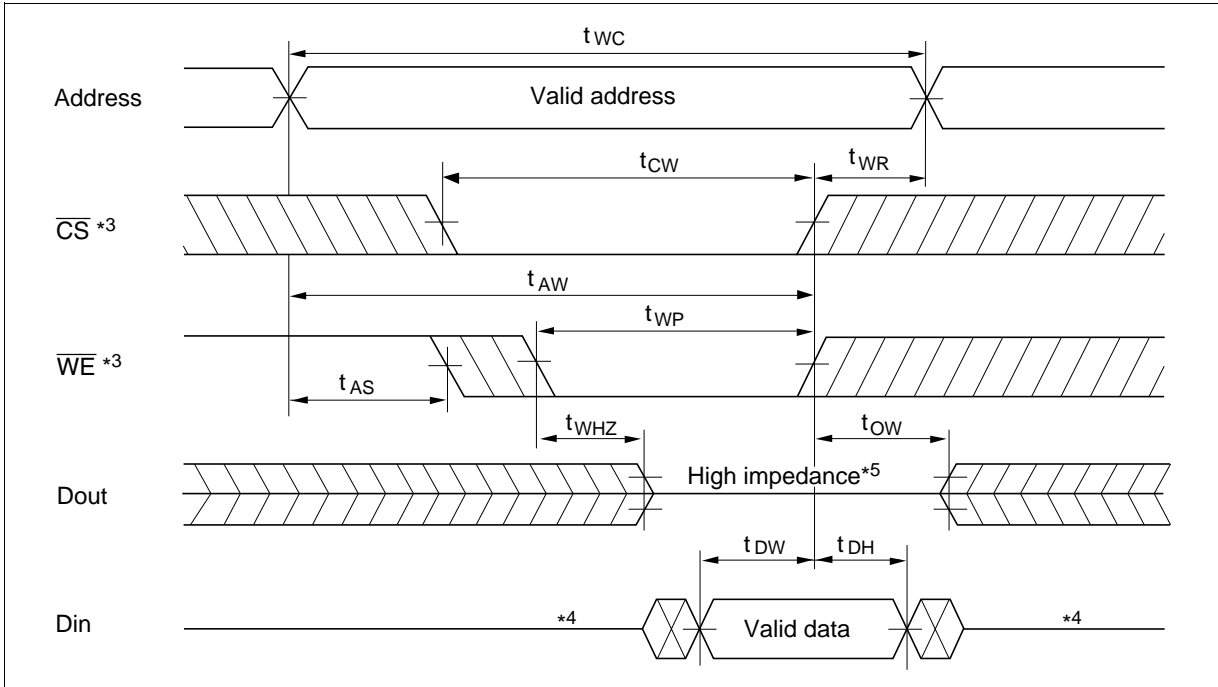


Write Timing Waveform (1) (\overline{WE} Controlled)



HM628127HB Series

Write Timing Waveform (2) (\overline{CS} Controlled)



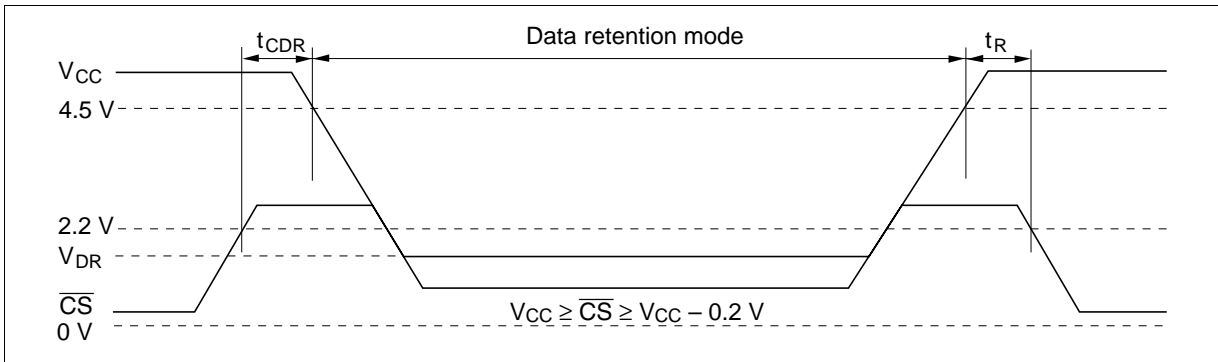
Low V_{CC} Data Retention Characteristics ($T_a = 0$ to 70°C)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2\text{ V}$ (1) $0\text{ V} \leq V_{in} \leq 0.2\text{ V}$ or (2) $V_{CC} \geq V_{in} \geq V_{CC} - 0.2\text{ V}$
Data retention current	I_{CCDR}	—	2	80	μA	$V_{CC} = 3\text{ V}$, $V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2\text{ V}$ (1) $0\text{ V} \leq V_{in} \leq 0.2\text{ V}$ or (2) $V_{CC} \geq V_{in} \geq V_{CC} - 0.2\text{ V}$
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	5	—	—	ms	

Note: 1. Typical values are at $V_{CC} = 3.0\text{ V}$, $T_a = 25^\circ\text{C}$, and not guaranteed.

Low V_{CC} Data Retention Timing Waveform

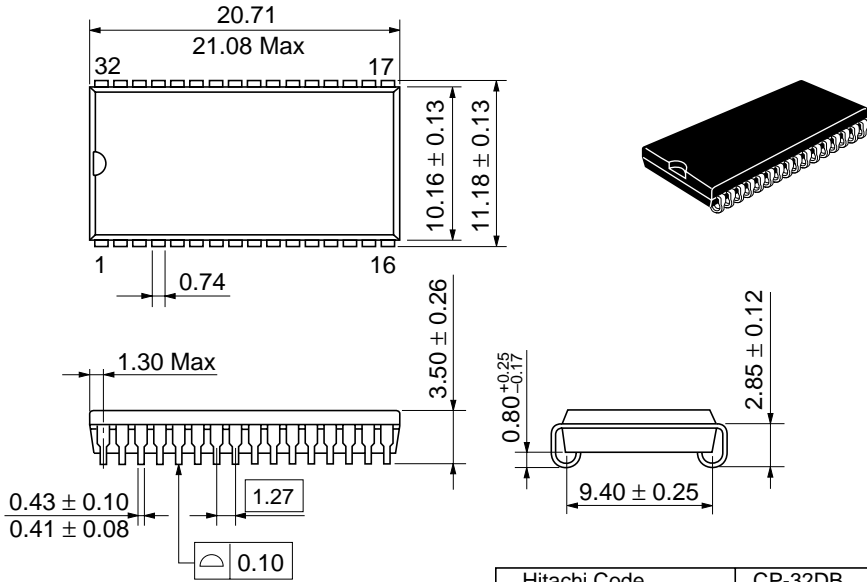


HM628127HB Series

Package Dimensions

HM628127HBJP/HBLJP Series (CP-32DB)

Unit: mm



Hitachi Code	CP-32DB
JEDEC Code	MO-061-AB
EIAJ Code	SC-638
Weight	1.2 g

When using this document, keep the following in mind:

1. This document may, wholly or partially, be subject to change without notice.
2. All rights are reserved: No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without Hitachi's permission.
3. Hitachi will not be held responsible for any damage to the user that may result from accidents or any other reasons during operation of the user's unit according to this document.
4. Circuitry and other examples described herein are meant merely to indicate the characteristics and performance of Hitachi's semiconductor products. Hitachi assumes no responsibility for any intellectual property claims or other problems that may result from applications based on the examples described herein.
5. No license is granted by implication or otherwise under any patents or other rights of any third party or Hitachi, Ltd.
6. **MEDICAL APPLICATIONS:** Hitachi's products are not authorized for use in **MEDICAL APPLICATIONS** without the written consent of the appropriate officer of Hitachi's sales company. Such use includes, but is not limited to, use in life support systems. Buyers of Hitachi's products are requested to notify the relevant Hitachi sales offices when planning to use the products in **MEDICAL APPLICATIONS**.

HITACHI

Hitachi, Ltd.

Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan
Tel: Tokyo (03) 3270-2111
Fax: (03) 3270-5109

For further information write to:

Hitachi America, Ltd.
Semiconductor & IC Div.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1835
U S A
Tel: 415-589-8300
Fax: 415-583-4207

Hitachi Europe GmbH
Electronic Components Group
Continental Europe
Dornacher Straße 3
D-85622 Feldkirchen
München
Tel: 089-9 91 80-0
Fax: 089-9 29 30 00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel: 0628-585000
Fax: 0628-778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 0104
Tel: 535-2100
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon
Hong Kong
Tel: 27359218
Fax: 27306071

HM628127HB Series

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Sep. 9, 1995	Initial issue	Y. Saitou	K. Yoshizaki
1.0	Nov. 15, 1995	Deletion of HM628127HB-25 series	Y. Saitou	K. Yoshizaki
2.0	Jun. 27 1996	Change of format Change of Block Diagram Function Table Addition of Mode parameter Recommended DC Operating Conditions Change of note 2. Addition of note 3. AC Characteristics Change order of notes Change of Timing Waveform Addition of Read timing waveform(2), (3) Low V_{CC} Data Retention Characteristics Change of Test conditions for I_{CCDR}	Y. Saitou	A. Ide
3.0	Nov. 19, 1996	Change of Package Dimensions		