

# IEEE1394 Link Layer Controller with DV Codec

The  $\mu$ PD72891 and 72893 support IEEE1394 bus control and AV/C commands via the on-chip CPU, as well as external control using either a serial or a parallel interface.

- All functions required for Digital AV 1394 interface are equipped in a single-chip
  - On chip 32-bit RISC CPU
  - Copy Protection circuit equipped (the  $\mu$ PD72891 only)
  - Full duplex MPEG/DV transmission supported
  - On-chip IEC61883 function
- Compliant to IEEE1394-1995 and IEEE1394a-2000
- Supports 400 Mbps, 200 Mbps, 100 Mbps speed
- 3.3 V/2.5 V power supply
- Package : 208-pin QFP

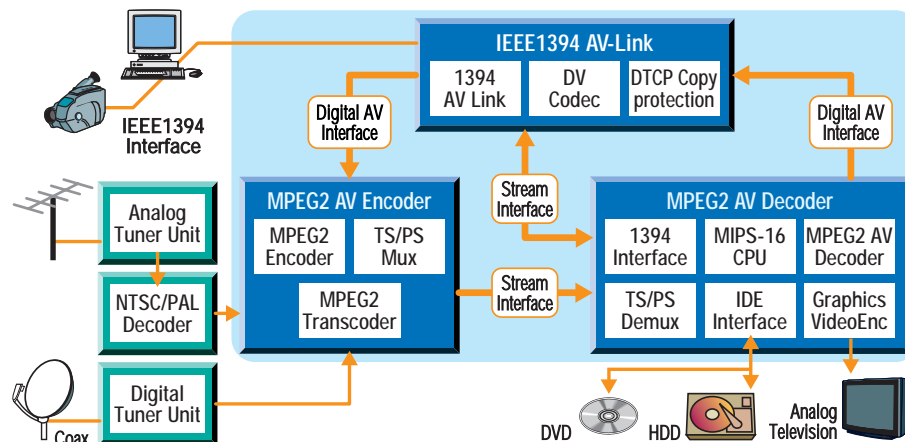
The diagram illustrates the system architecture of the TMS320C6410. Key components and their connections include:

- IEEE1394 Bus:** Connected to the system via a PHY and Link I/F.
- Link Core:** The central processing unit, featuring an Async I/F, CSR, and ISO Stream I/F.
- Link I/F:** Manages data flow between the Link Core and the CPU/SIO.
- Bus Controller:** Coordinates communication between the Link Core and the CPU/SIO.
- CPU (NB85E):** Contains 192 KB ROM and 60 KB RAM.
- SIO, Port, Timer...**: Serial I/O and control components.
- HOST I/F:** Interface for host communication.
- DV Decoder Encoder:** Processes digital video signals.
- 16M SDRAM:** System memory, connected via VCLKI/MCK44/MCK48 and VCLKO/MCKO.
- MPEG2 Decoder/Encoder:** Connected via TS I/F and PCM Serial I/F.
- System Controller:** Can select either the CPU I/F (68k / ISA) or the HOST I/F for communication.

- Application
  - Set-top Box
  - Digital VHS, DVD-RW, AV HDD
  - Digital Television
- Companion Chip
  - $\mu$ PD72852 : 2-port low power PHY compliant with IEEE1394a-2000

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## Device Solution for Digital AV



## URL

<http://www.ic.nec.co.jp/>

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