

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# TC74LCX16244AFT

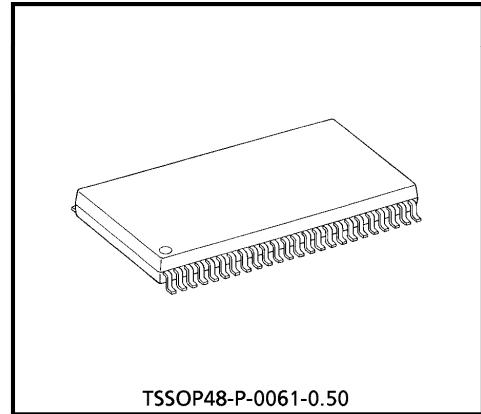
## LOW-VOLTAGE 16-BIT BUS BUFFER WITH 5V TOLERANT INPUTS AND OUTPUTS

The TC74LCX16244AFT is a high performance CMOS 16bit BUS BUFFER. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3V) V<sub>CC</sub> applications, but it could be used to interface to 5V supply environment for both inputs and outputs.

This device is non-inverting 3-state buffer having four active-low output enables. It can be used as four 4-bit buffers two 8-bit buffers or one 16-bit buffer. When the  $\overline{OE}$  input is high, the outputs are in a high impedance state. This device is designed to be used with 3-state memory address drivers, etc.

All inputs are equipped with protection circuits against static discharge.



TSSOP48-P-0061-0.50

Weight : 0.25 g (Typ.)

### FEATURES

- Low Voltage Operation :  $V_{CC} = 2.0 \sim 3.6V$
- High Speed Operation :  $t_{pd} = 5.2\text{ns}$  (max.) at  $V_{CC} = 3.0 \sim 3.6V$
- Output Current :  $|I_{OH}| / |I_{OL}| = 24\text{mA}$  (MIN) at  $V_{CC} = 3.0V$
- Latch-up Performance :  $\pm 500\text{mA}$
- Package : TSSOP  
(Thin Shrink Small Outline Package)
- Power Down Protection is provided on all inputs and outputs.

### PIN CONNECTION

1 $\overline{OE}$	1 O	48	2 $\overline{OE}$
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V <sub>CC</sub>	7	42	V <sub>CC</sub>
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
V <sub>CC</sub>	18	31	V <sub>CC</sub>
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
4OE	24	25	3OE

(TOP VIEW)

961001EBA2

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## TRUTH TABLE

INPUTS		OUTPUTS
$\bar{1OE}$	$1A1-1A4$	$1Y1-1Y4$
L	L	L
L	H	H
H	X	Z

INPUTS		OUTPUTS
$2OE$	$1A1-2A4$	$2Y1-2Y4$
L	L	L
L	H	H
H	X	Z

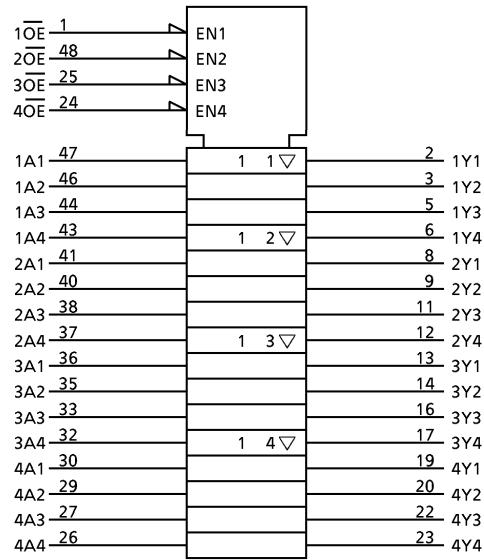
INPUTS		OUTPUTS
$3OE$	$3A1-3A4$	$3Y1-3Y4$
L	L	L
L	H	H
H	X	Z

INPUTS		OUTPUTS
$4OE$	$4A1-4A4$	$4Y1-4Y4$
L	L	L
L	H	H
H	X	Z

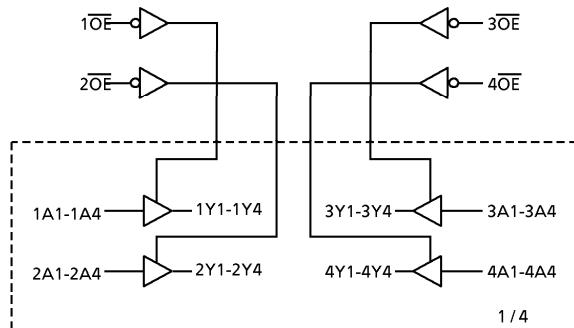
X : Don't Care

Z : High impedance

## IEC LOGIC SYMBOL



## SYSTEM DIAGRAM



- 961001EBA2'
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**MAXIMUM RATINGS**

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	$V_{CC}$	-0.5~7.0	V
Input Voltage	$V_{IN}$	-0.5~7.0	V
Output Voltage	$V_{OUT}$	-0.5~7.0 (Note 1)	V
		-0.5~ $V_{CC}$ +0.5 (Note 2)	
Input Diode Current	$I_{IK}$	-50	mA
Output Diode Current	$I_{OK}$	$\pm 50$ (Note 3)	mA
DC Output Current	$I_{OUT}$	$\pm 50$	mA
Power Dissipation	$P_D$	400	mW
DC $V_{CC}$ / Ground Current Per Supply Pin	$I_{CC} / I_{GND}$	$\pm 100$	mA
Storage Temperature	$T_{stg}$	-65~150	°C

(Note 1) Output in Off-State

(Note 2) High or Low State.  $I_{OUT}$  absolute maximum rating must be observed.(Note 3)  $V_{OUT} < GND$ ,  $V_{OUT} > V_{CC}$ **RECOMMENDED OPERATING RANGE**

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	$V_{CC}$	2.0~3.6	V
		1.5~3.6 (Note 4)	
Input Voltage	$V_{IN}$	0~5.5	V
Output Voltage	$V_{OUT}$	0~5.5 (Note 5)	V
		0~ $V_{CC}$ (Note 6)	
Output Current	$I_{OH} / I_{OL}$	$\pm 24$ (Note 7)	mA
		$\pm 12$ (Note 8)	
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise And Fall Time	$dt/dv$	0~10 (Note 9)	ns/V

(Note 4) Data Retention Only

(Note 5) Output in Off-State

(Note 6) High or Low State

(Note 7)  $V_{CC} = 3.0 \sim 3.6V$ (Note 8)  $V_{CC} = 2.7 \sim 3.0V$ (Note 9)  $V_{IN} = 0.8 \sim 2.0V$ ,  $V_{CC} = 3.0V$

## ELECTRICAL CHARACTERISTICS

DC characteristics ( $T_a = -40\sim85^\circ C$ )

PARAMETER		SYMBOL	TEST CONDITION		$V_{CC}$ (V)	MIN.	MAX.	UNIT	
Input Voltage	"H" Level	$V_{IH}$				2.7~3.6	2.0	—	V
	"L" Level	$V_{IL}$			2.7~3.6	—	0.8	V	
Output Voltage	"H" Level	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -100\mu A$	2.7~3.6	$V_{CC} - 0.2$	—	V	
				$I_{OH} = -12\mu A$	2.7	2.2	—		
				$I_{OH} = -18mA$	3.0	2.4	—		
				$I_{OH} = -24mA$	3.0	2.2	—		
Output Voltage	"L" Level	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 100\mu A$	2.7~3.6	—	0.2	V	
				$I_{OL} = 12mA$	2.7	—	0.4		
				$I_{OL} = 16mA$	3.0	—	0.4		
				$I_{OL} = 24mA$	3.0	—	0.55		
Input Leakage Current	$I_{IN}$	$V_{IN} = 0\sim 5.5V$		2.7~3.6	—	$\pm 5.0$	$\mu A$		
3-State Output Off-State Current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$V_{OUT} = 0\sim 5.5V$	2.7~3.6	—	$\pm 5.0$	$\mu A$		
Power Off Leakage Current	$I_{OFF}$	$V_{IN}/V_{OUT} = 5.5V$		0	—	10.0	$\mu A$		
Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND		2.7~3.6	—	20.0	$\mu A$		
		$V_{IN}/V_{OUT} = 3.6\sim 5.5V$		2.7~3.6	—	$\pm 20.0$			
Increase In $I_{CC}$ Per Input	$\Delta I_{CC}$	$V_{IH} = V_{CC} - 0.6V$		2.7~3.6	—	500	$\mu A$		

AC characteristics ( $T_a = -40\sim85^\circ C$ )

CHARACTERISTIC	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	MIN.	MAX.	UNIT
Propagation Delay Time	$t_{PLH}$	(Fig.1, 2)	2.7	—	6.2	ns
	$t_{PHL}$		$3.3 \pm 0.3$	1.5	5.2	
3-State Output Enable Time	$t_{PZL}$	(Fig.1, 3)	2.7	—	7.5	ns
	$t_{PZH}$		$3.3 \pm 0.3$	1.5	6.5	
3-State Output Disable Time	$t_{PLZ}$	(Fig.1, 3)	2.7	—	6.5	ns
	$t_{PHZ}$		$3.3 \pm 0.3$	1.5	5.5	
Output To Output Skew	$t_{osLH}$	(Note 10)	2.7	—	—	ns
	$t_{osHL}$		$3.3 \pm 0.3$	—	1.0	

(Note 10) Parameter guaranteed by design.

$$(t_{osLH} = |t_{PLHm} - t_{PLHn}|, t_{osHL} = |t_{PHLm} - t_{PHLn}|)$$

## Dynamic switching characteristics

 $(T_a = 25^\circ C, \text{ Input } t_r = t_f = 2.5\text{ns}, C_L = 50\text{pF}, R_L = 500\Omega)$ 

CHARACTERISTIC	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	TYP	UNIT
Quiet Output Maximum Dynamic $V_{OL}$	$V_{OLP}$	$V_{IH} = 3.3\text{V}, V_{IL} = 0\text{V}$	3.3	0.8	V
Quiet Output Minimum Dynamic $V_{OL}$	$ V_{OLV} $	$V_{IH} = 3.3\text{V}, V_{IL} = 0\text{V}$	3.3	0.8	V

Capacitive characteristics ( $T_a = 25^\circ C$ )

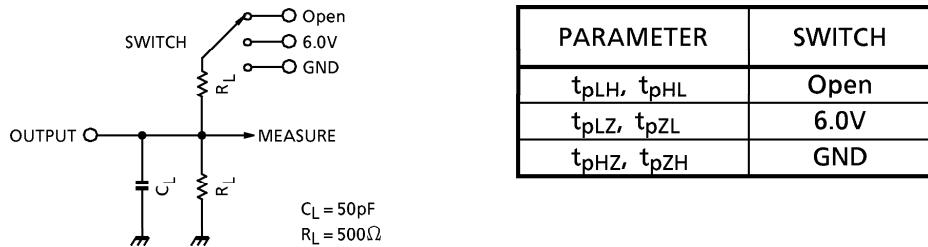
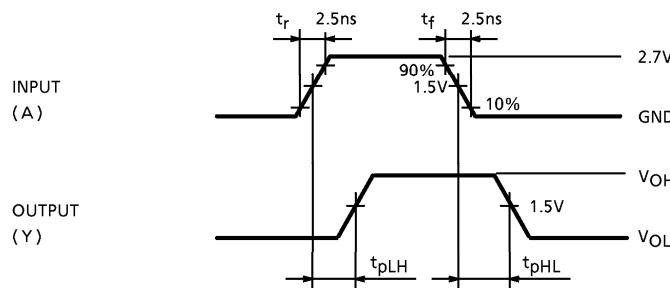
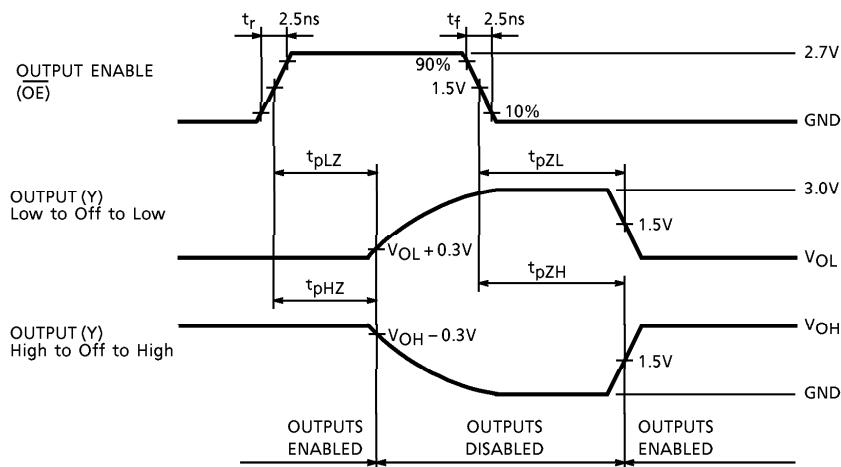
CHARACTERISTIC	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	TYP	UNIT	
Input Capacitance	$C_{IN}$	—	3.3	7	pF	
	$C_{OUT}$		3.3	8	pF	
Power Dissipation Capacitance	$C_{PD}$	$f_{IN} = 10\text{MHz}$	(Note 11)	3.3	25	pF

(Note 11)  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 16. \text{ (Per bit)}$$

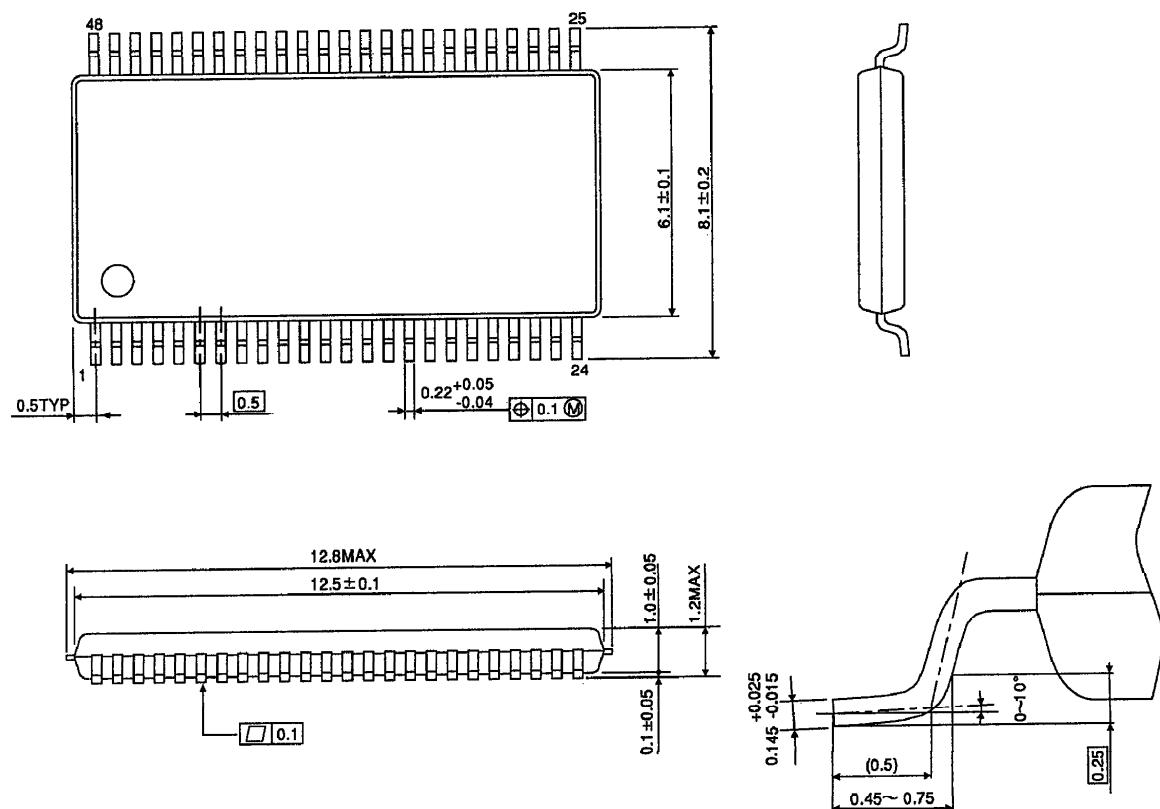
Fig.1 Test circuit

**AC WAVEFORM**Fig.2  $t_{pLH}, t_{pHL}$ Fig.3  $t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}$ 

## OUTLINE DRAWING

TSSOP48-P-0061-0.50

Unit : mm



Weight : 0.25g (Typ.)