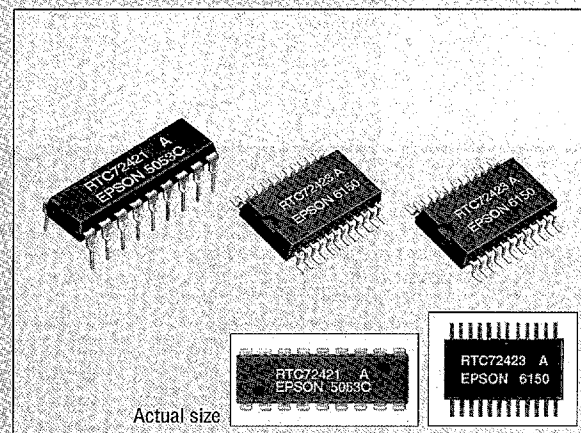


4-bit REAL TIME CLOCK MODULE

RTC-72421/72423

- Builtin crystal unit allows adjustment-free efficient operation.
- ALE input terminal available for 8048, 8051, and 8085 series.
- 12/24H clock switchover function and automatic leap year setting.
- Interrupt masking.
- 30 second adjustment function.
- Low current consumption and features a backup function.



Actual size

■ Specifications (characteristics)

■ Absolute Max. rating

Item	Symbol	Condition	Specifications	Unit
Power source voltage	V_{DD}	$T_a=25^\circ\text{C}$	-0.3 to 7.0	V
Input and output voltage	V_{IO}	$T_a=25^\circ\text{C}$	GND -0.3 to $V_{DD}+0.3$	V
Storage temperature	T_{STG}	RTC-72421	-55 to +85	$^\circ\text{C}$
		RTC-72423	-55 to +125	
Soldering condition	T_{SOL}	RTC-72421	Under 260°C within 10 sec. (lead part) (package should be less than 150°C)	
		RTC-72423	Twice at under 260°C within 10 sec. or under 230°C within 3 min.	

■ Operating range

Item	Symbol	Condition	Specifications	Unit
Operating voltage	V_{DD}		4.5 to 5.5	V
Operating temperature	T_{OPR}	RTC-72421	-10 to 70	$^\circ\text{C}$
		RTC-72423	-40 to 85	
Data holding voltage	V_{DH}		2.0 to 5.5	V
CSI data holding time	t_{ODR}	Refer to the data holding timing	2.0 min.	μs
Operation restoring time	t_R			

■ Frequency characteristics and current consumption characteristics

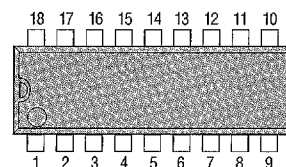
Item	Symbol	Condition	Specifications	Unit
Frequency tolerance	$\Delta f/f_0$	$T_a=25^\circ\text{C}$	72421 A ± 10	ppm
			72421 B ± 50	
		$V_{DD}=5V$	72423 A ± 20	
			72423 ± 50	
Frequency temperature characteristics		-10 to $+70^\circ\text{C}$ (25°C reference temperature)	$+10/-120$	
Aging	f_a	$V_{DD}=5V$, $T_a=25^\circ\text{C}$, first year	± 5 max.	ppm/Y
Shock resistance	S.R.	Three drops on a hard board from 75 cm or 3000G x 0.3ms x 1/2 sine wave x 3 directions	± 10 max.	ppm
Current consumption	I_{DD1}	$CS_1=0V$	$V_{DD}=5V$ 10 max.	μA
	I_{DD2}	Exclude input/output current	$V_{DD}=2V$ 5 max.	

■ Electrical characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Terminal
"H" input voltage (1)	V_{IH1}	$V_I=V_{DD}/0V$	2.2		—	V	All inputs other than CS_1
"L" input voltage (1)	V_{IL1}		—		0.8	V	
Input leak current (1)	I_{LK1}		—		± 1	μA	
Input leak current (2)	I_{LK2}		—		± 10	μA	
"L" output voltage (1)	V_{OL1}	$I_{OL}=2.5\text{mA}$	—	—	0.4	V	Do to D_3
"H" output voltage	V_{OH}	$I_{OH}=-400\mu\text{A}$	2.4	—	—	V	
"L" output voltage (2)	V_{OL2}	$I_{OL}=2.5\text{mA}$	—	—	0.4	V	STD.P
Off leak current	I_{OFFLK}	$V_I=V_{DD}/0V$	—	—	10	μA	
Input capacity	C_1	Input frequency 1 MHz	—	10	—	pF	Input other than Do to D_3
			—	20	—	pF	Do to D_3
"H" input voltage (2)	V_{IH2}	$V_{DD}=2$ to $5.5V$	$4/5 V_{DD}$	—	—	V	
"L" input voltage (2)	V_{IL2}		—	—	$1/5 V_{DD}$	V	CS_1

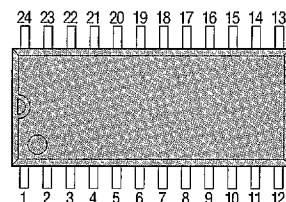
■ Terminal connection

● RTC-72421



No.	72421	No.	72423
1	STD. P	1	STD. P
2	CS_1	2	CS_1
3	ALE	3	NC
4	A_0	4	ALE
5	A_1	5	A_0
6	A_2	6	NC
7	A_3	7	A_1
8	RD	8	NC
9	GND	9	A_2
10	WR	10	A_3
11	D_2	11	RD
12	D_3	12	GND
13	D_1	13	WR
14	D_0	14	D_2
15	CS_1	15	D_3
16	(V_{DD})	16	D_1
17	(V_{DD})	17	NC
18	V_{DD}	18	NC
		19	D_0
		20	CS_1
		21	NC
		22	(V_{DD})
		23	(V_{DD})
		24	V_{DD}

● RTC-72423

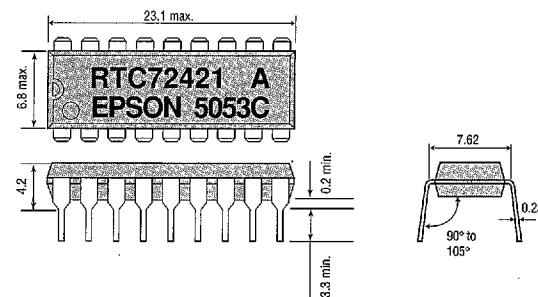


- (V_{DD}) and V_{DD} are to have the same level of voltage. Do not connect it to any external terminals.
- NC is not connected internally.

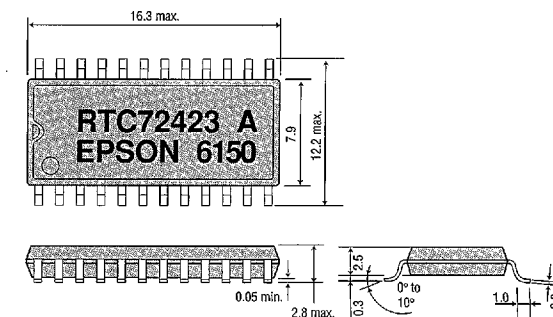
■ External dimensions

(Unit: mm)

● RTC-72421



● RTC-72423



■ Register table

Address	A ₃	A ₂	A ₁	A ₀	Register	Data				Count Value	Remarks
						D ₃	D ₂	D ₁	D ₀		
0	0	0	0	0	S ₁	S ₈	S ₄	S ₂	S ₁	0 to 9	1-second digit register
1	0	0	0	1	S ₁₀	*	S ₄₀	S ₂₀	S ₁₀	0 to 5	10-second digit register
2	0	0	1	0	M ₁₁	m ₁₆	m ₄	m ₂	m ₁	0 to 9	1-minute digit register
3	0	0	1	1	M ₁₀	*	m ₄₀	m ₂₀	m ₁₀	0 to 5	10-minute digit register
4	0	1	0	0	H ₁	h ₈	h ₄	h ₂	h ₁	0 to 9	1-hour digit register
5	0	1	0	1	H ₁₀	*	PM/AM	h ₂₀	h ₁₀	0 to 2 or 0 to 1	PM/AM, 10-hours digit register
6	0	1	1	0	D ₁	d ₈	d ₄	d ₂	d ₁	0 to 9	1-day digit register
7	0	1	1	1	D ₁₀	*	*	d ₂₀	d ₁₀	0 to 3	10-day digit register
8	1	0	0	0	M ₀₁	m ₀₈	m ₀₄	m ₀₂	m ₀₁	0 to 9	1-month digit register
9	1	0	0	1	M ₀₀	*	*	*	m ₀₁₀	0 to 1	10-month digit register
A	1	0	1	0	Y ₁	y ₈	y ₄	y ₂	y ₁	0 to 9	1-year digit register
B	1	0	1	1	Y ₁₀	y ₈₀	y ₄₀	y ₂₀	y ₁₀	0 to 9	10-year digit register
C	1	1	0	0	W	*	w ₄	w ₂	w ₁	0 to 6	Week register
D	1	1	0	1	RegD	30 sec. ADJ	IRQ FLAG	BUSY	HOLD		Control Register D
E	1	1	1	0	RegE	t ₁	t ₀	ITRPT/STND	MASK	—	Control Register E
F	1	1	1	1	RegF	TEST	24/12	STOP	REST		Control Register F

0="L" level, 1="H" level, REST = RESET ITRPT/STND=INTERRUPT/STANDARD

- 1) Bit * does not exist.
- 2) Please mask AM/PM bit with 10's of hours operations.
- 3) Busy is read only. IRQ can only. IRQ can only be set low ("0").
- 4)

Data Bit	PM/AM	ITRPT/STND	24/12
1	PM	ITRPT	24
0	AM	STND	12
- 5) TEST bit should be "0".

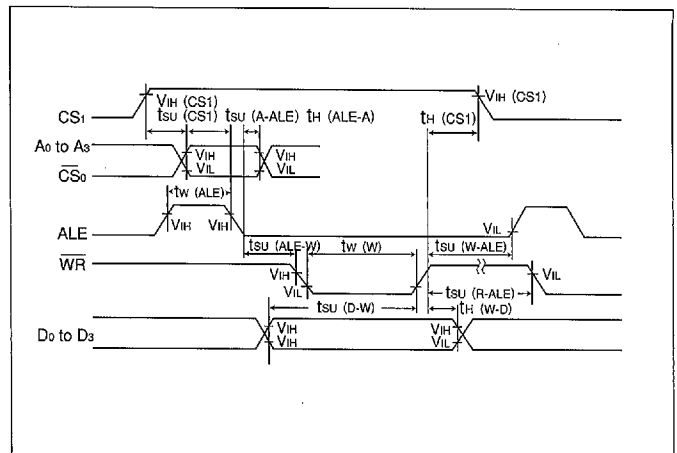
■ Switching characteristics (with ALE)

(Please connect ALE to V_{DD} if the microprocessor does not have an ALE output.)

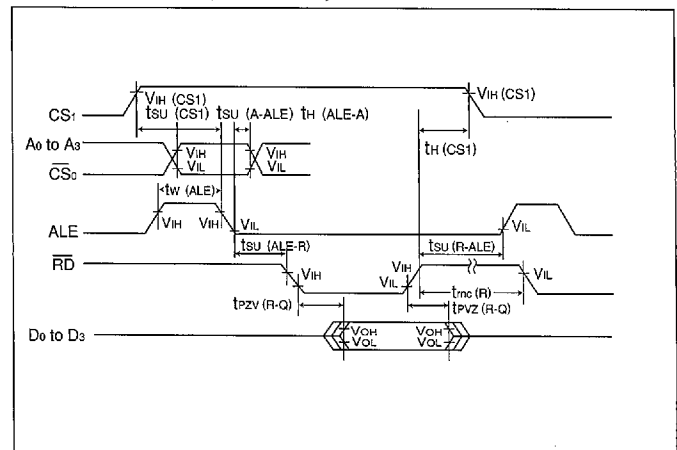
Item	Symbol	Condition	Min	Max	Unit
CS ₁ setup time	t _{su} (CS ₁)		1000		
Address setup time before ALE	t _{su} (A-ALE)		50		
Address hold time after ALE	t _h (ALE-A)		50		
ALE pulse width	t _w (ALE)		80		
ALE setup time before WRITE	t _{su} (ALE-W)		0		—
ALE setup time before READ	t _{su} (ALE-R)		0		
ALE setup time after WRITE	t _{su} (W-ALE)		50		ns
ALE setup time after READ	t _{su} (R-ALE)		50		
WRITE pulse width	t _w (W)		120		
DATA delay time after READ	t _{pZV} (R-Q)	C _L =150pF	—	120	
DATA Hold time after READ	t _{pVZ} (R-Q)		0	70	
DATA setup time before WRITE	t _{su} (D-W)		80		
DATA hold time after WRITE	t _h (W-D)		10		—
CS ₁ hold time	t _h (CS ₁)		1000		
READ/WRITE recovery time	t _{rec} (R/W)		200		

(V_{DD} = 5V ± 0.5V)

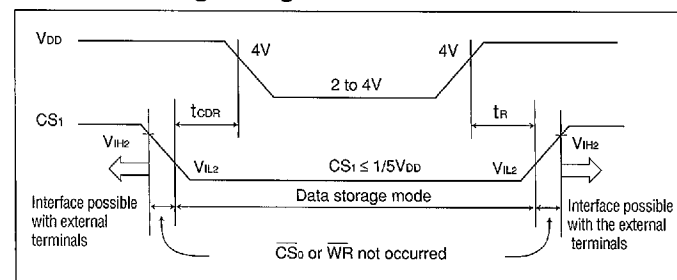
■ Write mode (with ALE)



■ Read mode (with ALE)



■ Data holding timing



■ Block diagram

