

SONY

CXP87452/87460

CMOS 8-bit Single Chip Microcomputer

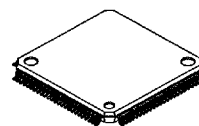
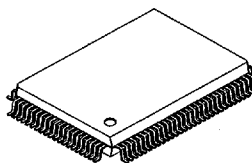
Description

The CXP87452/87460 is a CMOS 8-bit microcomputer which consists of A/D converter, serial interface (2ch independently), timer/counter, time base timer, vector interruption, high precision timing pattern generation circuit (PPG 2ch independently, RTG 2ch independently), PWM generator, general purpose prescaler, PWM for tuner, VCR vertical sync separation circuit and the measuring circuit which measure signals of capstan FG and drum FG/PG and other servo systems, as well as basic configurations like 8-bit CPU, ROM, RAM and I/O port. They are integrated into a single chip.

Also CXP87452/87460 provides power on reset function, sleep/stop function which enables to lower power consumption.

100 pin QFP (Plastic)

100 pin LQFP (Plastic)



Structure

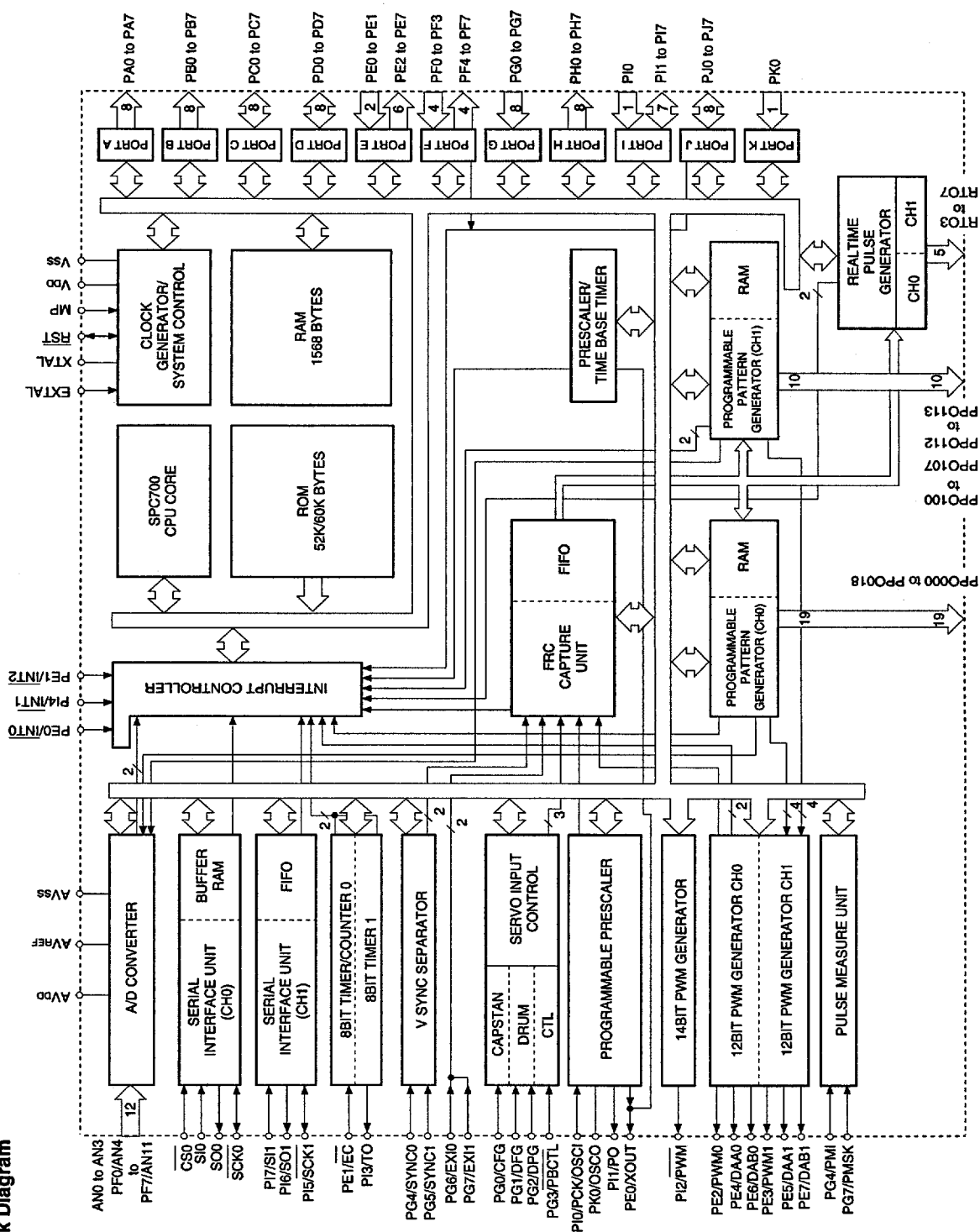
Silicon gate CMOS IC

Features

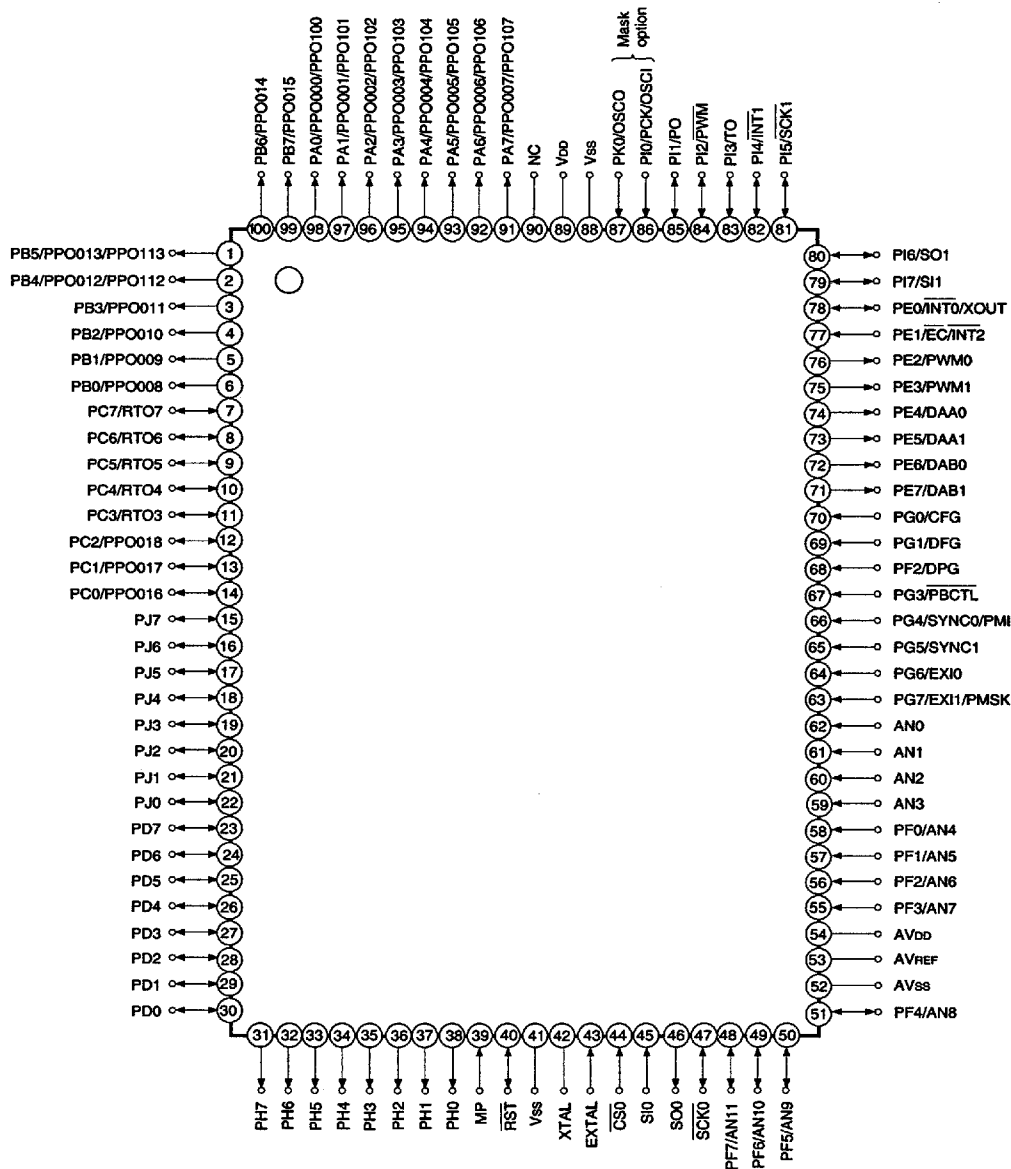
- A wide instruction set (213 instructions) which cover various types of data
 - 16-bit arithmetic instruction/multiplication and division instructions/boolean bit operation instruction
- Minimum instruction cycle
 - During operation 333ns/12MHz (3.0 to 5.5V)
 - During operation 250ns/16MHz (4.5 to 5.5V)
- Incorporated ROM capacity
 - 52K bytes (CXP87452)
 - 60K bytes (CXP87460)
- Incorporated RAM capacity
 - 1568 bytes
- Peripheral functions
 - A/D converter
 - 8-bit, 12-channel, successive approximation system (Conversion time: 20μs/16MHz)
 - Serial interface
 - Incorporated buffer RAM (1 to 32 bytes auto transfer) 1-channel
 - Incorporated 8-bit and 8-stage FIFO (1 to 8 bytes auto transfer) 1-channel
 - Timer
 - 8-bit timer, 8-bit timer/counter, 19-bit time base timer
 - High precision timing pattern generator
 - PPG 19 pins 32-stage programmable
 - PPG 10 pins 21-stage programmable
 - RTG 5 pins 2-channel
 - PWM/DA gate output
 - PWM 12-bit, 2-channel (Repetitive frequency 62.5kHz/16MHz)
 - DA gate pulse 12-bit, 4-channel
 - Capstan FG, Drum FG/PG, CTL input
 - Servo input control
 - Incorporated 26-bit and 8-stage FIFO
 - VSYNC separator
 - 14-bit, 1-channel
 - FRC capture unit
 - 10-bit (System clock asynchronous)
 - PWM output
 - General purpose prescaler
 - Pulse cycle measurement circuit
- Interruption
 - 18 factors, 14 vectors, multi-interruption possible
- Standby mode
 - SLEEP/STOP
- Package
 - 100-pin plastic QFP/LQFP
- Piggyback/evaluation chip
 - CXP87400 100-pin ceramic QFP/LQFP

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Block Diagram

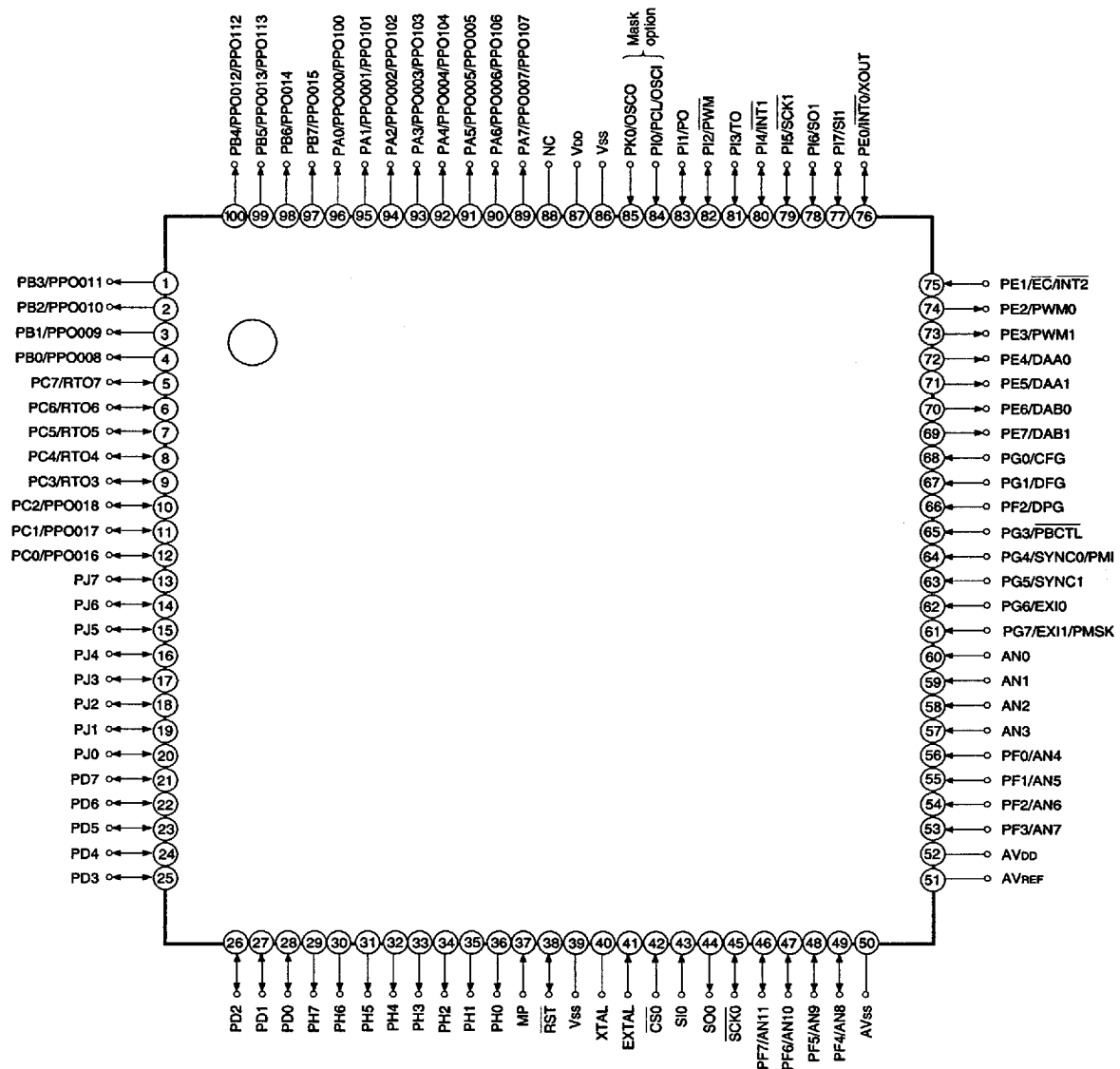


Pin Configuration 1 (Top View) 100 pin QFP Package



- Note)**
1. NC (Pin 90) is always connected to VDD.
 2. Vss (Pins 41 and 88) are both connected to GND.

Pin Configuration 2 (Top View) 100 pin LQFP Package



- Note)**
1. NC (Pin 88) is always connected to VDD.
 2. Vss (Pins 39 and 86) are both connected to GND.

Pin Description

Symbol	I/O	Description		
PA0/PPO000 /PPO100 to PA7/PPO007 /PPO107	Output/ Real time output	(Port A) 8-bit output port. Data is gated with PPO0 and PPO1 contents by OR-gate and they are output. (8 pins)	Programmable pattern generator (PPG0, PPG1) output. Functions as high precision real time pulse output port. (PPG0 19 pins) (PPG1 10 pins)	
PB0/PPO008 to PB7/PPO015	Output/ Real time output	(Port B) 8-bit output port. Data is gated with PPO0 and PPO1 contents by OR-gate and they are output. (8 pins)		
PC0/PPO016 to PC2/PPO018	I/O/ Real time output	(Port C) 8-bit I/O port. Enables to specify I/O by bit unit. Data is gated with PPO or RTO contents by OR-gate and they are output. (8 pins)		
PC3/RTO3 to PC7/RTO7	I/O/ Real time output		Real time pulse generator (RTG) output. Functions as high precision real time pulse output port. (5 pins)	
PD0 to PD7	I/O	(Port D) 8-bit I/O port. Enable to specify I/O by 4-bit unit. Enables to drive 12mA sinc current. (During 5V ± 0.5V operation) (8 pins)		
PE0/ $\overline{\text{INT0}}$ /XOUT	Input/input/output	(Port E) 8-bit port. Lower 2 bits are input port and upper 6 bits are output port. (8 pins)	Input pin to request external interruption. Active when falling edge.	
PE1/ $\overline{\text{EC}}$ / $\overline{\text{INT2}}$	Input/input/input		1/2 dividing clock output of XTAL or OSC0.	
PE2/PWM0	Output/output		External event input pin for timer/counter.	Input pin to request external interruption. Active when falling edge.
PE3/PWM1	Output/output		PWM output pins. (2 pins)	
PE4/DAA0	Output/output		DA gate pulse output pins. (4 pins)	
PE5/DAA1	Output/output			
PE6/DAB0	Output/output			
PE7/DAB1	Output/output			
AN0 to AN3	Input	Analog input pins to A/D converter. (12 pins)		
PF0/AN4 to PF3/AN7	Input/input	(Port F) Lower 4 bits are input port and upper 4 bits are output port. Lower 4 bits also serve as standby release input pin. (8 pins)		
PF4/AN8 to PF7/AN11	Output/input			
$\overline{\text{SCK0}}$	I/O	Serial clock (CH0) I/O pin.		
SO0	Ouput	Serial data (CH0) output pin.		
SI0	Input	Serial data (CH0) input pin.		
$\overline{\text{CS0}}$	Input	Serial chip select (CH0) input pin.		

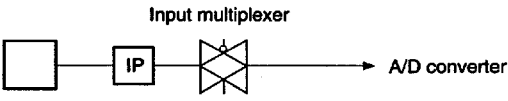
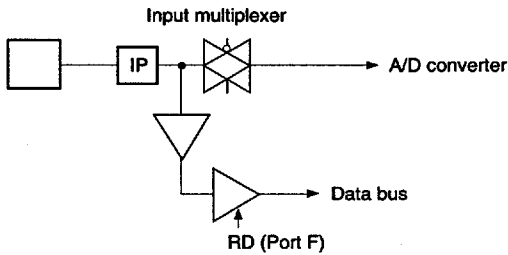
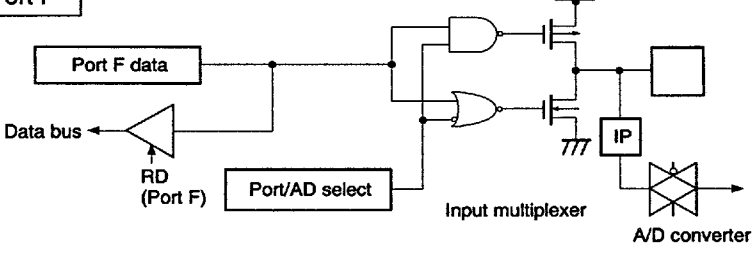
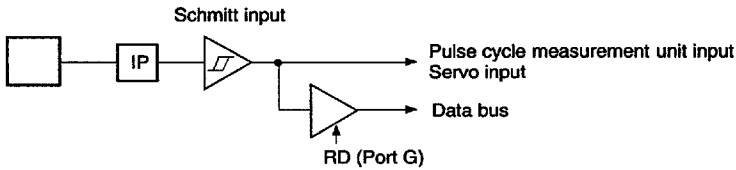
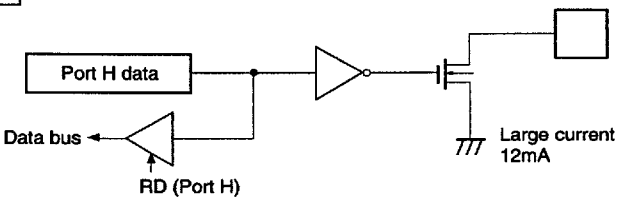
Symbol	I/O	Description		
PG0/CFG	Input/input	(Port G) 8-bit input port. (8 pins)	Capstan FG input pin.	
PG1/DFG	Input/input		Drum FG input pin.	
PG2/DPG	Input/input		Drum PG input pin.	
PG3/PBCTL	Input/input		Playback CTL pulse input pin.	
PG4/SYNC0 /PMI	Input/input/input		Composite sync signal input pin.	Measuring pulse signal input pin of pulse cycle measuring unit.
PG5/SYNC1	Input/input			
PG6/EXI0	Input/input		External input pin to FRC capture unit.	
PG7/EXI1/ PMSK	Input/input/input			Measuring enable signal input pin of pulse cycle measuring unit.
PH0 to PH7	Output	(Port H) 8-bit output port; large current, N-ch open drain output. (8 pins)		
PI0/PCK /OSCI	Input/input/input	(Port I) Lower 1 bit is input port (mask option) and upper 7 bits are I/O port. I/O port can be specified by bit unit. (8 pins)	External clock input pin of general purpose prescaler.	Connecting pin of crystal oscillation circuit for general purpose prescaler. (Mask option)
PI1/PO	I/O/output		General purpose prescaler output pin.	
PI2/PWM	I/O/output		14-bit PWM output pin.	
PI3/TO	I/O/output		Timer/counter, output pin. (duty = 50%)	
PI4/INT1	I/O/input		Input pin to request external interruption. Active when falling edge.	
PI5/SCK1	I/O/I/O		Serial clock (CH1) I/O pin.	
PI6/SO1	I/O/output		Serial data (CH1) output pin.	
PI7/SI1	I/O/input		Serial data (CH1) input pin.	
PJ0 to PJ7	I/O	(Port J) 8-bit I/O port. Function as standby release input can be specified by bit unit. I/O can be specified by bit unit.		

Symbol	I/O	Description	
PK0/OSCO	Input/output	Input port. (Mask option)	Connecting pin of crystal oscillation circuit for general purpose prescaler. (Mask option)
EXTAL	Input	Connecting pin of crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and input opposite phase clock to XTAL pin.	
XTAL	Output		
$\overline{\text{RST}}$	I/O	System reset pin of active "L" level. $\overline{\text{RST}}$ pin is I/O pin, which output "L" level by incorporated power on reset function when power on. (Mask option)	
MP	Input	Microprocessor mode input pin. Always connect to GND.	
AVDD		Positive power supply pin of A/D converter.	
AVREF	Input	Reference voltage input pin of A/D converter.	
AVSS		GND pin of A/D converter.	
VDD		Positive power supply pin.	
VSS		GND pin. Connect both Vss pins to GND.	

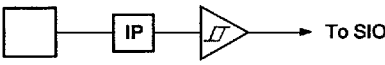
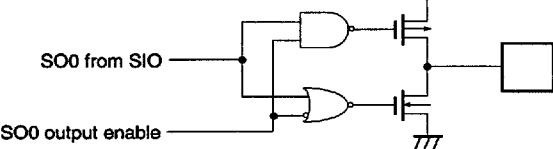
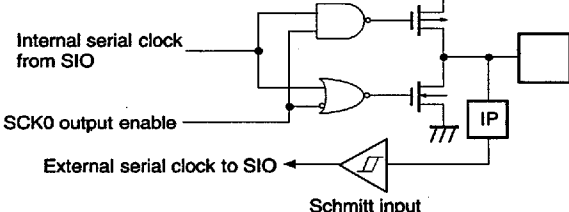
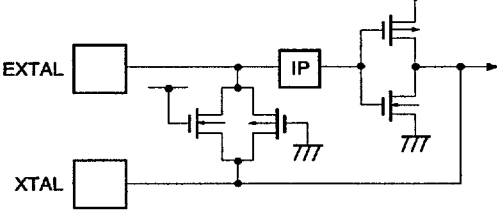
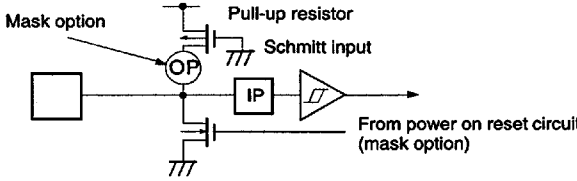
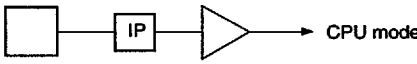
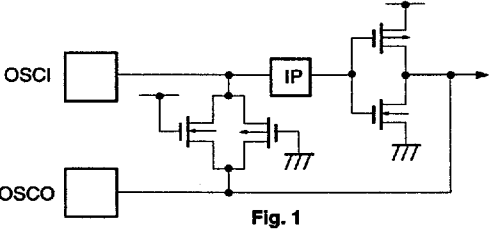
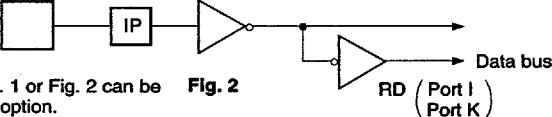
Input/Output Circuit Format for Pins

Pin	Circuit format	When reset
PA0/PPO000 /PPO100 to PA7/PPO007 /PPO107 PB4/PPO012 /PPO112 to PB5/PPO013 /PPO113 10 pins	Port A Port B PPO0 data PPO1 data Port A or Port B Data bus RD Output becomes active from high impedance by data writing to port register.	Hi-Z
PB0/PPO008 to PB3/PPO011 PB6/PPO014 to PB7/PPO015 6 pins	Port B PPO0 data Port A or Port B Data bus RD Output becomes active from high impedance by data writing to port register.	Hi-Z
PC0/PPO016 to PC2/PPO018 PC3/RTO3 to PC7/RTO7 8 pins	Port C PPO, RTO data Port C data Port C direction Data bus RD (Port C) (Every bit) Input protection circuit IP	Hi-Z
PD0 to PD7 8 pins	Port D Port D data Port D direction Data bus RD (Port D) (Every 4 bits) (PD0 to 3 PD4 to 7) Large current 12mA IP	Hi-Z

Pin	Circuit format	When reset
PE1/ $\overline{\text{EC}}/\overline{\text{INT2}}$ 1 pin	Port E	Hi-Z
PE0/ $\overline{\text{INT0}}$ / XOUT 1 pin	Port E	Hi-Z
PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1 4 pins	Port E	Hi-Z
PE6/DAB0 PE7/DAB1 2 pins	Port E	H level

Pin	Circuit format	When reset
AN0 to AN3 4 pins		Hi-Z
PF0/AN4 to PF3/AN7 4 pins	Port F 	Hi-Z
PF4/AN8 to PF7/AN11 4 pins	Port F 	Hi-Z
PG0/CFG PG1/DFG PG2/DPG PG3/PBCTL PG4/SYNC0/PMI PG5/SYNC1 PG6/EXI0 PG7/EXI1/PMSK 8 pins	Port G  Note) For PG4/SYNC0, PG5/SYNC1, CMOS schmitt input and TTL schmitt input can be selected with the mask option.	Hi-Z
PH0 to PH7 8 pins	Port H 	Hi-Z

Pin	Circuit format	When reset
PI1/PO PI2/PWM PI3/TO 3 pins	Port I Port I function select (PI1: From general purpose prescaler PI2: From 14-bit PWM PI3: From timer/counter) Port I data Port I direction Data bus RD (Port I) IP	Hi-Z
PI4/INT1 PI7/SI1 2 pins	Port I Port I data Port I direction Data bus RD (Port I) IP PI4: To interruption circuit PI7: To serial CH1 Schmitt input	Hi-Z
PI5/SCK1 PI6/SO1 2 pins	Port I Port I function select From serial CH1 Port I data Port I direction Data bus RD (Port I) IP Note) (PI5 is schmitt input PI6 is inverter input) To serial CH1	Hi-Z
PJ0 to PJ7 8 pins	Port J Port J data Port J direction Data bus RD (Port J) IP Edge detection Standby release	Hi-Z

Pin	Circuit format	When reset
$\overline{\text{CS0}}$ SIO 2 pins	Schmitt input 	Hi-Z
SO0 1 pin		Hi-Z
$\overline{\text{SCK0}}$ 1 pin		Hi-Z
EXTAL XTAL 2 pins	 • Shows the circuit composition during oscillation. • Feedback resistor is removed during stop.	Oscillation
$\overline{\text{RST}}$ 1 pin	 From power on reset circuit (mask option)	L level
MP 1 pin		Hi-Z
Port I Port K PIO/PCK/OSCI PK0/OSCO 2 pins	 Fig. 1  Fig. 2 Note) Circuit format of Fig. 1 or Fig. 2 can be selected with mask option.	Oscillation Hi-Z

Absolute Maximum Ratings

(Vss = 0V)

Item	Symbol	Rating	Unit	Remarks
Power supply voltage	V _{DD}	−0.3 to +7.0	V	
	AV _{DD}	AV _{SS} to +7.0* ¹	V	
	AV _{SS}	−0.3 to +0.3	V	
Input voltage	V _{IN}	−0.3 to +7.0* ²	V	
Output voltage	V _{OUT}	−0.3 to +7.0* ²	V	
High level output current	I _{OH}	−5	mA	
High level total output current	ΣI _{OH}	−50	mA	Total of output pins
Low level output current	I _{OL}	15	mA	Other than large current output pins: per pin
	I _{OLC}	20	mA	Large current output pin* ³ : per pin
Low level total output current	ΣI _{OL}	130	mA	Total of output pins
Operating temperature	T _{opr}	−20 to +75	°C	
Storage temperature	T _{stg}	−55 to +150	°C	
Allowable power dissipation	P _D	600	mW	QFP
		380		LQFP

*¹ AV_{DD} and V_{DD} should be set to a same voltage.

*² V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V. ($\overline{\text{CS0}}$, $\overline{\text{SIO}}$, PG and PH excluded.)

*³ The large current operation transistors are the N-CH transistors of the PD and PH ports.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Power supply voltage	V _{DD}	3.0	5.5	V	Guaranteed range during high speed mode (1/2 dividing clock) operation
		2.7	5.5	V	Guaranteed range during low speed mode (1/16 dividing clock) operation
		2.5	5.5	V	Guaranteed data hold operation range during STOP
Analog power supply	AV _{DD}	3.0	5.5	V	*1
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*2
	V _{IHS}	0.8V _{DD}	V _{DD}	V	CMOS schmitt input*3 and PE0/INT0 pins
			5.5	V	CMOS schmitt input*4
	V _{IHTS}	2.2	5.5	V	TTL schmitt input*5, *8
	V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL pin*6, *8
		V _{DD} - 0.2	V _{DD} + 0.2	V	EXTAL pin*6, *7
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	*2, *8
			0.2V _{DD}	V	*2, *7
	V _{ILS}	0	0.2V _{DD}	V	CMOS schmitt input*3, *4 and PE0/INT0 pins
	V _{ILTS}	0	0.8	V	TTL schmitt input*5, *8
	V _{ILEX}	-0.3	0.4	V	EXTAL pin*6, *8
		-0.3	0.2	V	EXTAL pin*6, *7
Operating temperature	Topr	-20	+75	°C	

*1 AV_{DD} and V_{DD} should be set to a same voltage.

*2 Normal input port (each pin of PC, PD, PF0 to PF3, PI PJ, and PK), MP pin.

*3 Each pin of SCK0, RST, PE1/EC/INT2, PI1/PO, PI4/INT1, PI5/SCK1 and PI7/SI1.

*4 Each pin of CS0, SI0, and PG (for PG and PG5, when CMOS schmitt input is selected.)

*5 Each pin of PG4 and PG5 (When TTL schmitt input is selected with mask option)

*6 It specifies only when the external clock is input.

*7 In case of 3.0 to 3.6V supply voltage (V_{DD}).

*8 In case of 4.5 to 5.5V supply voltage (V_{DD}).

Electrical Characteristics

DC Characteristics

Supply voltage (V_{DD}) 4.5 to 5.5V(T_a = -20 to +75°C, V_{SS} = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V _{OH}	PA to PE, PF4 to PF7, PH (V _{OL} only)	V _{DD} = 4.5V, I _{OH} = -0.5mA	4.0			V
			V _{DD} = 4.5V, I _{OH} = -1.2mA	3.5			V
Low level output voltage	V _{OL}	PI1 to PI7, PJ, SO, SCK, RST*1 (V _{OL} only)	V _{DD} = 4.5V, I _{OL} = 1.8mA			0.4	V
			V _{DD} = 4.5V, I _{OL} = 3.6mA			0.6	V
		PD, PH	V _{DD} = 4.5V, I _{OL} = 12.0mA			1.5	V
Input current	I _{IHE}	EXTAL	V _{DD} = 5.5V, V _{IH} = 5.5V	0.5		40	μA
	I _{IIE}		V _{DD} = 5.5V, V _{IL} = 0.4V	-0.5		-40	μA
	I _{ILR}	RST*2	V _{DD} = 5.5V, V _{IL} = 0.4V	-1.5		-400	μA
I/O leakage current	I _{Iz}	PA to PK, MP, AN0 to AN3, CS, SI, SO, SCK, RST*2	V _{DD} =5.5V, V _I = 0, 5.5V			±10	μA
Supply current*3	I _{DD1}	V _{DD}	Crystal oscillation (C ₁ = C ₂ = 15pF) of 16MHz		31	50	mA
	V _{DD} = 5V ± 0.5V*4						
	SLEEP mode			2.0	8.0	mA	
			V _{DD} = 5V ± 0.5V				
	I _{DDs3}		STOP mode			10	μA
		V _{DD} = 5.5V					
Input capacity	C _{IN}	Other than V _{DD} , V _{SS} , AV _{DD} , and AV _{SS} pins	Clock 1MHz 0V other than the measured pins		10	20	pF

*1 RST pin specifies only when the power on reset circuit has been selected with mask option.

*2 RST pin specifies the input current when the pull-up resistor is selected, and specifies leakage current when non-resistance is selected.

*3 When entire output pins are open.

*4 When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FEh) to "00" and operating in high speed mode (1/2 dividing clock).

Supply voltage (V_{DD}) 3.0 to 3.6V(T_a = -20 to +75°C, V_{SS} = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V _{OH}	PA to PE, PF4 to PF7, PH (V _{OL} only)	V _{DD} = 3.0V, I _{OH} = −0.15mA	2.7			V
			V _{DD} = 3.0V, I _{OH} = −0.5mA	2.3			V
Low level output voltage	V _{OL}	PI1 to PI7, PJ, SO, SCK, RST*1 (V _{OL} only)	V _{DD} = 3.0V, I _{OL} = 1.2mA			0.3	V
			V _{DD} = 3.0V, I _{OL} = 1.6mA			0.5	V
		PD, PH	V _{DD} = 3.0V, I _{OL} = 5.0mA			1.0	V
Input current	I _{IHE}	EXTAL	V _{DD} = 3.6V, V _{IH} = 3.6V	0.3		20	μA
	I _{IIE}		V _{DD} = 3.6V, V _{IL} = 0.3V	−0.3		−20	μA
	I _{ILR}	RST*2	V _{DD} = 3.6V, V _{IL} = 0.3V	−0.9		−200	μA
I/O leakage current	I _{Iz}	PA to PK, MP, AN0 to AN3, CS, SI, SO, SCK, RST*2	V _{DD} = 5.5V, V _I = 0, 5.5V			±10	μA
Supply current*3	I _{DD2}	V _{DD}	Crystal oscillation (C ₁ = C ₂ = 15pF) of 12MHz		15	30	mA
			V _{DD} = 3.3V ± 0.3V*4				
	I _{DD2}		SLEEP mode		0.8	2.5	mA
			V _{DD} = 3.3V ± 0.3V				
	I _{DD3}		STOP mode				10
		V _{DD} = 5.5V					
Input capacity	C _{IN}	Other than V _{DD} , V _{SS} , AV _{DD} , and AV _{SS} pins	Clock 1MHz 0V other than the measured pins		10	20	pF

*1 $\overline{\text{RST}}$ pin specifies only where the power on reset circuit has been selected with mask option.*2 $\overline{\text{RST}}$ pin specifies the input current when the pull-up resistor is selected, and specifies leakage current when non-resistance is selected.

*3 When entire output pins are open.

*4 When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FEh) to "00" and operating in high speed mode (1/2 dividing clock).

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, VDD = 3.0 to 5.5V, VSS = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2 VDD = 4.5 to 5.5V	1	16	MHz
				1	12	
System clock input pulse width	t _{XL} , t _{XH}	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive) VDD = 4.5 to 5.5V	28		ns
				37.5		
System clock input rising and falling times	t _{CR} , t _{CF}	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive)		200	ns
Event count clock input pulse width	t _{EL} , t _{EH}	PE1/ $\overline{EC}$	Fig. 3	t _{sys} × 4*		ns
Event count clock input rising and falling times	t _{ER} , t _{EF}	PE1/ $\overline{EC}$	Fig. 3		20	ms

* t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Fig. 1. Clock timing

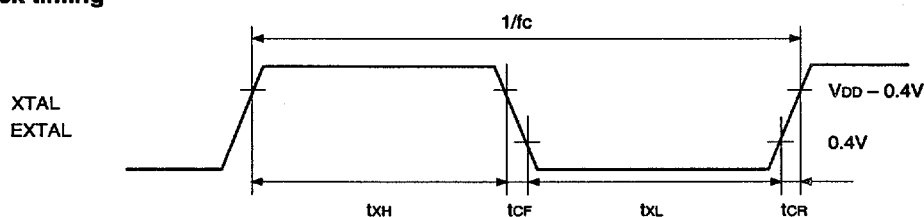


Fig. 2. Clock applied condition

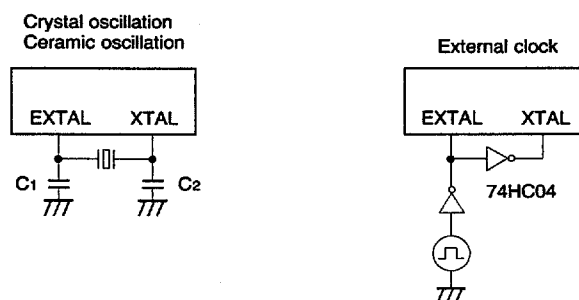
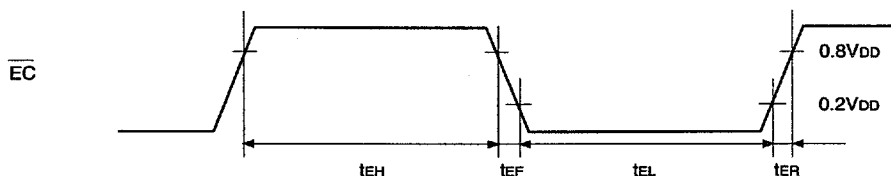


Fig. 3. Event count clock timing



(2) Serial transfer (CH0)

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		$t_{sys} + 20$	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		$t_{sys} + 20$	ns
$\overline{CS} \downarrow \rightarrow SO$ delay time	t_{DCSO}	SO0	Chip select transfer mode		$t_{sys} + 20$	ns
$\overline{CS} \downarrow \rightarrow SO$ floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		$t_{sys} + 20$	ns
$\overline{CS}$ high level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	$t_{sys} + 200$		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	$2t_{sys} + 200$		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	$t_{sys} + 100$		ns
			Output mode	8000/fc - 100		ns
SI input setup time (against $\overline{SCK} \uparrow$)	t_{SIK}	SI0	$\overline{SCK}$ input mode	$-t_{sys} + 100$		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (against $\overline{SCK} \uparrow$)	t_{KSI}	SI0	$\overline{SCK}$ input mode	$2t_{sys} + 100$		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK} \downarrow \rightarrow SO$ delay time	t_{KSO}	SO0	$\overline{SCK}$ input mode		$2t_{sys} + 200$	ns
			$\overline{SCK}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) $\overline{CS}$, $\overline{SCK}$, SI and SO means each pin of $\overline{CS} \rightarrow \overline{CS0}$, $\overline{SCK} \rightarrow \overline{SCK0}$, SI $\rightarrow$ SI0, and SO $\rightarrow$ SO0 respectively.

Note 3) The load of $\overline{SCK}$ output mode and SO output delay time is 50pF + 1TTL.

Serial transfer (CH0)

(Ta = -20 to +75°C, VDD = 3.0 to 3.6V, VSS = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	tDCSK	$\overline{SCK0}$	Chip select transfer mode (SCK = output mode)		tsys + 25	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ floating delay time	tDCSKF	$\overline{SCK0}$	Chip select transfer mode (SCK = output mode)		tsys + 20	ns
$\overline{CS} \downarrow \rightarrow SO$ delay time	tDCSO	SO0	Chip select transfer mode		tsys + 25	ns
$\overline{CS} \downarrow \rightarrow SO$ floating delay time	tDCSOF	SO0	Chip select transfer mode		tsys + 20	ns
$\overline{CS}$ high level width	tWHCS	$\overline{CS0}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK}$ cycle time	tKCY	$\overline{SCK0}$	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK}$ high and low level widths	tKH tKL	$\overline{SCK0}$	Input mode	tsys + 100		ns
			Output mode	8000/fc - 150		ns
SI input setup time (against $\overline{SCK} \uparrow$)	tSIK	SI0	$\overline{SCK}$ input mode	-tsys + 100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (against $\overline{SCK} \uparrow$)	tKSI	SI0	$\overline{SCK}$ input mode	2tsys + 100		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK} \downarrow \rightarrow SO$ delay time	tKSO	SO0	$\overline{SCK}$ input mode		2tsys + 250	ns
			$\overline{SCK}$ output mode		125	ns

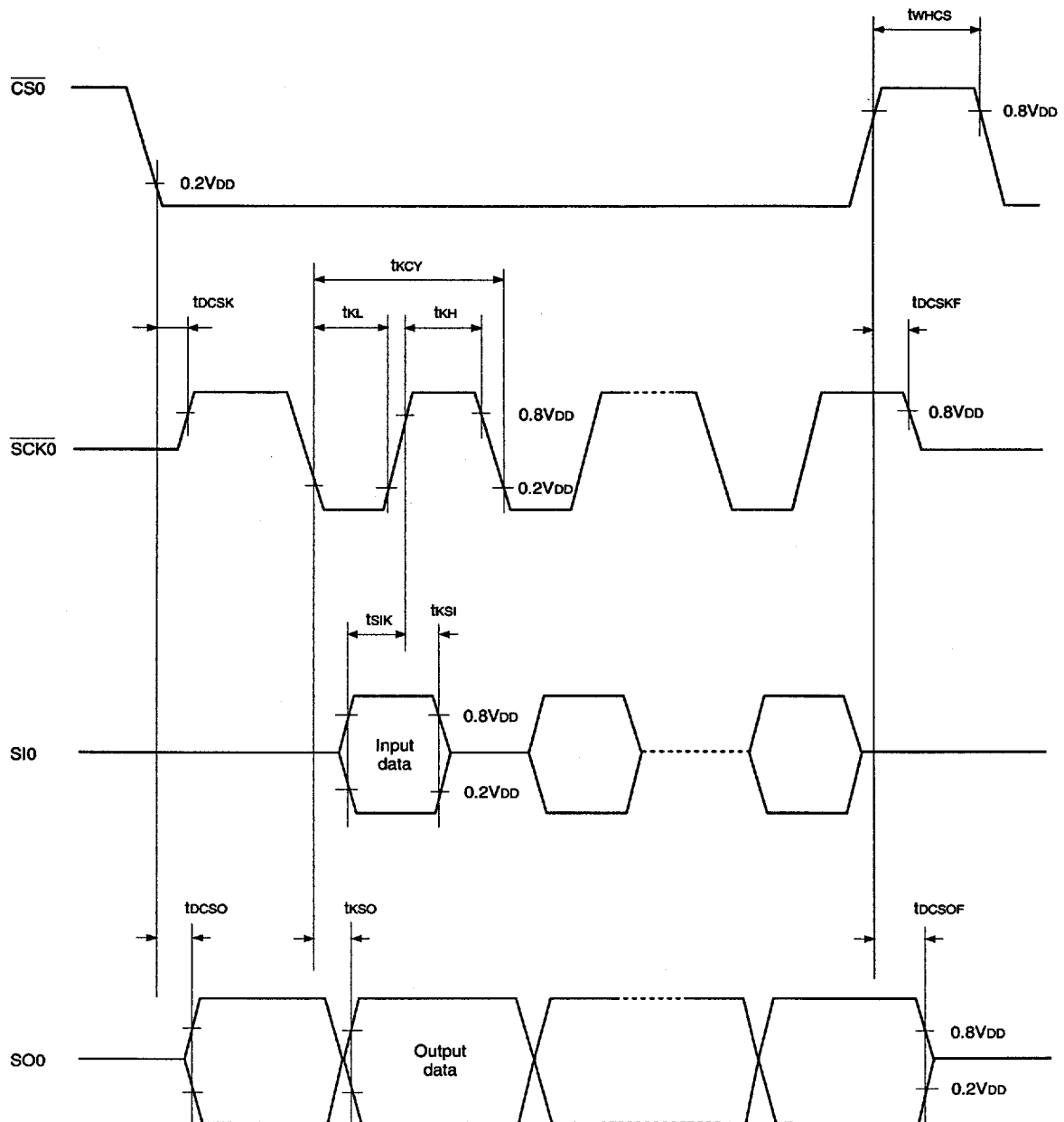
Note 1) tsys indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) $\overline{CS}$, $\overline{SCK}$, SI and SO means each pin of $\overline{CS} \rightarrow \overline{CS0}$, $\overline{SCK} \rightarrow \overline{SCK0}$, SI $\rightarrow$ SI0, and SO $\rightarrow$ SO0 respectively.

Note 3) The load of $\overline{SCK}$ output mode and SO output delay time is 50pF.

Fig. 4. Serial transfer timing (CH0)



Serial transfer (CH1) (SIO mode)

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY}	$\overline{\text{SCK1}}$	Input mode	$2t_{\text{sys}} + 200$		ns
			Output mode	$16000/f_c$		ns
$\overline{\text{SCK1}}$ high and low level widths	t_{KH} t_{KL}	$\overline{\text{SCK1}}$	Input mode	$t_{\text{sys}} + 100$		ns
			Output mode	$8000/f_c - 100$		ns
SI1 input setup time (against $\overline{\text{SCK1}}$ ↑)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (against $\overline{\text{SCK1}}$ ↑)	t_{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	$t_{\text{sys}} + 200$		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}} \downarrow \rightarrow \text{SO1}$ delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		$t_{\text{sys}} + 200$	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = $2000/f_c$ (Upper 2 bits = "00"), $4000/f_c$ (Upper 2 bits = "01"), $16000/f_c$ (Upper 2 bits = "11")

Note 2) The load of $\overline{\text{SCK1}}$ output mode and SO1 output delay time is 50pF + 1TTL.

Serial transfer (CH1) (SIO mode)

(Ta = -20 to +75°C, VDD = 3.0 to 3.6V, VSS = 0V)

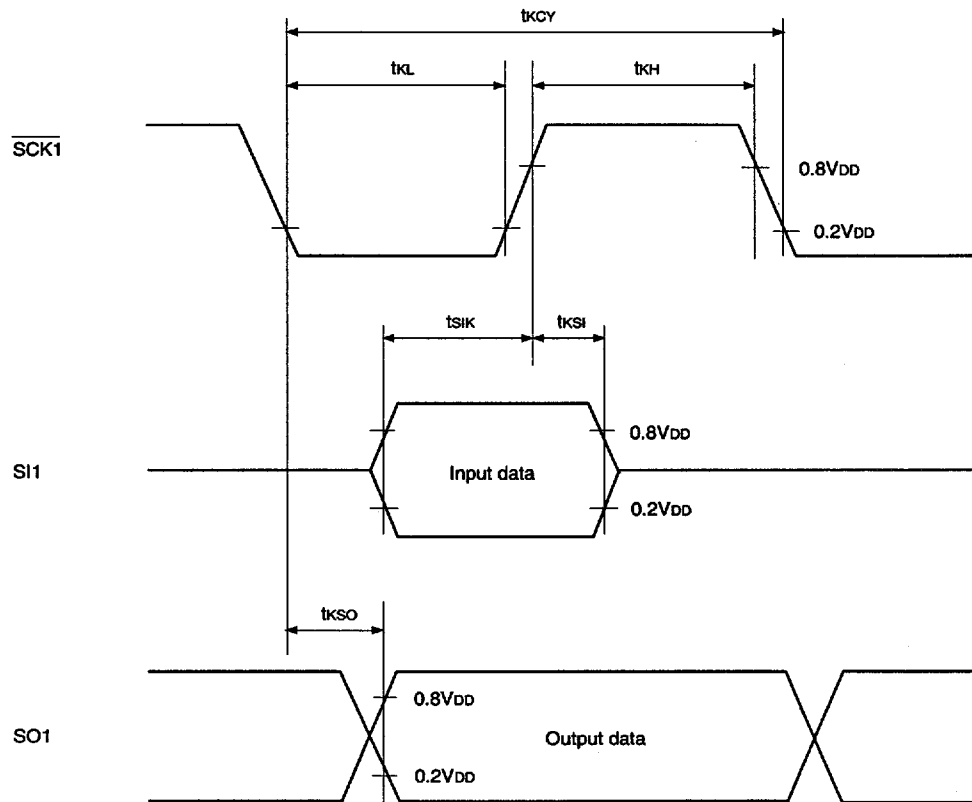
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY}	$\overline{\text{SCK1}}$	Input mode	$2t_{\text{sys}} + 200$		ns
			Output mode	$16000/f_c$		ns
$\overline{\text{SCK1}}$ high and low level widths	t_{KH} t_{KL}	$\overline{\text{SCK1}}$	Input mode	$t_{\text{sys}} + 100$		ns
			Output mode	$8000/f_c - 150$		ns
SI1 input setup time (against $\overline{\text{SCK1}}$ ↑)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (against $\overline{\text{SCK1}}$ ↑)	t_{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	$t_{\text{sys}} + 200$		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}} \downarrow \rightarrow \text{SO1}$ delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		$t_{\text{sys}} + 250$	ns
			$\overline{\text{SCK1}}$ output mode		125	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = $2000/f_c$ (Upper 2 bits = "00"), $4000/f_c$ (Upper 2 bits = "01"), $16000/f_c$ (Upper 2 bits = "11")

Note 2) The load of $\overline{\text{SCK1}}$ output mode and SO1 output delay time is 50pF.

Fig. 5. Serial transfer CH1 timing (SIO mode)



Serial transfer (CH1) (Special mode)

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
SO1 cycle time	t _{LCY}	SO1 SI1	Note 1)		104		μs
SI1 data setup time	t _{LSU}	SI1		2			μs
SI1 data hold time	t _{LHD}	SI1		2			μs

Note 1) t_{LCY} specifies only serial mode register (CH1) (SIOM1: Address 01FAh) lower 2 bits (SO1 clock selection) has been set at 104μs.

Note 2) The load of SO1 pin is 50pF + 1TTL.

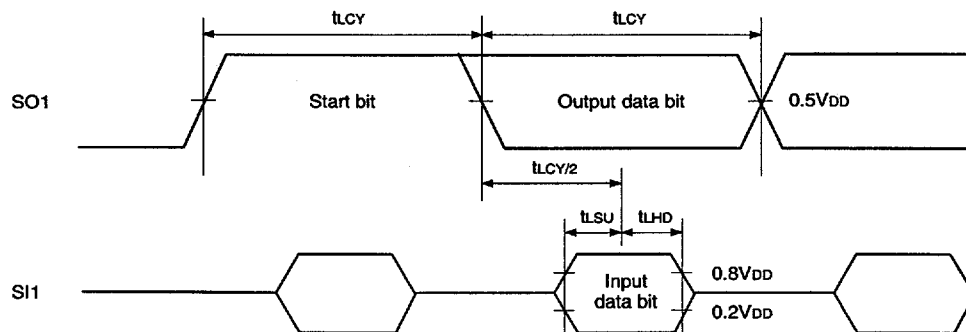
Serial transfer (CH1) (Special mode)

(Ta = -20 to +75°C, VDD = 3.0 to 3.6V, VSS = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
SO1 cycle time	t _{LCY}	SO1 SI1	Note 1)		104		μs
SI1 data setup time	t _{LSU}	SI1		2			μs
SI1 data hold time	t _{LHD}	SI1		2			μs

Note 1) t_{LCY} specifies only serial mode register (CH1) (SIOM1: Address 01FAh) lower 2 bits (SO1 clock selection) has been set at 104μs.

Note 2) The load of SO1 pin is 50pF.

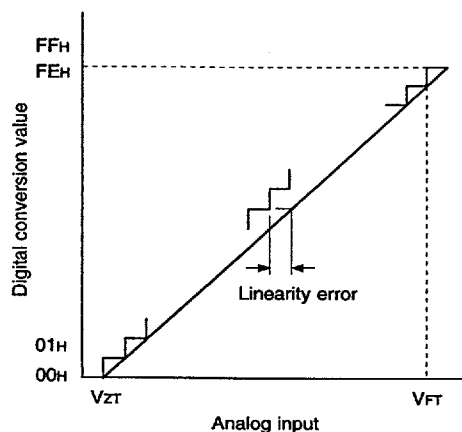
Fig. 6. Serial transfer CH1 timing (Special mode)

(3) A/D converter characteristics ($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = AV_{DD} = 4.5$ to 5.5V , $AV_{REF} = 4.0$ to AV_{DD} , $V_{SS} = AV_{SS} = 0\text{V}$)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Only for A/D converter operation $T_a = 25^\circ\text{C}$			± 1	LSB
Absolute error			$V_{DD} = AV_{DD} = AV_{REF} = 5.0\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$			± 2	LSB
Conversion time	t_{CONV}			$160/f_{ADC}$			μs
Sampling time	t_{SAMP}			$12/f_{ADC}$			μs
Reference input voltage	V_{REF}	AV_{REF}	$V_{DD} = AV_{DD} = 4.5$ to 5.5V	$AV_{DD} - 0.5$		AV_{DD}	V
Analog input voltage	V_{IAN}	$AN0$ to $AN11$		0		AV_{REF}	V
AVREF current	I_{REF}	AV_{REF}	Operating mode $AV_{REF} = 4.0$ to 5.5V		0.6	1.0	mA
			SLEEP mode STOP mode			10	μA

A/D converter characteristics ($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = AV_{DD} = 3.0$ to 3.6V , $AV_{REF} = 2.7$ to AV_{DD} , $V_{SS} = AV_{SS} = 0\text{V}$)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Only for A/D converter operation $T_a = 25^\circ\text{C}$			± 1	LSB
Absolute error			$V_{DD} = AV_{DD} = AV_{REF} = 3.3\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$			± 2	LSB
Conversion time	t_{CONV}			$160/f_{ADC}$			μs
Sampling time	t_{SAMP}			$12/f_{ADC}$			μs
Reference input voltage	V_{REF}	AV_{REF}	$V_{DD} = AV_{DD} = 3.0$ to 3.6V	$AV_{DD} - 0.3$		AV_{DD}	V
Analog input voltage	V_{IAN}	$AN0$ to $AN11$		0		AV_{REF}	V
AVREF current	I_{REF}	AV_{REF}	Operating mode $AV_{REF} = 2.7$ to 3.6V		0.4	0.7	mA
			SLEEP mode STOP mode			10	μA

Fig. 7. Definitions of A/D converter terms

* The value of f_{ADC} is as follows by selecting ADC operation clock (MSC: Address 01FFH bit 0).

When PS2 is selected, $f_{ADC} = f_c/2$

When PS1 is selected, $f_{ADC} = f_c$

(4) Interruption, reset input

(Ta = -20 to +75°C, VDD = 3.0 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t_{IH} t_{IL}	$\overline{INT0}$ $\overline{INT1}$ $\overline{INT2}$ PJ0 to PJ7		1		μs
Reset input low level width	t_{RSL}	$\overline{RST}$		32/fc		μs

Fig. 8. Interruption input timing

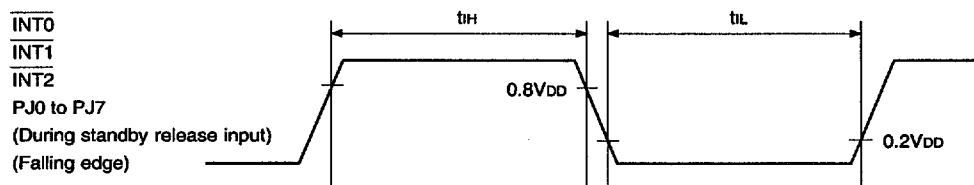
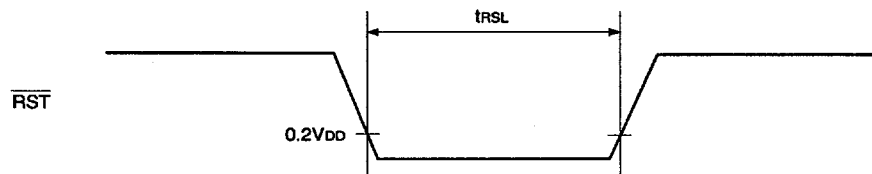


Fig. 9. Reset input timing



(5) Power on reset

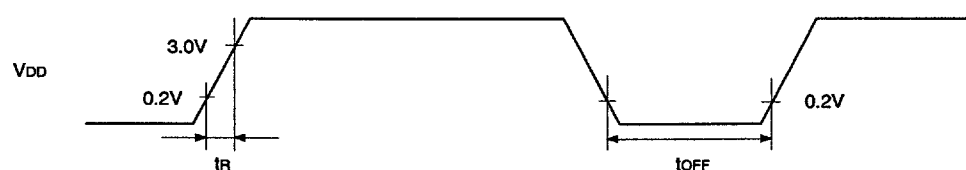
Power on reset*

(Ta = -20 to +75°C, VDD = 3.0 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rising edge	t_r	VDD	Power on reset	0.05	30	ms
Power supply cut-off time	t_{OFF}		Repetitive power on reset	1		ms

* Specifies only when power on reset function is selected.

Fig. 10. Power on reset



The power supply should rise smoothly.

(6) General purpose prescaler

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

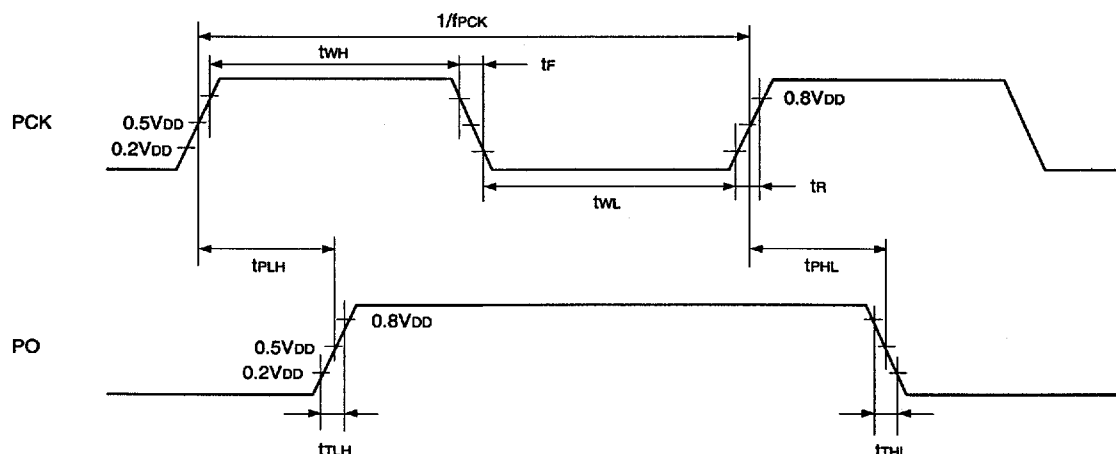
Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
External clock input frequency	f _{PCK}	PCK				12	MHz
External clock input pulse width	t _{WH} , t _{WL}	PCK		33			ns
External clock input rising and falling times	t _R , t _F	PCK				200	ns
Prescaler output delay time (against PCK ↑)	t _{PLH}	PO	External clock input PCK t _R = t _F = 6ns		80	130	ns
	t _{PHL}				60	100	ns
Prescaler output rising and falling times	t _{TLH}	PO	External clock input PCK t _R = t _F = 6ns		50	100	ns
	t _{THL}				20	40	ns

Note) The load of PO pin is 50pF.

General purpose prescaler

(Ta = -20 to +75°C, VDD = 3.0 to 3.6V, VSS = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
External clock input frequency	f _{PCK}	PCK				12	MHz
External clock input pulse width	t _{WH} , t _{WL}	PCK		33			ns
External clock input rising and falling times	t _R , t _F	PCK				200	ns
Prescaler output delay time (against PCK ↑)	t _{PLH}	PO	External clock input PCK t _R = t _F = 6ns		130	220	ns
	t _{PHL}				90	150	ns
Prescaler output rising and falling times	t _{TLH}	PO	External clock input PCK t _R = t _F = 6ns		100	280	ns
	t _{THL}				30	70	ns

Note) The load of PO pin is 50pF.**Fig. 11. General purpose prescaler timing**

(7) Others

(Ta = -20 to +75°C, V_{DD} = 3.0 to 5.5V, V_{SS} = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
CFG input high and low level widths	t _{CFH} t _{CFL}	CFG		t _{FRC} × 24 + 200		ns
DFG input high and low level widths	t _{DFH} t _{DFL}	DFG		t _{FRC} × 8 + 200		ns
DPG minimum pulse width	t _{DPW}	DPG		50		ns
DPG minimum removal time	t _{rem}	DPG		50		ns
$\overline{\text{PBCTL}}$ input high and low level widths	t _{CTH} t _{CTL}	$\overline{\text{PBCTL}}$	t _{sys} = 2000/f _c	t _{FRC} × 8 + t _{sys} + 200		ns
EXI input high and low level widths	t _{EIH} t _{EIL}	EXI0 EXI1	t _{sys} = 2000/f _c	t _{FRC} × 8 + t _{sys} + 200		ns
PMI input high and low level widths	t _{PIH} t _{PIL}	PMI		t _{sys} + 200		ns
PMSK input high and low level widths	t _{PSH} t _{PSL}	PMSK		t _{sys} + 200		ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

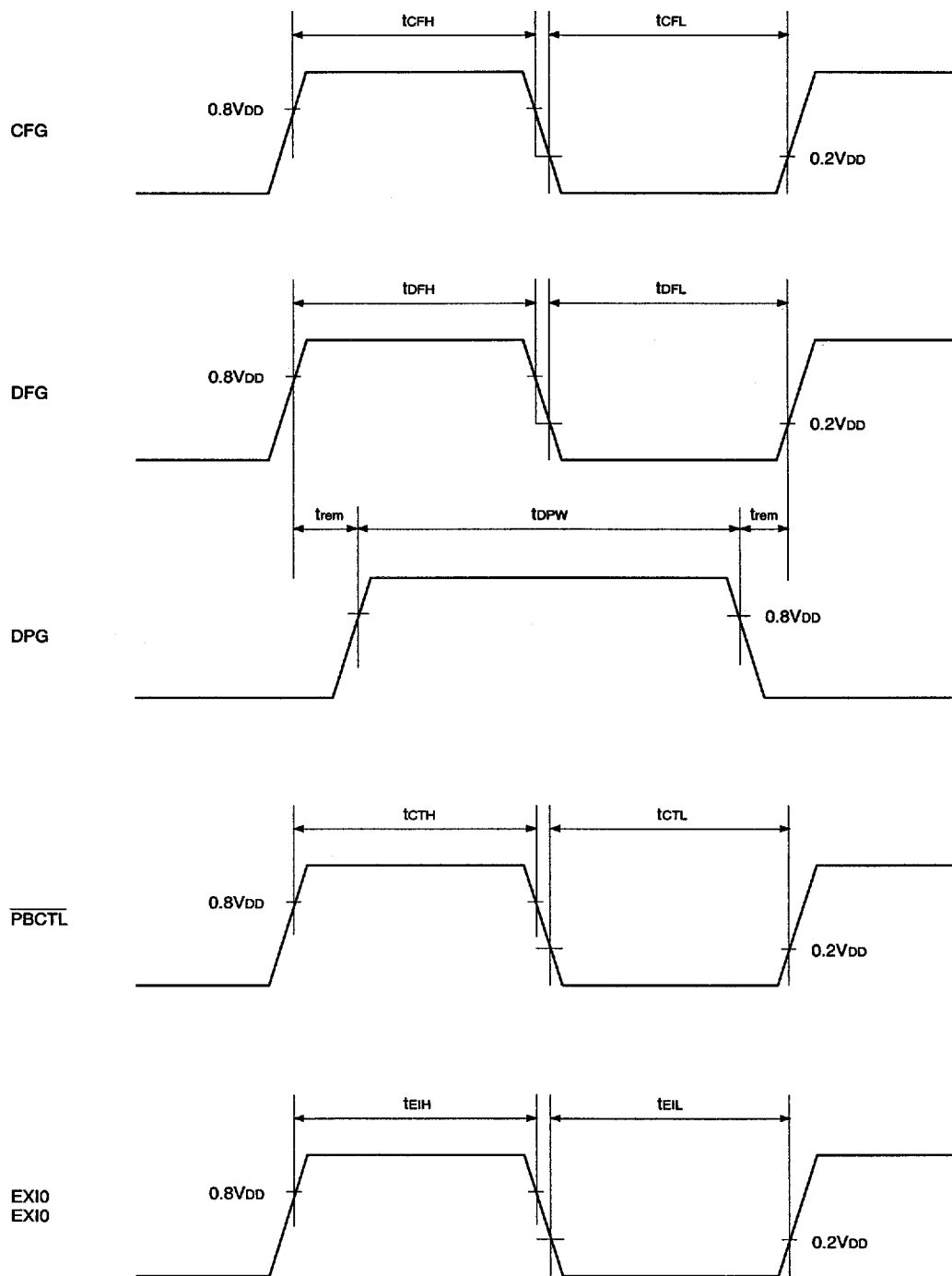
t_{sys} [ns] = 2000/f_c (Upper 2 bits = "00"), 4000/f_c (Upper 2 bits = "01"), 16000/f_c (Upper 2 bits = "11")

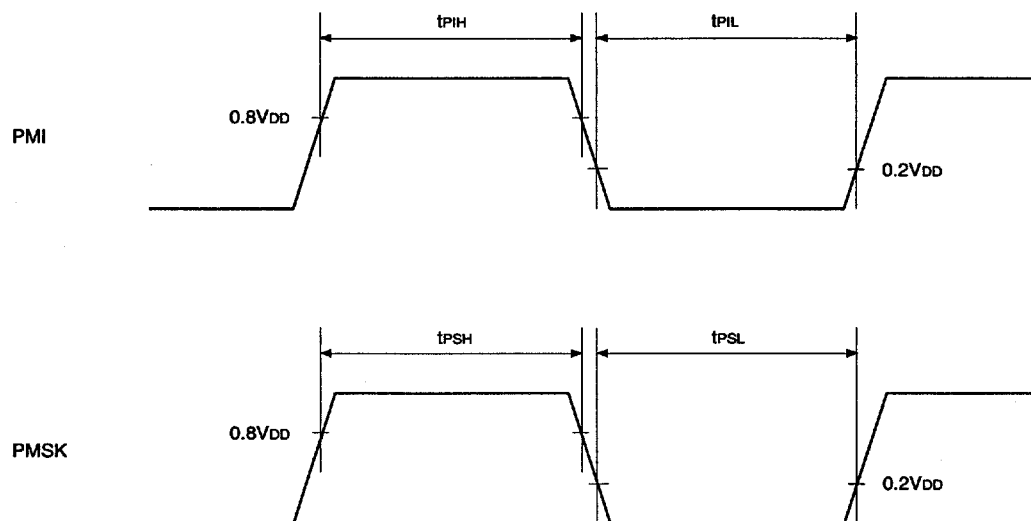
Note 2) The value of t_{FRC} is as follows by selecting FRC clock (FRCS: 01EEH bit 7)

When PS0 is selected, t_{FRC} = 1000/f_c (ns)

When PS1 is selected, t_{FRC} = 2000/f_c (ns)

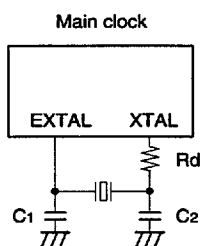
Fig. 12. Other timings





Supplement

Fig. 13. Recommended oscillation circuit



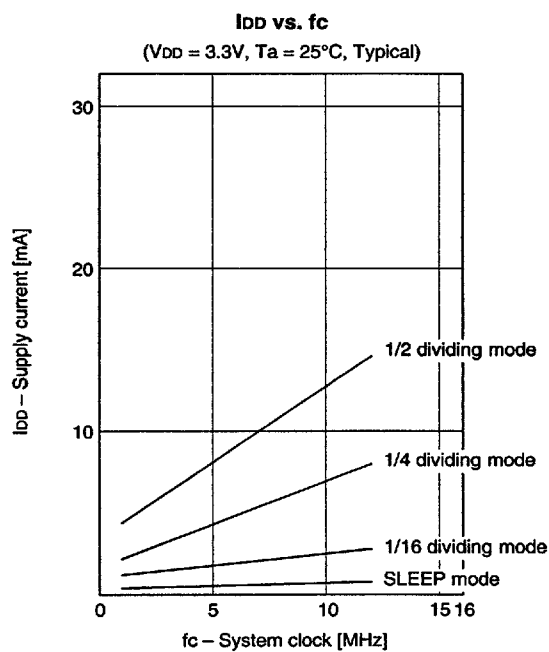
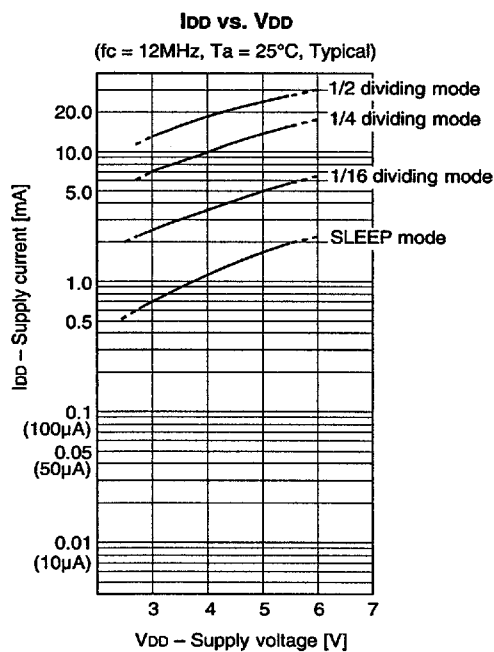
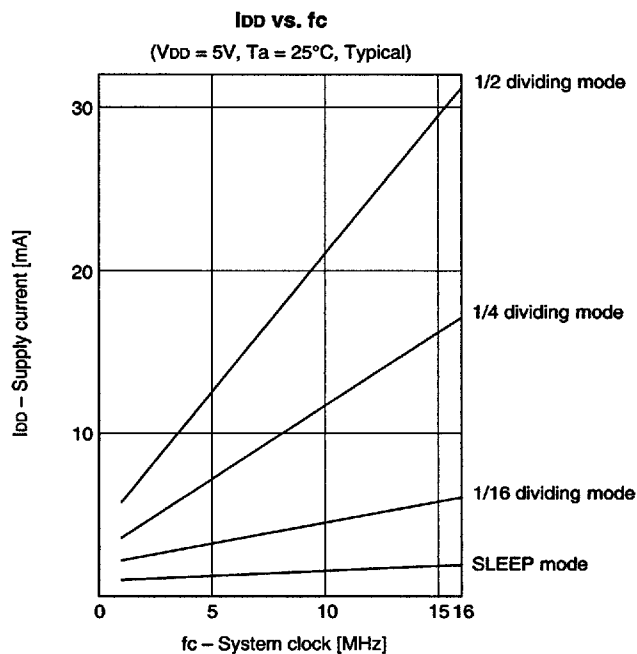
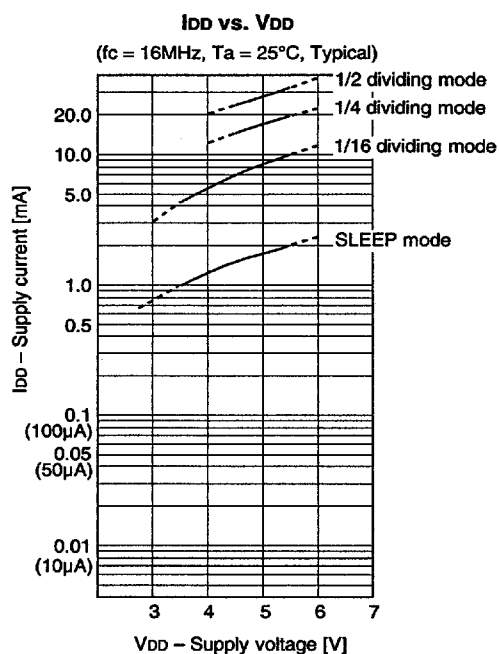
Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00	5	5		
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	22 (15)	22 (15)	0	(i)
		10.00				
		12.00	15	15		
		16.00	12	12		

Mask Option Table

Item	Content	
Reset pin pull-up resistor	Non-existent	Existent
Power on reset circuit	Non-existent	Existent
General purpose prescaler oscillation circuit	Non-existent	Existent
Input circuit format*	CMOS schmitt	TTL schmitt

* In PG4/SYNC0/PMI pin and PG5/SYNC1 pin, the input circuit format can be selected every pin.
However, TTL schmitt can not be selected when the supply voltage (V_{DD}) ranges from 3.5V to 5.5V.

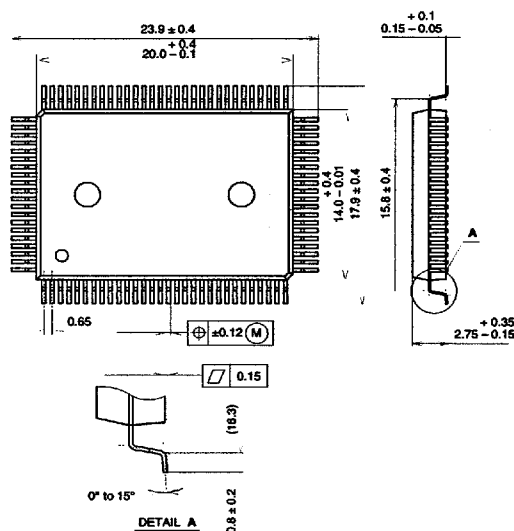
Characteristics Curve



Package Outline

Unit: mm

100PIN QFP (PLASTIC)

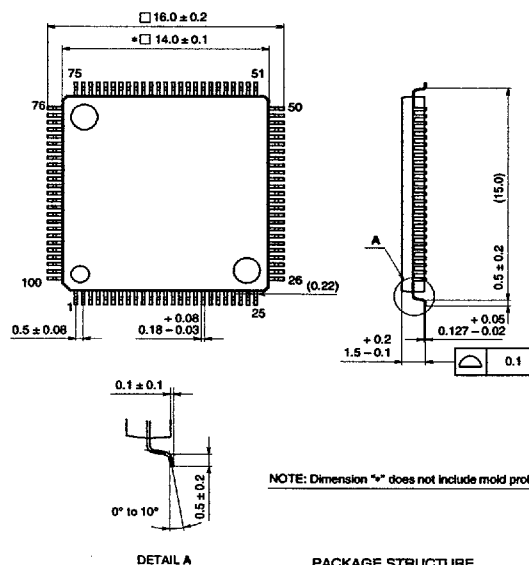


PACKAGE STRUCTURE

SONY CODE	QFP-100P-L01
EIAJ CODE	*QFP100-P-1420-A
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.4g

100PIN LQFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	LQFP-100P-L01
EIAJ CODE	*QFP100-P-1414-A
JEDEC CODE	

PACKAGE MATERIAL	EPOXY/PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	