National Semiconductor

CD4522BM/CD4522BC, CD4526BM/CD4526BC Programmable Divide-By-N 4-Bit Binary Counter

General Description

The CD4522BM/CD4522BC, CD4526BM/CD4526BC are CMOS programmable cascadable down counters with a decoded "0" state output for divide-by-N applications. In single stage applications, the "0" output is applied to the Preset Enable input. For multi-stage applications, the "0" output is used in conjunction with the CF (Cascade Feedback) input to perform the divide-by-N function. The "0" output is normally at logical "0" level; it will go to a logical "1" state only when the counter is at its terminal count (0000) and if CF is at logical "1" level. Thus, CF acts as an active low inhibit for the "0" output. This feature allows cascade divide-by-N operations with no additional gate required (see Applications section). The Master Reset function provides synchronous initiation of divide-by-N cycles. The Clock Inhibit input allows disabling of the pulse counting function.

All inputs are protected against static discharge by diode clamps to V_{DD} and V_{SS}.

Features

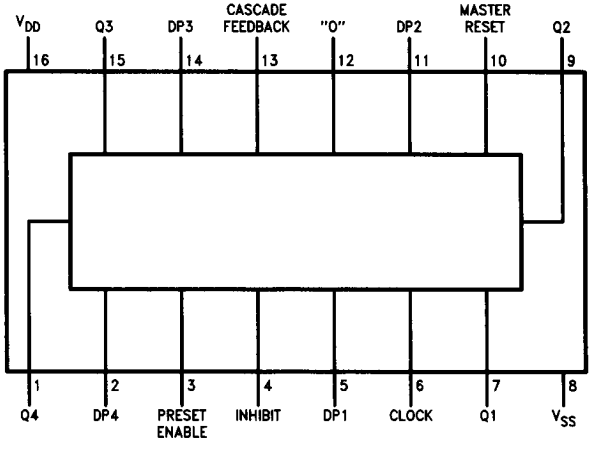
- Wide supply voltage range 3.0V to 18V
- High noise immunity 0.45 V_{DD} (typ.)
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- Quiescent current = 5 nA/package (typ.)@V_{DD} = 5.0V
- Internally synchronous for high internal and external speed
- Logic edge-clocked design—incremented on positive transition of Clock or negative transition of Clock Inhibit
- Medium speed 7.7 MHz (typ.)@V_{DD} = 10V
- Asynchronous Preset Enable

Applications

- Programmable down counter
- Programmable frequency divider
- Frequency synthesizers
- Phase-locked loops

Connection Diagram

Dual-In-Line Package



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Top View

Order Number CD4522B* or CD4526B*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
Input Voltage (V_{IN})	$-0.5\ V_{DC}$ to $V_{DD} + 0.5\ V_{DC}$
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

DC Supply Voltage (V_{DD})	$3\ V_{DC}$ to $15\ V_{DC}$
Input Voltage (V_{IN})	$0\ V_{DC}$ to $V_{DD}\ V_{DC}$
Operating Temperature Range (T_A)	
CD4522BM, CD4526BM	$-55°C$ to $+125°C$
CD4522BC, CD4526BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4522BM, CD4526BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		5		0.005	5		150	μA
		$V_{DD} = 10V$		10		0.010	10		300	μA
		$V_{DD} = 15V$		20		0.015	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or 4.5V		1.5			1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1.0V$ or 9.0V		3.0			3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or 4.5V	3.5		3.5			3.5		V
		$V_{DD} = 10V$, $V_O = 1.0V$ or 9.0V	7.0		7.0			7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.6		−1.3	−2.25		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4522BC, CD4526BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		20		0.005	20		150	μA
		$V_{DD} = 10V$		40		0.010	40		300	μA
		$V_{DD} = 15V$		80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V

DC Electrical Characteristics CD4522BC, CD4526BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics* T_A = 25°C, C_L = 50 pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{THL}, t_{TLH}	Output Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{PHL}, t_{PLH}	Propagation Delay Time from Clock to Q Outputs	V_{DD} = 5V		350	825	ns
		V_{DD} = 10V		130	345	ns
		V_{DD} = 15V		90	240	ns
t_{PHL}, t_{PLH}	Propagation Delay Time from Clock to "0" Output	V_{DD} = 5V		200	500	ns
		V_{DD} = 10V		80	250	ns
		V_{DD} = 15V		60	190	ns
PW_C	Minimum Clock Pulse Width	V_{DD} = 5V		120	280	ns
		V_{DD} = 10V		50	120	ns
		V_{DD} = 15V		35	85	ns
f_{CL}	Maximum Clock Pulse Frequency	V_{DD} = 5V	1.5	2.9		MHz
		V_{DD} = 10V	3.0	7.7		MHz
		V_{DD} = 15V	4.0	11		MHz
T_{rCL}, T_{fCL}	Maximum Clock or Inhibit Rise and Fall Time	V_{DD} = 5V	15			μs
		V_{DD} = 10V	15			μs
		V_{DD} = 15V	15			μs
t_{HOLD}	Hold Time	V_{DD} = 5V		40	125	ns
		V_{DD} = 10V		25	50	ns
		V_{DD} = 15V		20	40	ns
PW_{PE}	Minimum Preset Enable Pulse Width	V_{DD} = 5V		120	280	ns
		V_{DD} = 10V		50	120	ns
		V_{DD} = 15V		35	85	ns
PW_{MR}	Minimum Master Reset Pulse Width	V_{DD} = 5V		160	350	ns
		V_{DD} = 10V		75	180	ns
		V_{DD} = 15V		50	120	ns
C_{IN}	Input Capacitance	(Note 4)		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 5)		100		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

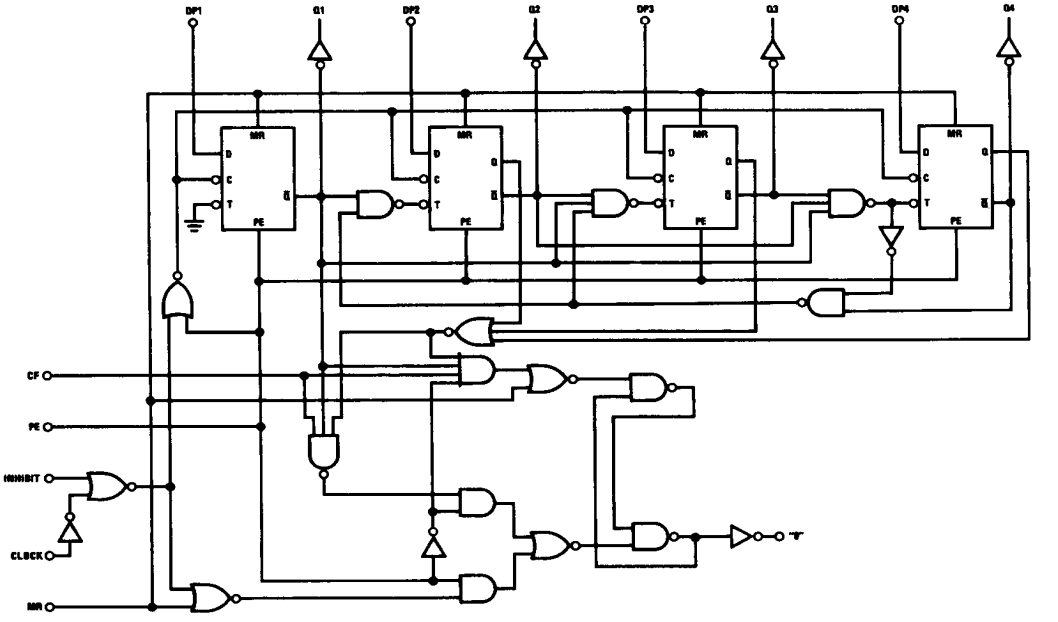
Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: Capacitance is guaranteed by periodic testing.

Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

Logic Diagrams

CD4522BM/CD4522BC



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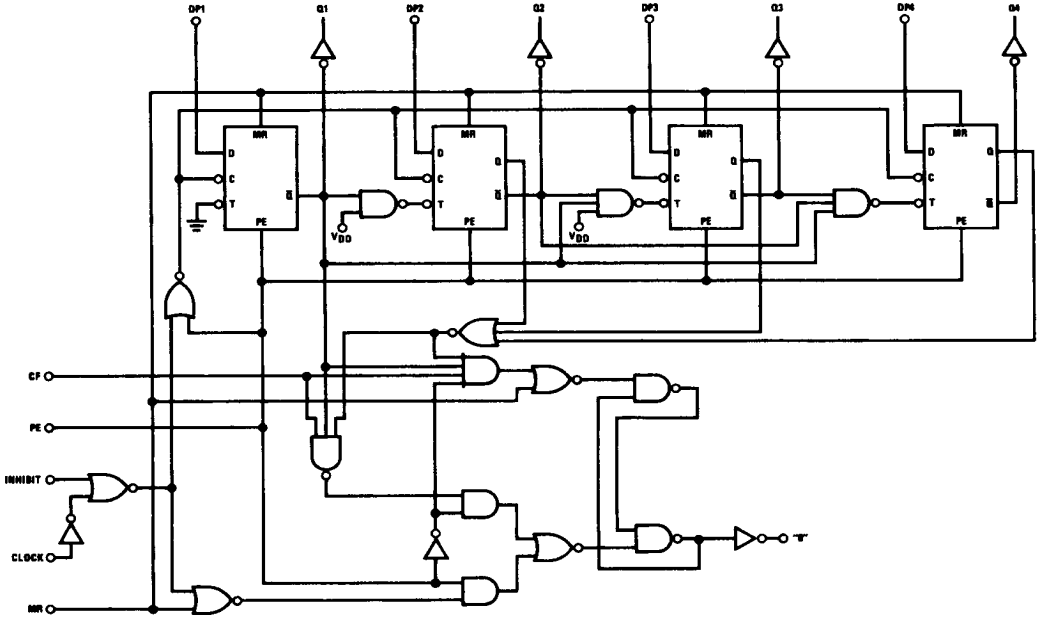
CD4526BM/CD4526BC



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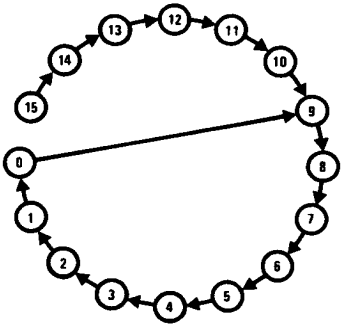
Truth Tables and Count Sequences

Both Types

Clock	Inhibit	Preset Enable	Master Reset	Action
0	0	0	0	No Count
⌐‾	0	0	0	Count 1
X	1	0	0	No Count
1	‾⌐	0	0	Count 1
X	X	1	0	Preset
X	X	X	1	Reset

CD4522BM/CD4522BC

Count	Output			
	Q4	Q3	Q2	Q1
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0



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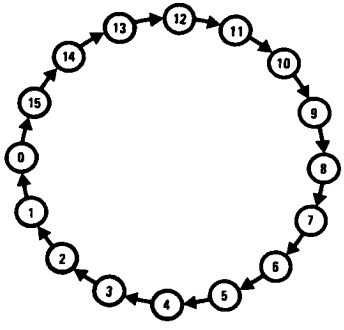
CD4526BM/CD4526BC

Count	Output			
	Q4	Q3	Q2	Q1
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0



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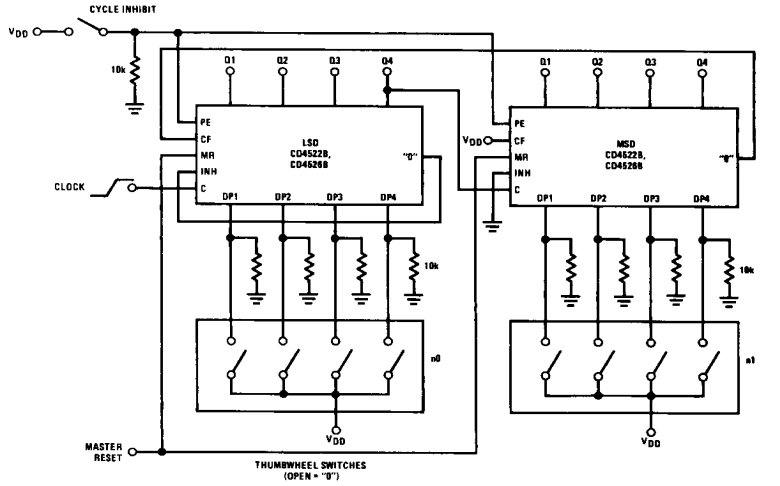
Typical Applications

2-Stage Programmable Down Counter



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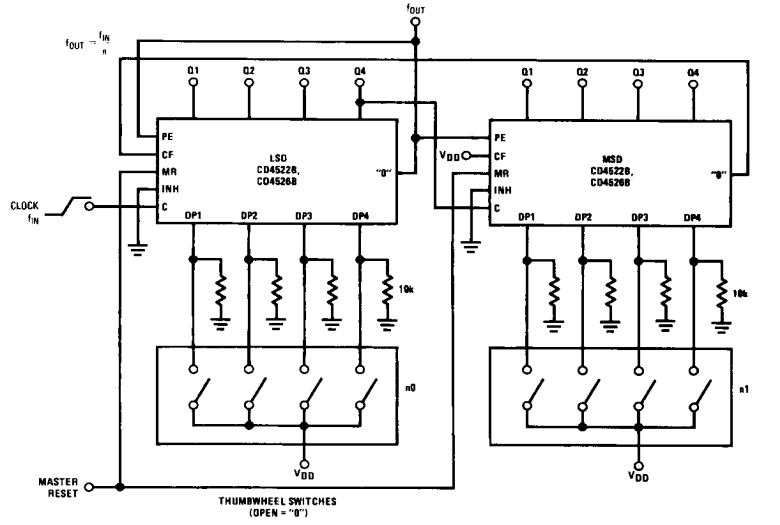
Counting Cycle

LSD	MSD
n0	
n0 − 1	
•	
•	n1
•	
1	
0	
9 (15)	
8 (14)	
•	
•	n1 − 1
•	
1	
0	
•	•
•	•
•	•
9 (15)	
8 (14)	
•	
•	0
•	
1	
0	
↓ STOP	

2-Stage Programmable Fequency Divider



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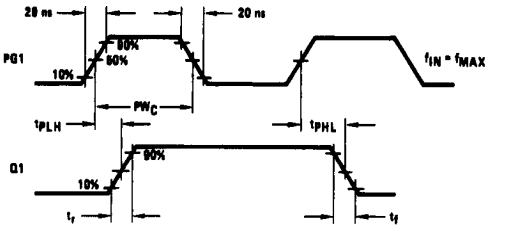
Counting Cycle

LSD	MSD
n0	
n0 − 1	
•	
•	n1
•	
1	
0	
9 (15)	
8 (14)	
•	
•	n1 − 1
•	
1	
0	
•	•
•	•
•	•
9 (15)	
8 (14)	
•	
•	0
•	
1	
0	
↓ REPEAT CYCLE	

Note: When cascading more than 2 packages, tie "0" output of the nth package to CF input of the (n − 1)th package for all n = 2, 3.

Switching Time Waveforms

Test No. 1



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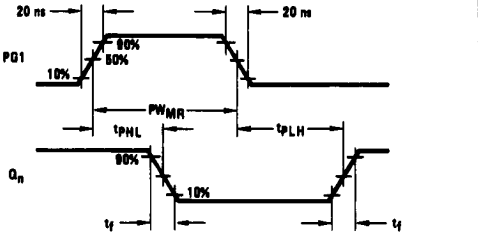
Test No. 4



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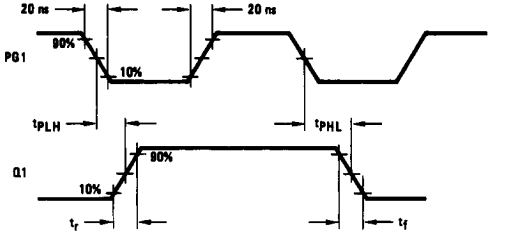
Test No. 2



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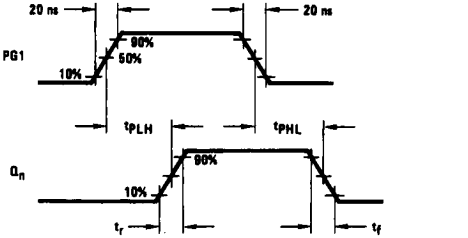
Tests No. 5 and 7



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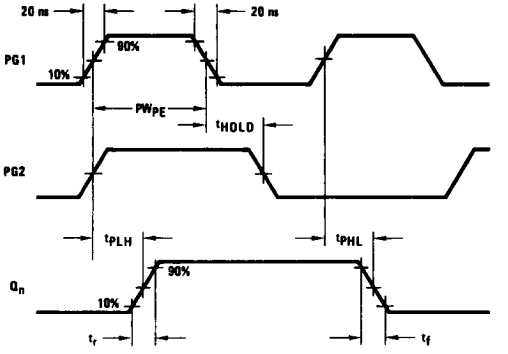
Test No. 3



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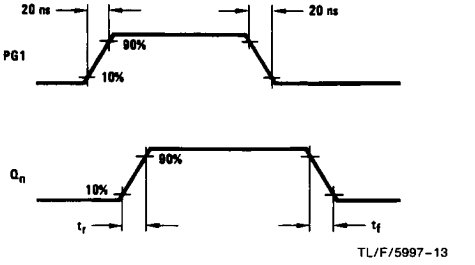
Test No. 6



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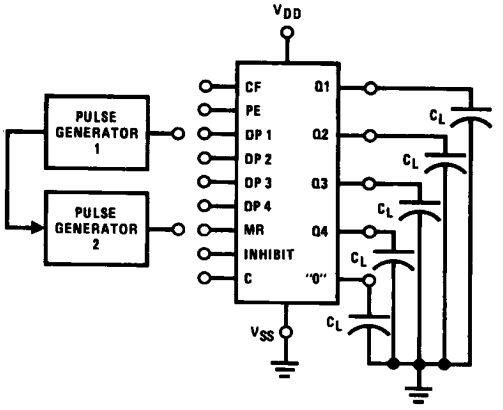
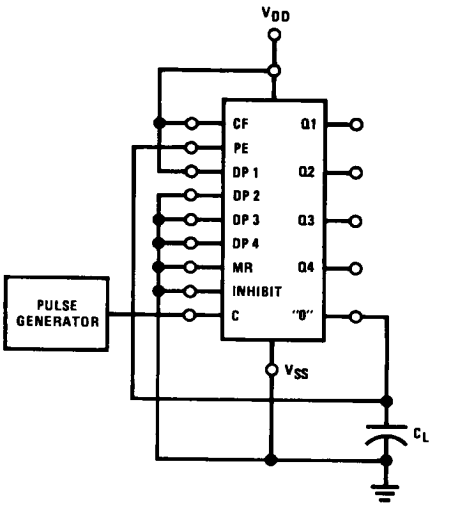
AC Test Circuits



a) Tests No. 1–6



b) Test No. 7

FIGURE 1. Test Circuits

Test Conditions

TABLE I

Characteristic	Test No.	Clock	Inhibit	PE	MR	DP_n	CF	Output
t_r, t_f, t_{PLH}, t_{PHL}	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
	2	V_{DD}	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
	4	V_{SS}	V_{SS}	V_{DD}	PG1	V_{DD}	V_{SS}	Q_n
	5	V_{SS}	V_{SS}	V_{DD}	V_{SS}	PG1	V_{SS}	Q_n
PW_{MR}	4	V_{SS}	V_{SS}	V_{DD}	PG1	V_{DD}	V_{SS}	Q_n
PW_{PE}	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
PW_C	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
f_{MAX}	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
t_{HOLD}	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
t_r, t_f	6	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{SS}	PG1	"0"
t_{PLH}, t_{PHL}	7	PG	V_{SS}	*Fig. 1b*	V_{SS}	*Fig. 1b*	V_{DD}	"0"