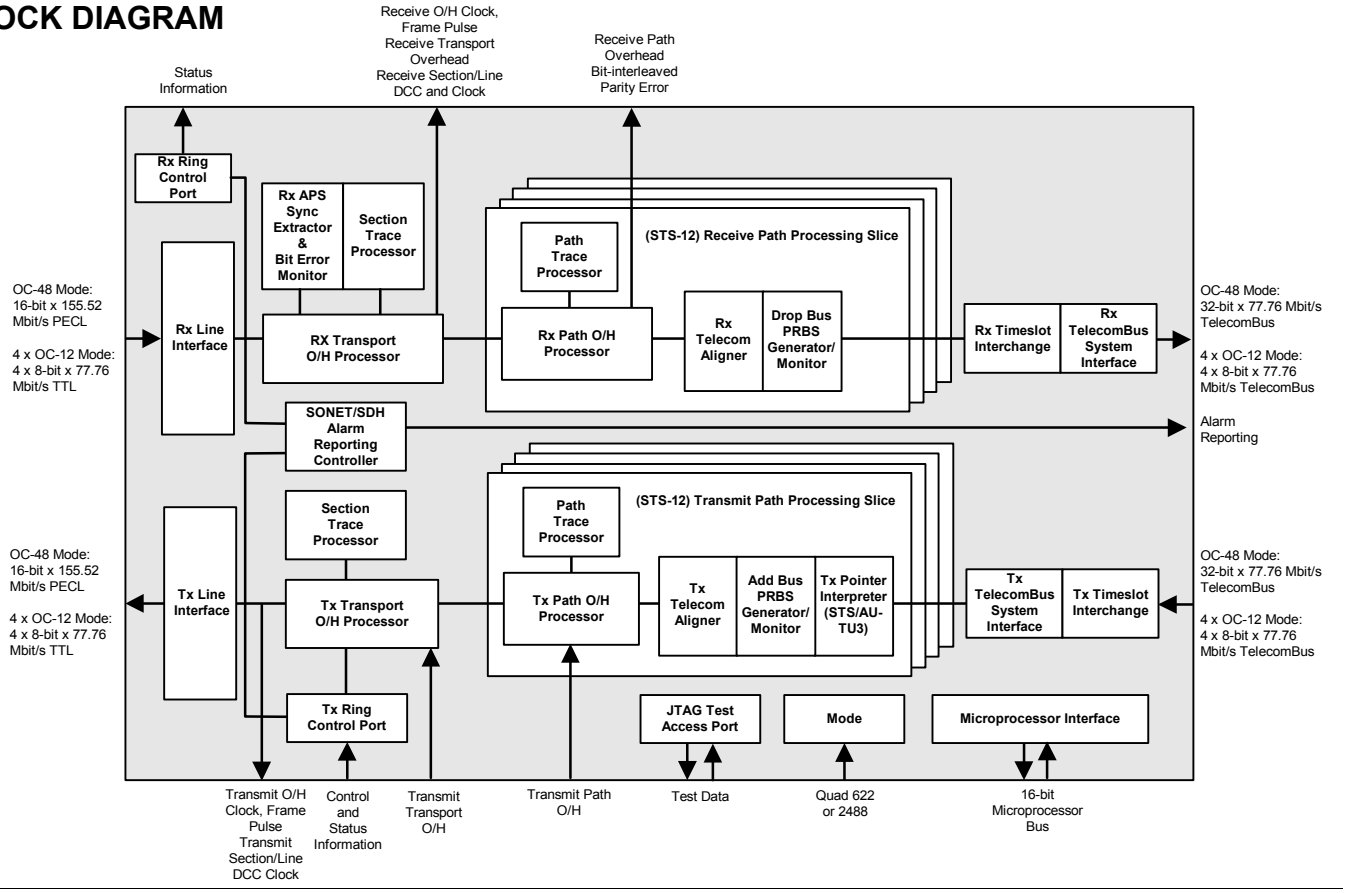
SONET/SDH Payload Extractor/Aligner for 2488 Mbit/s

FEATURES

- Monolithic SONET/SDH Payload Extractor/Aligner for use in interface applications, operating at serial interface speeds of up to 2488 Mbit/s:
  - single STS-48c (STM-16/AU4-16c);
  - single STS-48 (STM-16/AU4-4c/AU4/AU3/TU3);
  - quad STS-12c (STM-4/AU4-4c);
  - quad STS-12 (STM-4/AU4/AU3/TU3).
- In single STS-48/STM-16 mode, supports a duplex 16-bit 155.52 MHz differential PECL line side interface for direct connection to external clock recovery, clock synthesis and serializer-deserializer components.
- In quad STS-12/STM-4 mode, supports four duplex 8-bit 77.76 MHz TTL compatible line side interfaces for direct connection to external clock recovery, clock synthesis and serializer-deserializer components.
- Provides termination for SONET Section, Line and Path overhead or SDH Regenerator Section, Multiplexer Section and High Order Path overhead.
- In single STS-48/STM-16 mode provides a 32-bit 77.76 MHz ADD and DROP TelecomBus.
- In quad STS-12/STM-4 mode provides four 8-bit 77.76 MHz ADD and DROP TelecomBus Interfaces.
- Maps SONET/SDH payloads to system timing, accommodating plesiochronous timing offsets between the line and system timing references, through pointer processing.
- The entire SONET/SDH transport and path overheads are extracted to and inserted from dedicated pins.
- Frames to the SONET/SDH receive stream and inserts framing bytes and STS identification into the transmit stream and processes or inserts the transport overhead.
- Interprets or generates the STS (AU) pointer bytes (H1, H2, H3), extracts or inserts the synchronous payload envelope(s) and processes or inserts the path overhead.
- Provides Time Slot Interchange (TSI) function at the ADD and DROP TelecomBus Interfaces for grooming any legal mix of SONET/SDH paths.
- Supports Automatic Protection Switching (APS):
  - Ring control port communication of path REI and path RDI alarms;
  - Filters the APS channel (K1,K2) bytes into internal registers; inserts the APS channel into the transmit stream.
- Supports line loopback from the line side receive stream to the transmit stream and diagnostic loopback from an ADD TelecomBus interface to a DROP TelecomBus interface.
- Provides a standard five signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.

BLOCK DIAGRAM



SONET/SDH Payload Extractor/Aligner for 2488 Mbit/s

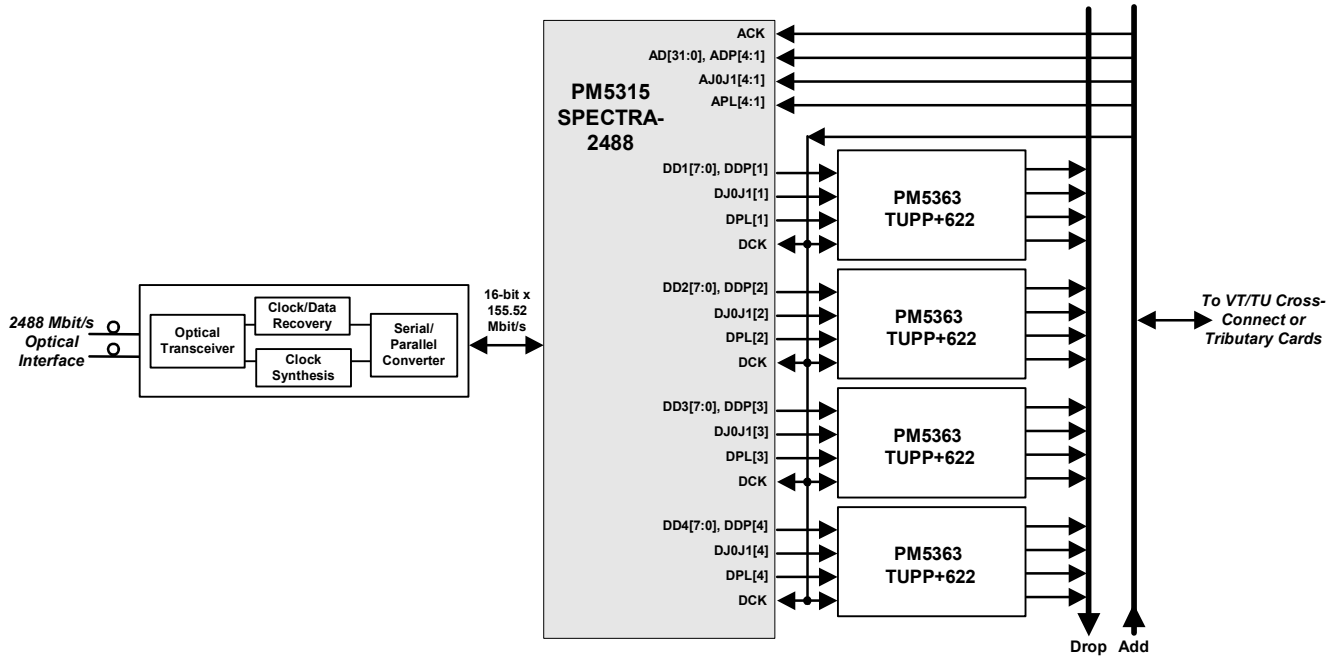
- Provides a generic 16-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power 1.8 V CMOS core logic with 3.3 V CMOS/TTL compatible digital inputs and digital outputs. PECL inputs and outputs are 3.3 V compatible.
- Industrial temperature range (-40°C to +85°C).
- 520 pin Super BGA package.

APPLICATIONS

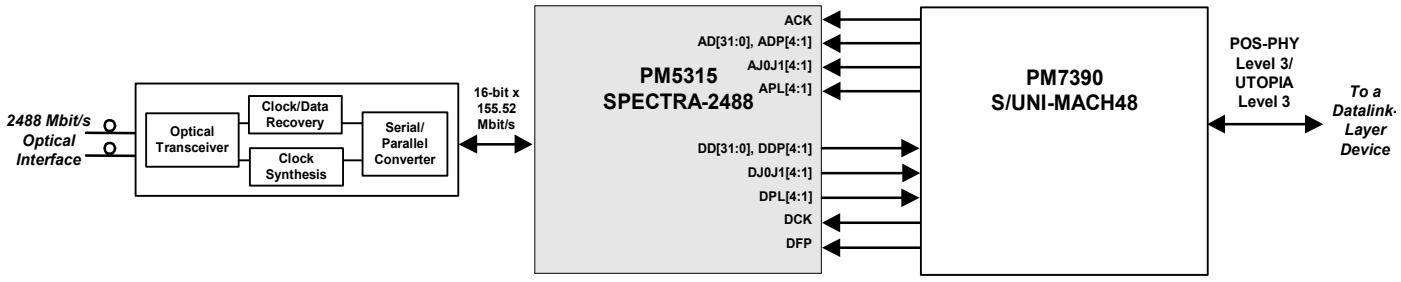
- Channelized STS-48/STM-16 or 4 x STS-12/STM-4 Interfaces for:
  - Optical Cross Connects;
  - Digital Cross Connects;
  - Router and Switch Line Cards;
  - ADM Aggregate Cards for TDM and Multiservice applications;
  - Terminal Multiplexers.

TYPICAL APPLICATIONS

STS-48/STM-16 APPLICATION WITH VT/TU POINTER PROCESSING/ALIGNMENT



STS-48/STM-16 APPLICATION WITH POS/ATM PROCESSING



Head Office:
PMC-Sierra, Inc.
#105 - 8555 Baxter Place
Burnaby, B.C. V5A 4V7
Canada
Tel: 604.415.6000
Fax: 604.415.6200

To order documentation, send email to: document@pmc-sierra.com or contact the head office, Attn: Document Coordinator

All product documentation is available on our web site at: http://www.pmc-sierra.com For corporate information, send email to: info@pmc-sierra.com

PMC-2000326 (p1)

March 2000