



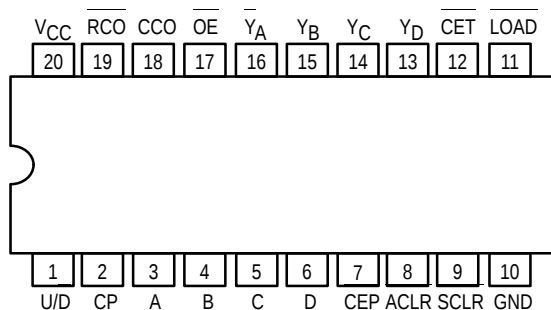
FOUR-BIT UP/DOWN COUNTER WITH THREE-STATE OUTPUTS

The SN54/74LS569A is designed as programmable up/down BCD and Binary counters respectively. These devices have 3-state outputs for use in bus organized systems. With the exception of output enable (OE) and asynchronous clear (ACLR), all functions occur on the positive edge of the clock pulse (CP).

When the LOAD input is LOW, the outputs will be programmed by the parallel data inputs (A, B, C, D) on the next clock edge. Enabling of the counters occurs only when CEP and CET are LOW and LOAD is HIGH. Direction of the count is controlled by the up-down input (U/D), HIGH counts up and LOW counts down. High-speed counting and cascading is implemented by internal look-ahead carry logic and an active LOW ripple carry output (RCO). On the LS569A, the RCO is LOW at binary 15 during up-count and during down-count it is also LOW at binary 0. During normal cascading operation RCO connected to the succeeding block at CET is the only requisite. When counting and when RCO is LOW, the clocked carry output (CCO) provides a HIGH-LOW-HIGH pulse for a duration equal to the LOW time of the clock pulse. Two active LOW reset lines are provided, a master reset asynchronous clear (ACLR) and a synchronous clear (SCLR). When in a HIGH state, the output control (OE) input forces the counter output into a HIGH impedance state and when LOW, the counter outputs are enabled.

- ESD > 3500 Volts

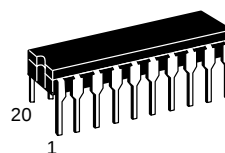
CONNECTION DIAGRAM (TOP VIEW)



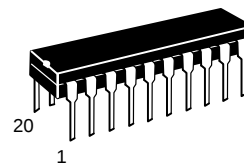
SN54/74LS569A

FOUR-BIT UP/DOWN COUNTER WITH THREE-STATE OUTPUTS

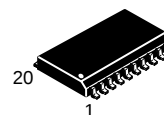
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXDW SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High Except RCO, CCO	54 74			-1.0 -2.6	mA
I _{OH}	Output Current — High RCO, CCO	54, 74			-0.44	mA
I _{OL}	Output Current — Low Except RCO, CCO	54 74			12 24	mA
I _{OL}	Output Current — Low, RCO, CCO	54 74			4.0 8.0	mA

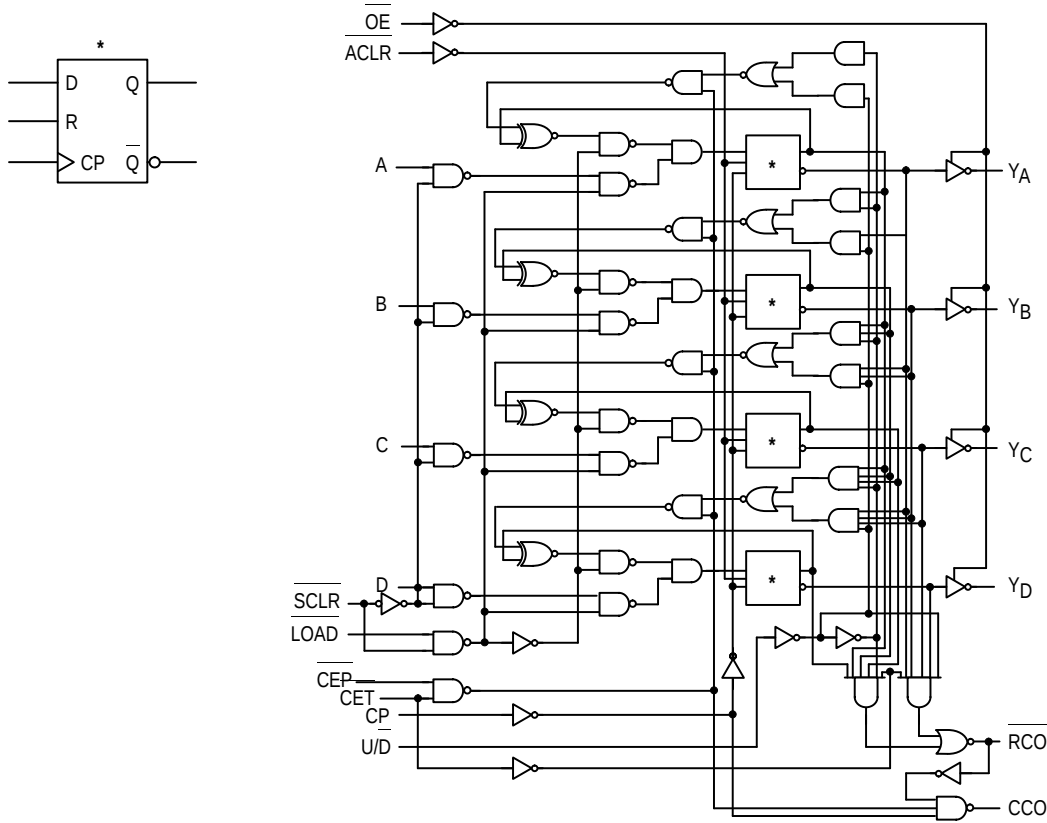
SN54/74LS569A

FUNCTION TABLE

INPUTS											OUTPUTS							
CP	D	C	B	A	LOAD	CET	CEP	U/D	ACLR	SCLR	OE	RCO	CCO	Y _D	Y _C	Y _B		Y _A
↑	X	X	X	X	H	L	L	H	H	H	L	A/R	A/R	(Q _T − CP) + 1				Count Up
↑	X	X	X	X	H	L	L	L	H	H	L	A/R	A/R	(Q _T − CP) − 1				Count Down
↑	X	X	X	X	H	H	X	X	H	H	L	H	H	NC	NC	NC	NC	Count Inhibit
↑	X	X	X	X	H	L	H	X	H	H	L	A/R	H	NC	NC	NC	NC	Count Inhibit
Ω	X	X	X	X	X	L	L	H	H	H	L	L	⌊	H	H	H	H	Overflow
↑	X	X	X	X	X	L	H	H	H	H	L	L	H	H	H	H	H	Overflow
↑	X	X	X	X	X	H	X	H	H	H	L	H	H	H	H	H	H	Overflow Inhibit
⌊	X	X	X	X	X	L	L	L	H	H	L	L	⌊	L	L	L	L	Underflow
↑	X	X	X	X	X	L	H	L	H	H	L	L	H	L	L	L	L	Underflow
↑	X	X	X	X	X	H	X	L	H	H	L	H	H	L	L	L	L	Underflow Inhibit
↑	L	H	L	H	L	X	X	X	H	H	L	H	H	L	H	L	H	Load Example
↑	X	X	X	X	X	H	X	H	H	L	L	H	H	L	L	L	L	Clear (Synchronous)
⌊	X	X	X	X	X	L	L	L	H	L	L	L	⌊	L	L	L	L	Clear (Synchronous)
↑	X	X	X	X	X	L	H	L	H	L	L	L	H	L	L	L	L	Clear (Synchronous)
↑	X	X	X	X	X	H	X	L	H	L	L	H	H	L	L	L	L	Clear (Synchronous)
X	X	X	X	X	X	X	X	H	L	X	L	H	H	L	L	L	L	Asynchronous Clear
⌊	X	X	X	X	X	L	L	L	L	X	L	L	⌊	L	L	L	L	Asynchronous Clear
X	X	X	X	X	X	L	H	L	L	X	L	L	H	L	L	L	L	Asynchronous Clear
X	X	X	X	X	X	H	X	L	L	X	L	H	H	L	L	L	L	Asynchronous Clear
X	X	X	X	X	X	X	X	X	X	X	H	X	X	Hi-Z				Output Disabled

(Q_T — CP) = Output state prior to clock edge
A/R = Assumes required output state;
NC = No change
High except during Overflow and Underflow
X = Don't care

LOGIC DIAGRAM

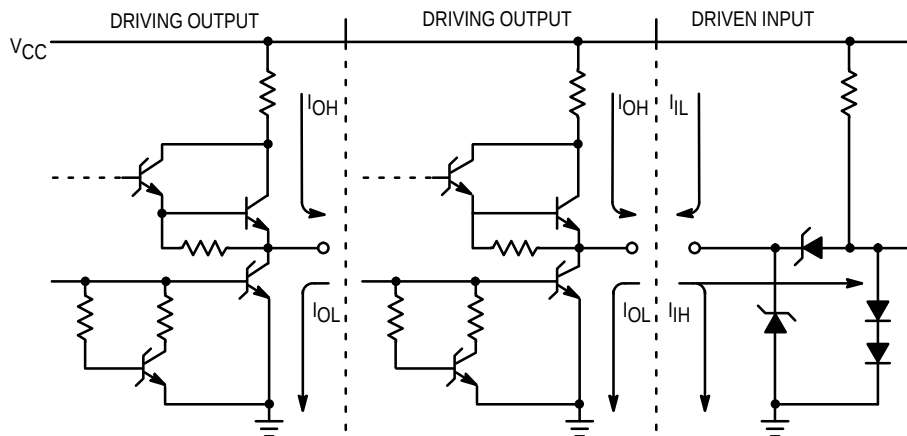


SN54/74LS569A

DEFINITION OF FUNCTIONAL TERMS

A, B, C, D	The four programmable data inputs.	$\overline{\text{ACLR}}$	Asynchronous Clear. <u>Master</u> reset of counters to zero when ACLR is LOW, independent of the clock.
$\overline{\text{CEP}}$	Count Enable Parallel. Can be used to enable and inhibit <u>counting</u> in high speed cascaded operation. CEP must be LOW to count.	$\overline{\text{SCLR}}$	Synchronous clear of <u>counters</u> to zero on the next clock edge when SCLR is LOW.
$\overline{\text{CET}}$	Count Enable Trickle. Enables the ripple carry output for cascaded operation. Must be LOW to count.	$\overline{\text{OE}}$	A HIGH on the output control sets the four counter outputs in the high impedance, and a LOW, enables the output.
CP	Clock Pulse. All synchronous functions occur on the LOW-to-HIGH transition of the clock.	$\text{Y}_A, \text{Y}_B, \text{Y}_C, \text{Y}_D$	The four counter outputs.
$\overline{\text{LOAD}}$	Enables parallel load of counter outputs from data inputs on the next clock edge. Must be HIGH to count.	$\overline{\text{RCO}}$	Ripple Carry Output. Output will be LOW on the <u>maximum count</u> on up-count. Upon down-count, RCO is LOW at 0000.
$\overline{\text{U/D}}$	Up/Down Count Control. HIGH counts up and LOW counts down.	CCO	<u>Clock</u> Carry Output. While counting and RCO is LOW, CCO will follow the clock HIGH-LOW-HIGH transition.

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown

SN54/74LS569A

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions		
			Min	Typ	Max				
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs		
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs		
		74			0.8				
V _{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V _{CC} = MIN, I _{IN} = −18 mA		
V _{OH}	Output HIGH Voltage	YA–YD	54	2.4	3.4		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
			74	2.4	3.1		V		
		RCO, CCO	54	2.5	3.5		V		
			74	2.7	3.5		V		
V _{OL}	Output LOW Voltage		54, 74		0.25	0.4	V	I _{OL} = I _{OL} MAX	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
			74		0.35	0.5	V		
I _{OZH}	Output Off Current HIGH				20	μA	V _{CC} = MAX, V _O = 2.7 V		
I _{OZL}	Output Off Current LOW				−20	μA	V _{CC} = MAX, V _O = 0.4 V		
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V		
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V		
I _{IL}	Input LOW Current	Others			−0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V		
		CET			−0.8	mA			
I _{OS}	Short Circuit Current (Note 1)	RCO, CCO	−20		−100	mA	V _{CC} = MAX		
		Others	−30		−130	mA			
I _{CC}	Power Supply Current, 3-State				43	mA	V _{CC} = MAX		

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		

t _{MAX}	Maximum Toggle Frequency	35			MHz	V _{CC} = 5.0 V C _L = 45 pF R _L = 667 Ω
t _{PLH} t _{PHL}	Propagation Delay Clock to Q			15 20	ns	
t _{PLH} t _{PHL}	Propagation Delay CET to RCO			14 15	ns	
t _{PLH} t _{PHL}	Propagation Delay U/D to RCO			20 24	ns	
t _{PLH} t _{PHL}	Propagation Delay Clock to RCO			20 25	ns	
t _{PLH} t _{PHL}	Propagation Delay CET to CCO			16 28	ns	
t _{PLH} t _{PHL}	Propagation Delay CEP to CCO			16 26	ns	
t _{PLH} t _{PHL}	Propagation Delay Clock to CCO			15 17	ns	
t _{PLH} t _{PHL}	Propagation Delay ACLR to Q			22 32	ns	
t _{PZH} t _{PZL}	Output Enable Time			15 20	ns	
t _{PHZ} t _{PLZ}	Output Disable Time			20 27	ns	C _L = 5.0 pF

SN54/74LS569A

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _W	Clock Pulse Width (Low)	20			ns	V _{CC} = 5.0 V
t _S	Setup Time, A, B, C, D	20			ns	
t _S	Setup Time, SCLR	20			ns	
t _S	Setup Time, LOAD	25			ns	
t _S	Setup Time, U/D	30			ns	
t _S	Setup Time, CET, CEP	20			ns	
t _H	Hold Time, Any Inputs	0			ns	
t _{rec}	ACLR	15			ns	

MICROPROGRAMMABLE DUAL-EVENT 8-BIT COUNTERS

