19-2062; Rev 0; 5/01

MAXIM

2.5Gbps, +3.3V Clock and Data Retiming ICs with Vertical Threshold Adjust

General Description

The MAX3877/MAX3878 are compact, low-power clock recovery and data retiming ICs for 2.488Gbps SONET/SDH applications. The fully integrated phase-locked loop (PLL) recovers a synchronous clock signal from the serial NRZ data input, which is retimed by the recovered clock. An additional 2.488Gbps serial input is available for system loopback diagnostic testing, or this input can be connected to a 155MHz reference clock to maintain a valid clock output in the absence of data transitions. The MAX3877/MAX3878 provide vertical threshold and phase-adjust control to optimize system BER in DWDM applications.

These devices provide both loss-of-lock ($\overline{LOL}$) and loss-of-signal (LOS) monitors. Differential CML outputs are provided for both clock and data signals on the MAX3877, and differential PECL outputs are provided for clock and data signals on the MAX3878.

The MAX3877/MAX3878 are designed for both section-regenerator and terminal-receiver applications in OC-48/STM-16 transmission systems. Their jitter performance exceeds all of the SONET/SDH specifications. These devices operate from a single +3.0V to +3.6V supply over a -40°C to +85°C temperature range. Typical power consumption is only 540mW with a +3.3V supply (MAX3878). They are available in a 32-pin TQFP-EP package with an exposed pad, as well as in die form.

Applications

Long Haul and Metro Systems with Optical Amplification

DWDM Transmission Systems

SONET/SDH Receivers and Regenerators

Add/Drop Multiplexers

Digital Cross-Connects

SONET/SDH Test Equipment

Typical Operating Circuit appears at end of data sheet.

Features

- ♦ **Exceeds ANSI, ITU, and Bellcore SONET/SDH Specifications**
- ♦ **Adjustable Input Threshold (±180mV)**
- ♦ **10mVp-p to 1.2Vp-p Differential Input Range**
- ♦ **540mW Power Dissipation (at +3.3V)**
- ♦ **Fully Integrated Clock Recovery and Data Retiming**
- ♦ **Optional Holdover Capability (Using External Reference Clock)**
- ♦ **0.003UI$_{RMS}$ Clock Jitter Generation**
- ♦ **Tolerates >2000 Consecutive Identical Digits**
- ♦ **Additional 2.488Gbps Input for Diagnostic Loopback Testing**
- ♦ **Differential PECL or CML Data and Clock Outputs**
- ♦ **Loss-of-Signal Indicator**
- ♦ **Loss-of-Lock Indicator**

Ordering Information

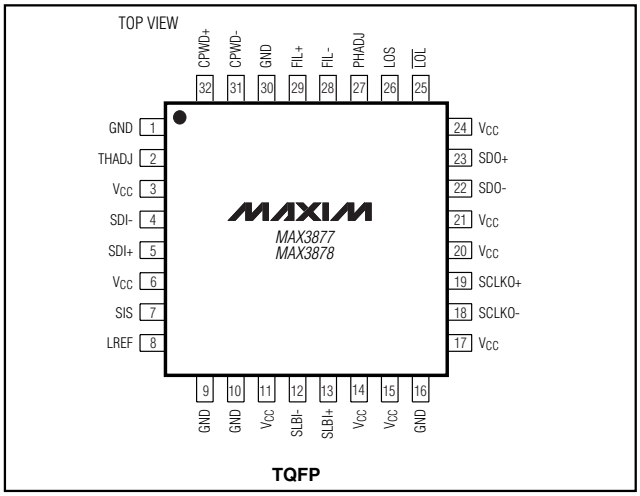
PART	TEMP. RANGE	PIN-PACKAGE
MAX3877EHJ	-40°C to +85°C	32 TQFP-EP*
MAX3877E/D***	-40°C to +85°C	DICE**
MAX3878EHJ	-40°C to +85°C	32 TQFP-EP*
MAX3878E/D***	-40°C to +85°C	DICE**

** Exposed pad*

*** Dice are designed to operate over this range, but are tested and guaranteed at T_A = +25°C only. contact factory for availability.*

**** Future product—contact factory for availability.*

Pin Configuration



2.5Gbps, +3.3V Clock and Data Retiming ICs with Vertical Threshold Adjust

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}.....-0.5V to +5.5V
Input Voltage Levels
(SDI+, SDI-, SLBI+, SLBI-).....(V_{CC} - 0.8V) to (V_{CC} + 0.5V)
Input Current Levels
(SDI+, SDI-, SLBI+, SLBI-).....-16mA to +10mA
PECL Output Current Levels
(SDO+, SDO-, SCLKO+, SCLKO-).....0mA to 56mA
CML Output Current Level
(SDO+, SDO-, SCLKO+, SCLKO-).....±22mA
Current into LOS, $\overline{LOL}$ .....-600µA to +4mA
Voltage at LOS, SIS, PHADJ, THADJ, CPWD+, CPWD-, $\overline{LOL}$, FIL+, FIL-, LREF.....-0.5V to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +85°C)
32-Pin TQFP-EP (derate 22.2mW/°C above +85°C) ..1444mW
Operating Temperature Range
MAX3877/MAX3878EHJ .....-40°C to +85°C
Operating Junction Temperature Range (die) ..-55°C to +150°C
Storage Temperature Range .....-65°C to +150°C
Processing Temperature (die) .....+400°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CURRENT						
Supply Current	I_{CC}	MAX3877 (Note 2)		175	262	mA
		MAX3878 (Note 2)		163	250	
INPUT SPECIFICATION (SDI±, SLBI±)						
Differential Input Voltage (SDI±)	V_{ID}	Figure 1 (Note 3)	10		1200	mVp-p
Differential System Loopback Input Voltage Range (SLBI±)	V_{ID}		50		1200	mVp-p
Single-Ended Input Voltage (SDI±, SLBI±)	V_{IS}		V_{CC} - 0.6		V_{CC} + 0.3	V
Input Termination to V_{CC} (SDI±, SLBI±)	R_{IN}			52		Ω
MAX3878 PECL OUTPUT SPECIFICATION (SDO±, SCLKO±)						
PECL Output High Voltage (SDO±, SCLKO±)		T_A = 0°C to +85°C	V_{CC} - 1.025		V_{CC} - 0.88	V
		T_A = -40°C	V_{CC} - 1.085		V_{CC} - 0.88	
PECL Output Low Voltage (SDO±, SCLKO±)		T_A = 0°C to +85°C	V_{CC} - 1.81		V_{CC} - 1.62	V
		T_A = -40°C	V_{CC} - 1.83		V_{CC} - 1.556	
MAX3877 CML OUTPUT SPECIFICATION (SDO±, SCLKO±)						
CML Differential Output Swing		R_L = 50Ω to V_{CC}	640	800	1000	mVp-p
CML Differential Output Impedance	R_O		85	100	115	Ω
CML Output Common-Mode Voltage		DC-coupling (R_L = 50Ω to V_{CC})		V_{CC} - 0.2		V

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
THRESHOLD SETTING SPECIFICATION (SDI±)						
Differential Input Voltage Range	V_{ID}	Note 4	100		600	mVp-p
Input Threshold Adjustment Range	V_{TH}	Figure 2	-180		180	mV
THADJ Voltage Range	V_{THADJ}	Figure 2	0.2		2.2	V
Threshold Control Linearity			-5		+5	%
Threshold Setting Accuracy		Figure 2	-27		+27	mV
Threshold Setting Stability		V_{TH} = ±30mV to ±80mV (Note 5, Figure 2)	-7.0		+7.0	mV
		V_{TH} = ±80mV to ±180mV (Note 5, Figure 2)	-11.5		+11.5	
Maximum Input Current (THADJ, PHADJ)		Control voltage = 0.2V to 2.2V	-10		+10	µA
TTL INPUT/OUTPUT SPECIFICATION (SIS, LREF, $\overline{LOL}$, LOS)						
TTL Input High Voltage (SIS, LREF)	V_{IH}		2.0			V
TTL Input Low Voltage (SIS, LREF)	V_{IL}				0.8	V
TTL Input Current (SIS, LREF)			-10		+10	µA
TTL Output High Voltage ($\overline{LOL}$>, LOS)	V_{OH}	I_{OH} = +40µA	2.4			V
TTL Output Low Voltage ($\overline{LOL}$>, LOS)	V_{OL}	I_{OL} = -2mA			0.4	V

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Output Clock Rate				2.488		Gbps
Clock-to-Q Delay		(Figure 4)	110		290	ps
Jitter Peaking	J_P	f ≤ 2MHz			0.1	dB
Jitter Transfer Bandwidth	J_{BW}			1.1	2.0	MHz

2.5Gbps, +3.3V Clock and Data Retiming ICs with Vertical Threshold Adjust

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Jitter Tolerance		f = 70kHz		3.18		UIp-p
		f = 100kHz (see "Jitter Tolerance" graph in *Typical Operating Characteristics*)		2.75		
		f = 1MHz	0.41	0.67		
		f = 10MHz	0.36	0.45		
Jitter Generation	J_{GEN}	Jitter bandwidth = 12kHz to 20MHz		0.003	0.006	UI_{RMS}
				0.026	0.056	UIp-p
Clock Output Edge Speed		(20% to 80%)			120	ps
Data Output Edge Speed		(20% to 80%)			120	ps
Tolerated Consecutive Identical Digits		BER ≤ 10^{-10}		2000		bits
Input Return Loss (SDI±, SLBI±)		100kHz to 2.5GHz		17		dB
		2.5GHz to 4.0GHz		14.5		
PLL Acquisition Time				14		ms
LOS Assert Time				1.65		µs
LOS Deassert Time				4.0		µs
Low-Frequency Cutoff for DC-Cancellation Loop		C_{PWD} = 0.1µF		10		kHz
HOLDOVER SPECIFICATION						
VCO Frequency Drift Rate in the Absence of Data	df/dt	C_{FIL} = 1µF		6.2		kHz/µs
PHASE ADJUST SPECIFICATION						
Minimum Phase Adjust Range		(Note 7)	-60		+60	ps
Phase Adjust Stability		(Note 8)	-8		+8	ps

Note 1: At T_A = -40°C, DC characteristics are guaranteed by design and characterization.
Note 2: Excluding PECL output termination, CML outputs open.
Note 3: Jitter specifications are guaranteed for this data input voltage range, measured by connecting THADJ to V_{CC}. Guaranteed by design and characterization.
Note 4: Jitter specifications are guaranteed when input threshold is set to ≤ 30% of the differential input swing. Measured with edge speed ≤ 150ps (Figure 3). Guaranteed by design and characterization.
Note 5: Threshold setting stability is guaranteed by design and characterization.
Note 6: AC characteristics are guaranteed by design and characterization.
Note 7: Phase adjust is disabled when PHADJ is connected to V_{CC}.
Note 8: Phase adjust stability is guaranteed over temperature and power-supply variation.

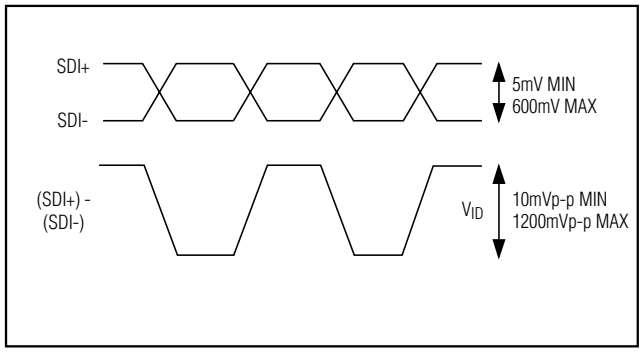


Figure 1. Input Amplitude

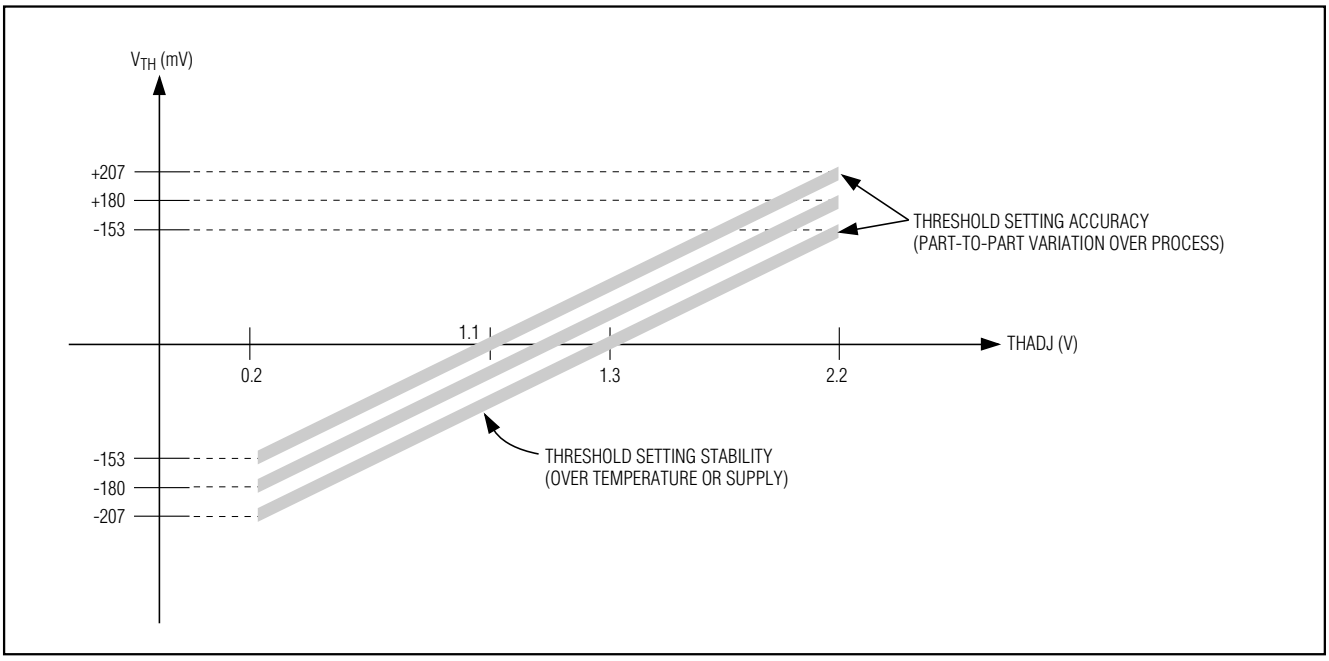


Figure 2. Setting the Input Threshold Level

2.5Gbps, +3.3V Clock and Data Retiming ICs with Vertical Threshold Adjust

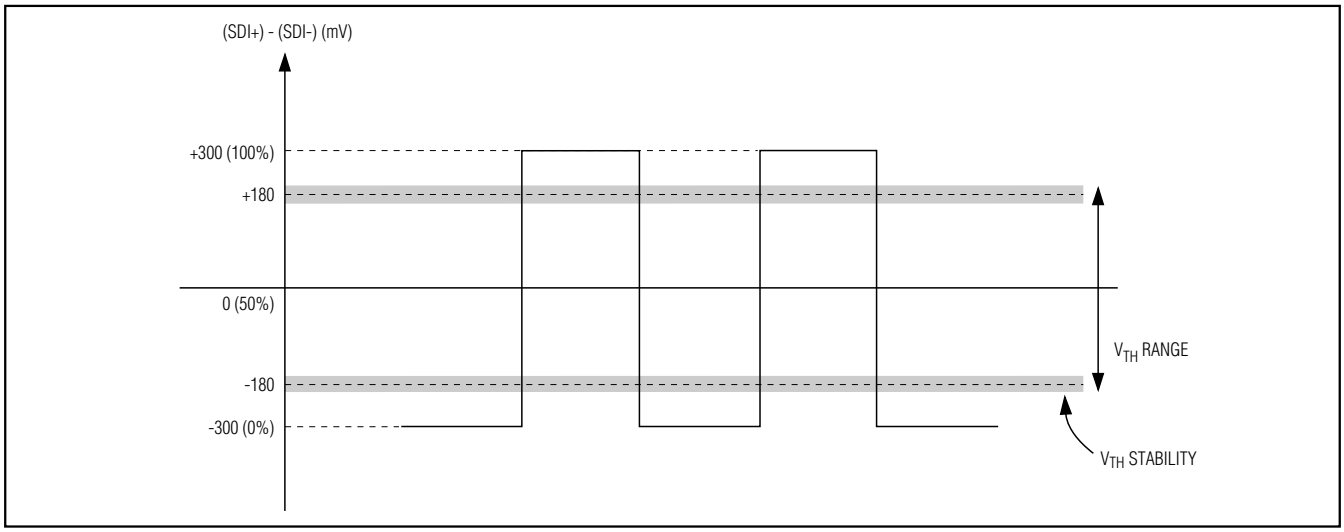


Figure 3. Definition of Input Threshold

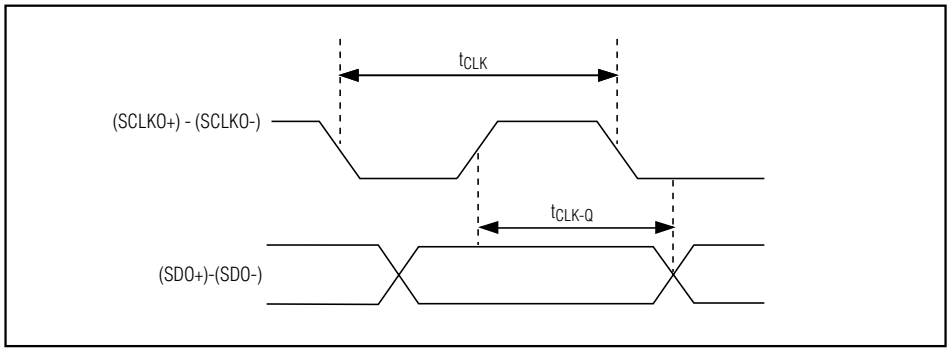
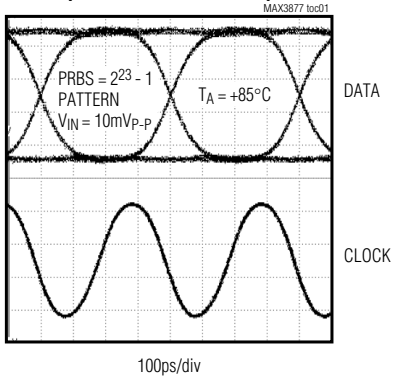


Figure 4. Output Clock-to-Q Delay

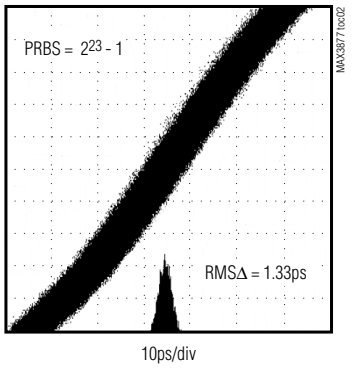
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

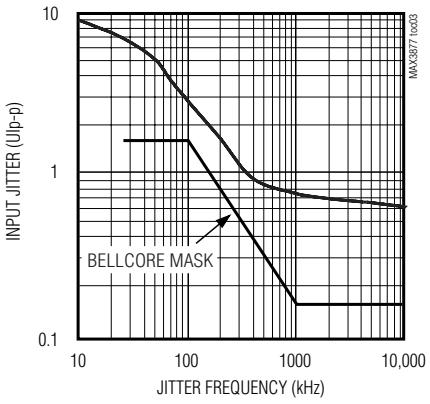
RECOVERED DATA AND CLOCK (DIFFERENTIAL OUTPUT)



RECOVERED CLOCK JITTER



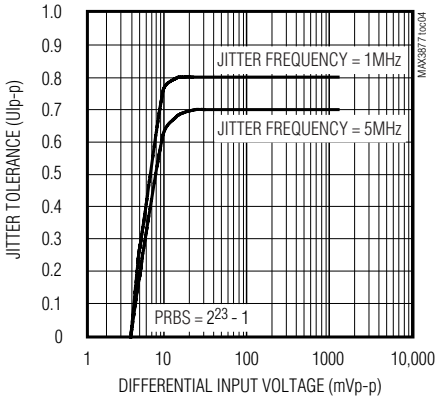
JITTER TOLERANCE



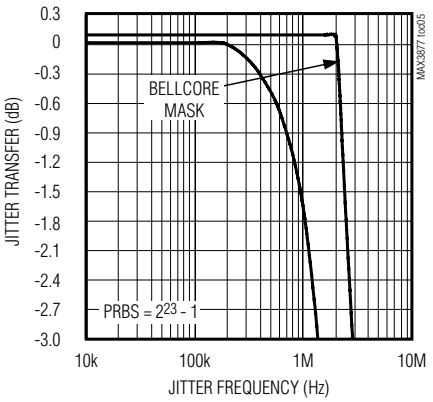
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

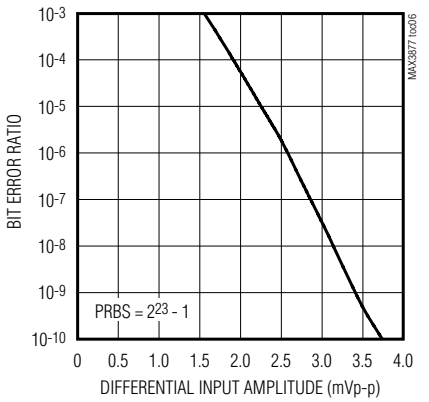
JITTER TOLERANCE vs. INPUT AMPLITUDE



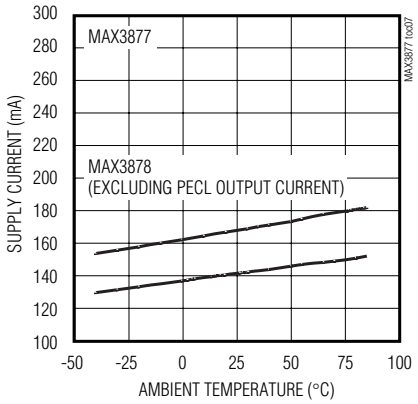
JITTER TRANSFER



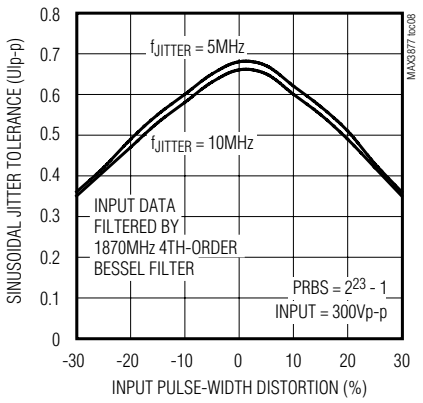
BIT ERROR RATIO vs. INPUT AMPLITUDE



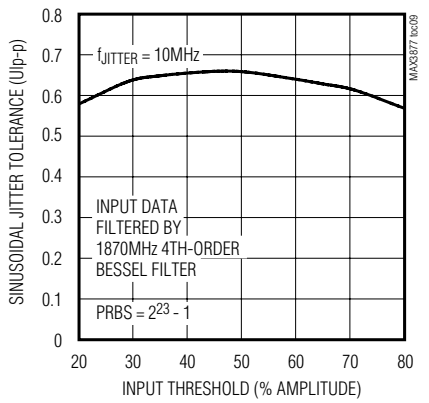
SUPPLY CURRENT vs. TEMPERATURE



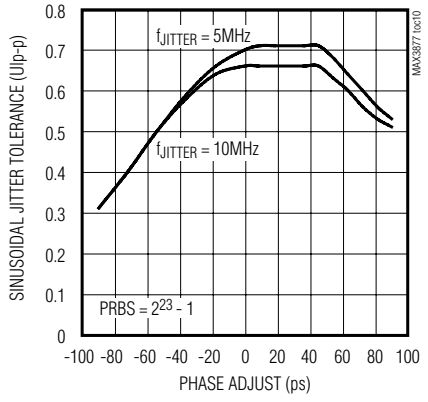
JITTER TOLERANCE vs. PULSE-WIDTH DISTORTION



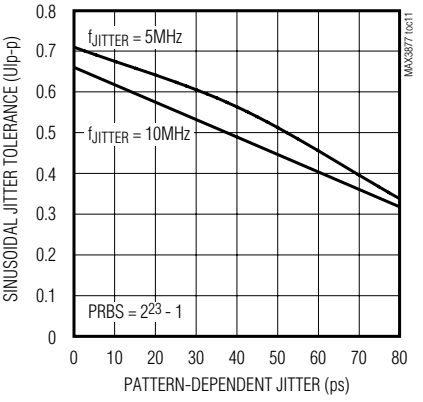
JITTER TOLERANCE vs. THRESHOLD ADJUST



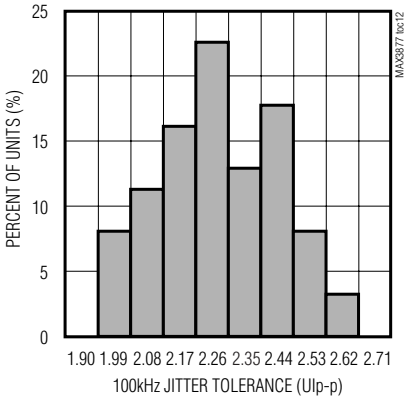
JITTER TOLERANCE vs. PHASE ADJUST



JITTER TOLERANCE vs. INPUT PATTERN-DEPENDENT JITTER



TYPICAL DISTRIBUTION OF 100kHz JITTER TOLERANCE



2.5Gbps, +3.3V Clock and Data Retiming ICs with Vertical Threshold Adjust

Pin Description

PIN	NAME	FUNCTION
1, 9, 10,16, 30	GND	Supply Ground
3, 6, 11, 14, 15, 17, 20, 21, 24	V_{CC}	Supply Voltage
2	THADJ	Threshold Control Voltage Input. Used for setting the data decision threshold. Connect to V_{CC} if not used. See Figure 7.
4	SDI-	Negative Data Input. 2.488Gbps serial data stream.
5	SDI+	Positive Data Input. 2.488Gbps serial data stream.
7	SIS	Signal Input Selection, TTL. High for system loopback input. See Table 1.
8	LREF	Lock to Reference Clock Control Signal, TTL.
12	SLBI-	Negative System Loopback or Reference Clock (in holdover mode) Input
13	SLBI+	Positive System Loopback or Reference Clock (in holdover mode) Input
18	SCLKO-	Negative Clock Output, CML (MAX3877) or PECL (MAX3878)
19	SCLKO+	Positive Clock Output, CML (MAX3877) or PECL (MAX3878)
22	SDO-	Negative Data Output, CML (MAX3877) or PECL (MAX3878)
23	SDO+	Positive Data Output, CML (MAX3877) or PECL (MAX3878)
25	$\overline{LOL}$	Loss-of-Lock Indicator, TTL Active-Low
26	LOS	Loss-of-Signal Indicator, TTL Active-High. LOS is asserted high if there are no incoming data transitions for approximately 1.65µs.
27	PHADJ	Phase-Adjust Input. Used to optimize sampling point. Connect to V_{CC} if not used. See Figure 6.
28	FIL-	Negative PLL Loop Filter Connection. Connect a 1.0µF capacitor between FIL+ and FIL-.
29	FIL+	Positive PLL Loop Filter Connection. Connect a 1.0µF capacitor between FIL+ and FIL-.
31	CPWD-	Negative Pulse-Width Distortion Cancellation Capacitor. Connect a 0.1µF capacitor between CPWD+ and CPWD-.
32	CPWD+	Positive Pulse-Width Distortion Cancellation Capacitor. Connect a 0.1µF capacitor between CPWD+ and CPWD-.

Detailed Description

The MAX3877/MAX3878 consist of a fully integrated phase-locked loop (PLL), input amplifier, data retiming block, and CML output buffer (MAX3877) or PECL output buffer (MAX3878). The PLL consists of a phase/frequency detector (PFD), a loop filter, and a voltage-controlled oscillator (VCO). Figure 5 shows the functional diagram.

This device is designed to deliver the best combination of jitter performance and power dissipation by using a fully differential signal architecture and low-noise design techniques.

SDI Input Amplifier

The SDI input amplifier accepts 2.488Gbps NRZ data with differential input swing from 10mVp-p up to 1200mVp-p. The bit error rate is better than 1×10^{-10} for input signals as small as 4mVp-p, though the jitter tolerance performance will be degraded. This amplifier allows for adjustment of the input threshold level. For interfacing with PECL signal levels, see *Applications Information*, or refer to Applications Note HFAN 1.0, *Interfacing Between CML, PECL, and LVDS.*

SLBI Input Amplifier

The SLBI input amplifier accepts either 2.488Gbps loopback data or a 155MHz reference clock. This amplifier accepts data with differential input swing from 50mVp-p up to 1200mVp-p. For interfacing with PECL signal levels, see *Applications Information.*

Phase/Frequency Detector

The phase detector incorporated in the MAX3877 and MAX3878 produces a voltage proportional to the phase difference between the incoming data and the internal clock. Because of its feedback nature, the PLL drives the error voltage to zero, aligning the recovered clock to the center of the incoming data eye for retiming.

The digital frequency detector (FD) aids frequency acquisition during startup conditions. The frequency difference between the received data and the VCO clock is derived by sampling the in-phase and quadrature VCO output on the rising edges of the data input signal. The FD drives the VCO until the frequency difference is reduced to zero. Once frequency acquisition is complete, the FD returns to a neutral state. False locking is completely eliminated by this digital frequency detector.

While in holdover mode, a Type 4 phase/frequency detector (PFD) is implemented to track the 155MHz reference clock signal. This PFD compares the incoming 155MHz reference clock with the divided down VCO clock. The LREF input is used to enable holdover mode (see *Applications Information*).

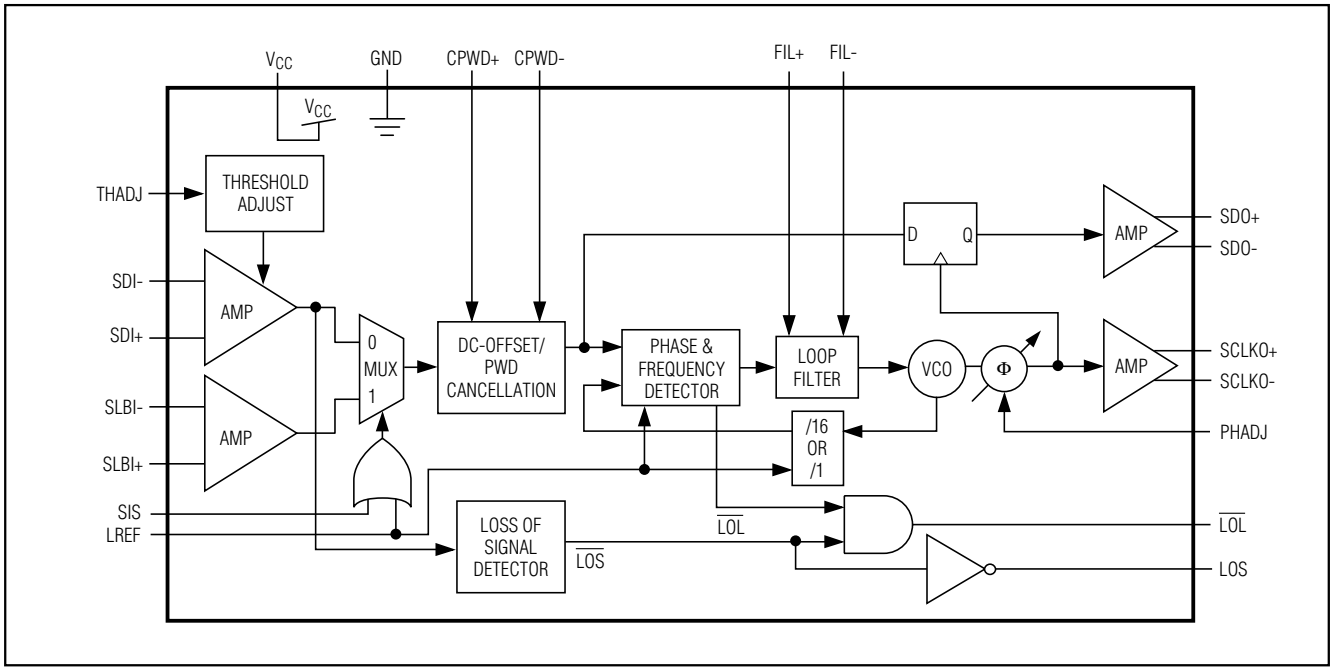


Figure 5. Functional Diagram

2.5Gbps, +3.3V Clock and Data Retiming ICs with Vertical Threshold Adjust

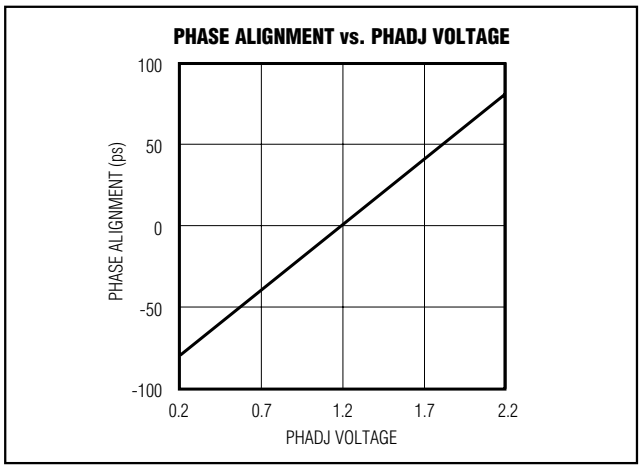


Figure 6. Phase Alignment vs. PHADJ Voltage

Phase Adjust

The internal clock is aligned to the center of the data eye. For specific applications, this sampling position can be shifted using the PHADJ input to optimize BER performance. Refer to Figure 6 for setting the voltage at PHADJ. When the phase adjust feature is not used, PHADJ should be tied directly to V_{CC}.

Loop Filter and VCO

The phase detector and frequency detector outputs are summed into the loop filter. An external capacitor, C_F, is required to set the PLL damping ratio. Refer to *Design Procedure* for guidelines on selecting this capacitor.

The loop filter output controls the on-chip LC VCO running at 2.488GHz. The VCO provides low phase noise and is trimmed to the correct frequency. Clock jitter generation is typically $1.2ps_{RMS}$ within a jitter bandwidth of 12kHz to 20MHz.

Loss-of-Lock Monitor

A loss-of-lock monitor is incorporated in the MAX3877/MAX3878 frequency detector. When the PLL is frequency locked, the internal $\overline{LOL}$ signal is high, and if the PLL is out of frequency lock, the internal $\overline{LOL}$ signal immediately becomes low.

Loss-of-Signal Detector

A loss of signal detector is provided to detect a loss of incoming data. If there are no transitions to the SDI data input for approximately 1.65µs, the LOS signal becomes high.

DC-Offset/Pulse-Width Distortion Cancellation Loop

The input signal is first limited in the forward signal path. The DC offset of this signal is detected and then amplified in the feedback path. C_{PWD} sets the cutoff frequency of the low pass filter. This error signal is then subtracted from the incoming data. When threshold adjust is enabled, this loop acts as a pulse-width distortion cancellation loop. Shorting the $C_{PWD}\pm$ pins together disables the DC-offset/pulse-width distortion cancellation loop.

Threshold Adjust

This analog input controls the decision threshold of the input stage. In applications where the noise density is not balanced between logical zeros and ones (i.e., optical amplification using EDFA amplifiers), it is possible to achieve lower bit-error ratios (BER) by adjusting the input threshold. Threshold adjust may be disabled by connecting THADJ to V_{CC}. The threshold level is set relative to the center of the differential input voltage swing at the input. Refer to Figures 3 and 7 for setting the voltage at THADJ.

Input Select Pins

TTL inputs SIS and LREF are provided to select between the SDI and SLBI inputs. Table 1 is a logical truth table describing the operation of SIS and LREF. In this way, the MAX3877/MAX3878 will automatically lock to the reference clock in the event of a loss-of-signal condition.

In systems where a valid clock output is required under loss-of-signal conditions, a 155MHz reference clock is applied to the SLBI inputs for holdover capabilities. This holdover mode is activated with the LREF input. LREF may be directly connected to the LOS pin or to an external system loss-of-signal monitor.

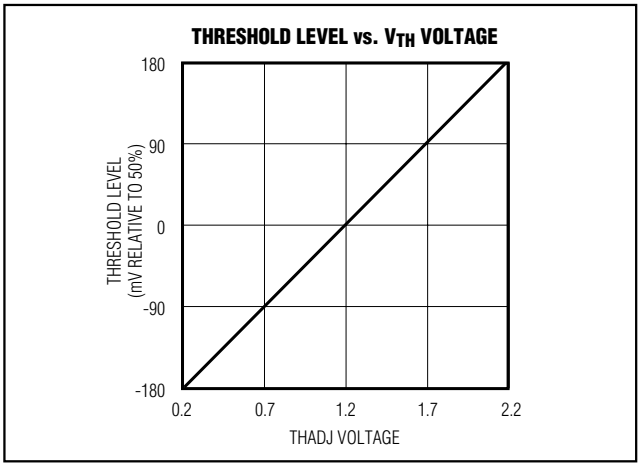


Figure 7. Threshold Level vs. THADJ Voltage

Table 1. Selecting Input Path

	SIS = 0	SIS = 1
LREF = 0	SDI (Normal Operation)	SLBI (System Loopback Mode)
LREF = 1	SLBI (Holdover Mode)	SLBI (Holdover Mode)

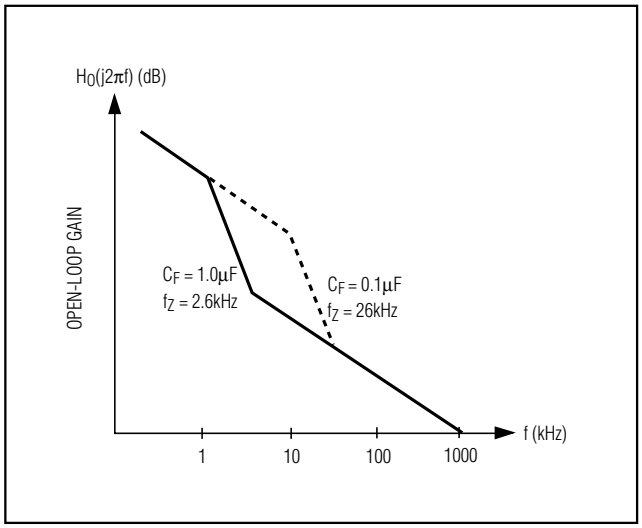


Figure 8. Open-Loop Transfer Function

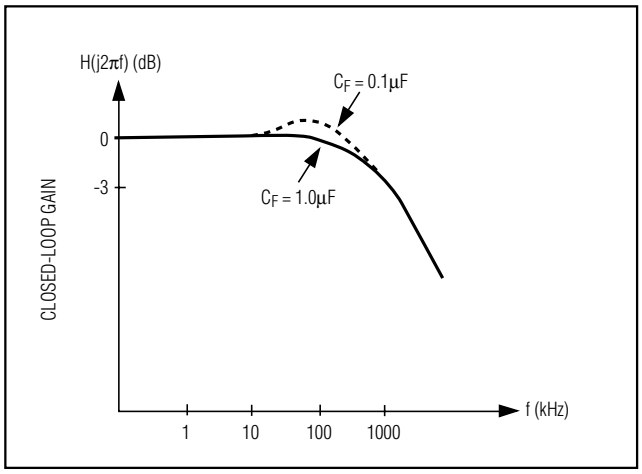


Figure 9. Closed-Loop Transfer Function

Design Procedure

Setting the Loop Filter

The MAX3877/MAX3878 are designed for both regenerator and receiver applications. The fully integrated PLL is a classic second-order feedback system, with a loop bandwidth (f_L) fixed at 1.4MHz. The external capacitor, C_F, can be adjusted to set the loop damping. Figures 8 and 9 show the open-loop and closed-loop transfer functions.

The PLL zero frequency, f_Z, is a function of external capacitor C_F, and can be approximated according to:

$$f_Z = \frac{1}{2\pi(60)C_F}$$

For an overdamped system ($f_Z / f_L < 0.25$), the jitter peaking (M_P) of a second-order system can be approximated by:

$$M_P = 20\log\left(1+\frac{f_Z}{f_L}\right)$$

For example, using C_F = 0.1µF results in a jitter peaking of 0.16dB. Reducing C_F below 0.01µF may result in PLL instability. The recommended value of C_F = 1.0µF is to guarantee a maximum jitter peaking of less than 0.1dB. C_F must be a low-TC, high-quality capacitor of type XR7 or better.

Input Termination

Inputs for the MAX3877/MAX3878 are current-mode logic (CML) compatible. The inputs all provide internal 50Ω termination to reduce the required number of external components. When interfacing to differential PECL levels, it is important to attenuate the signal while maintaining a 50Ω termination (see Figure 10). AC-coupling is also necessary to maintain the input common-mode level.

Output Termination (MAX3877)

The MAX3877 uses current-mode logic (CML) for its high-speed digital outputs. CML outputs are 50Ω back-terminated, reducing the external component count. Refer to Figure 11 for the output structure. CML outputs may be terminated by 50Ω to V_{CC}, or by 100Ω differential impedance.

Output Termination (MAX3878)

The MAX3878 uses positive emitter-coupled logic (PECL) for its high-speed outputs. PECL outputs are designed to be terminated by 50Ω to (V_{CC} - 2V). Refer to Applications Note HFAN 0.1.0, *Interfacing Between CML, PECL, and LVDS*, for more information.

2.5Gbps, +3.3V Clock and Data Retiming ICs with Vertical Threshold Adjust

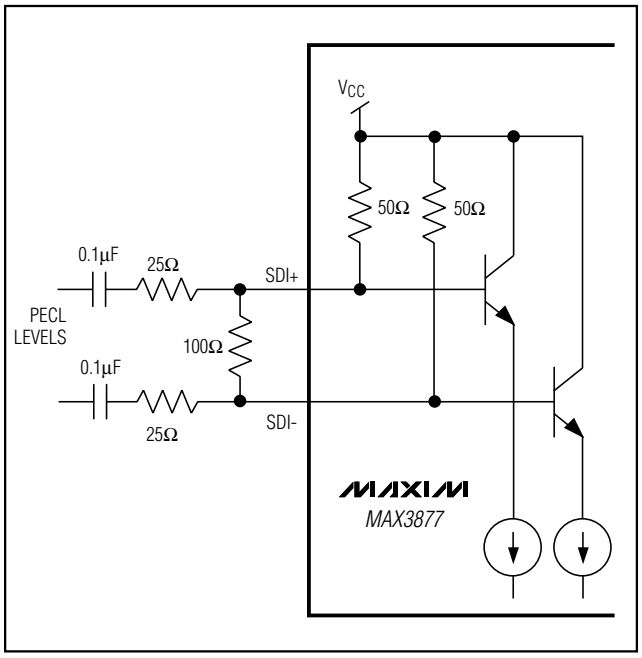


Figure 10. Interfacing with PECL Levels

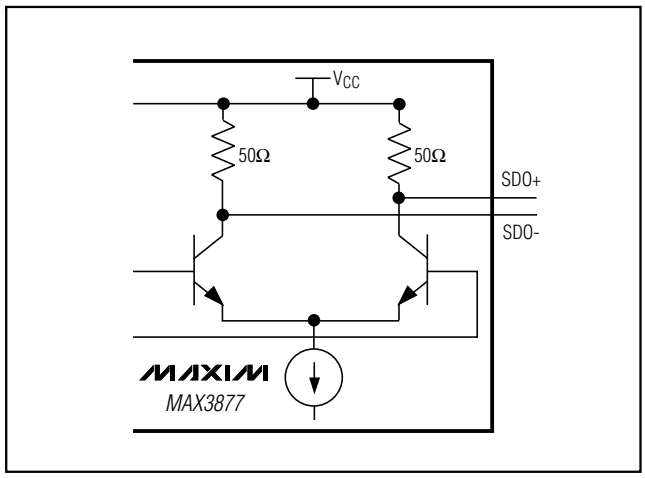


Figure 11. CML Outputs

Jitter Tolerance and Input Sensitivity Trade-Offs

When the received data amplitude is higher than 10mVp-p, the MAX3877/MAX3878 provide a typical jitter tolerance of 0.64UI at jitter frequencies greater than 10MHz. The SDH/SONET jitter tolerance specification is 0.15UI, leaving a jitter allowance of 0.49UI for receiver preamplifier and postamplifier design.

The BER is better than 1×10^{-10} for input signals greater than 4mVp-p. At 5mVp-p, jitter tolerance will be degraded, but will still be above the SDH/SONET requirement. The user can make a trade-off between jitter tolerance and input sensitivity according to the specific application. Refer to *Typical Operating Characteristics* for Jitter Tolerance and BER vs. Input Amplitude.

Applications Information

Holdover Mode

When in holdover mode, the MAX3877/MAX3878 can lock to an external reference clock to maintain a valid clock output in the absence of input data. When LREF is high, the PLL locks to an external 155.52MHz reference clock, which is applied to the SLBI inputs. To enter holdover mode automatically when there are no transitions to the SDI inputs, LOS can be directly tied to LREF. By maintaining frequency lock, the time required to reacquire lock is reduced.

System Loopback

The system loopback input may be used as an auxiliary input for system loopback testing or as input for an external 155.52MHz reference clock. When used as a loopback test, the user can connect a serializer output in a transceiver directly to the SLBI inputs for system diagnostics. Using an external reference clock can maintain PLL frequency lock in the absence of transitions on the SDI inputs.

Consecutive Identical Digits (CID)

The MAX3877/MAX3878 have low frequency drift in the absence of data transitions. As a result, long runs of consecutive zeros and ones can be tolerated while maintaining a BER better than 1×10^{-10}. The CID tolerance is tested using a 2^{13} - 1PRBS, substituting a long run of zeros to simulate the worst case. A CID tolerance of 2000 bits is typical.

The VCO frequency after 4096 bits (approximately 1.6µs) may be estimated by using the VCO drift rate:

$$f = 2.488\text{GHz} \pm \left(1.65\mu\text{s} \times \frac{6.2\text{kHz}}{\mu\text{s}}\right)$$

$$= 2.488\text{GHz} \pm 10.21\text{kHz} = 2.488\text{GHz} \pm 4.1\text{ppm}$$

Exposed Pad (EP) Package

The exposed pad, 32-pin TQFP incorporates features that provide a very low thermal-resistance path for heat removal from the IC. The pad is electrical ground on the MAX3877/MAX3878 and should be soldered to the circuit board for proper thermal and electrical performance.

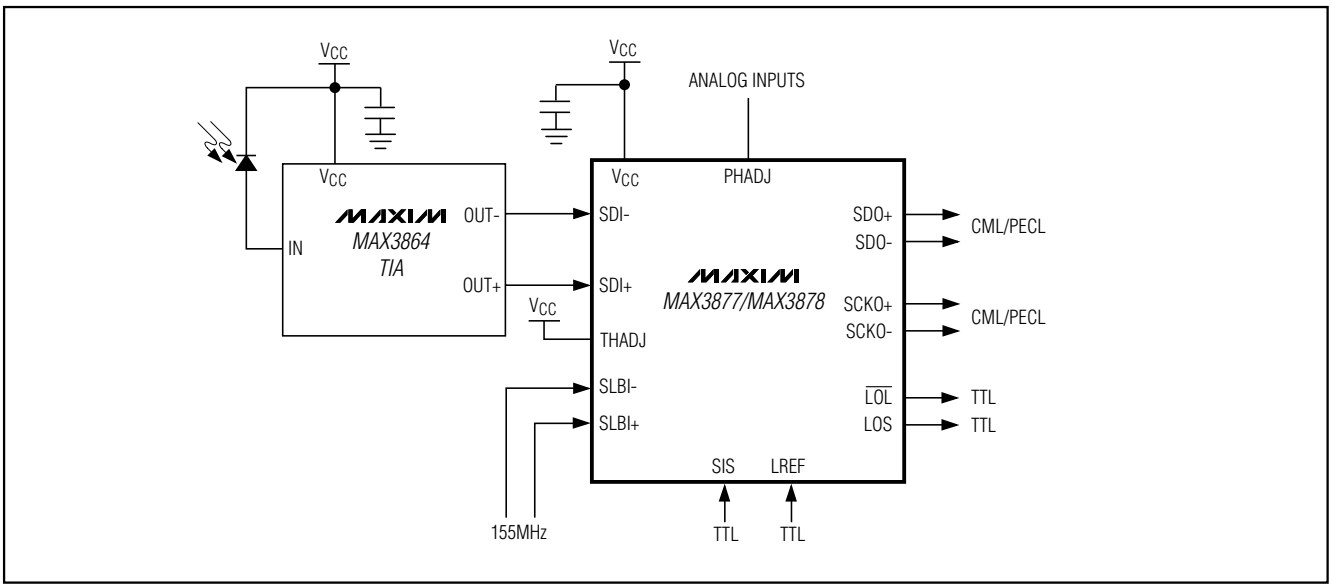


Figure 12. Typical Application Circuit (Interfacing with the MAX3864 TIA without using threshold adjust)

Layout Considerations

Performance can be significantly affected by circuit board layout and design. Use good high-frequency design techniques, including minimizing ground inductance and using fixed-impedance transmission lines on the data and clock signals. Power-supply decoupling should be placed as close to V_{CC} as possible. Take care to isolate the input from the output signals to reduce feedthrough.

Chip Information

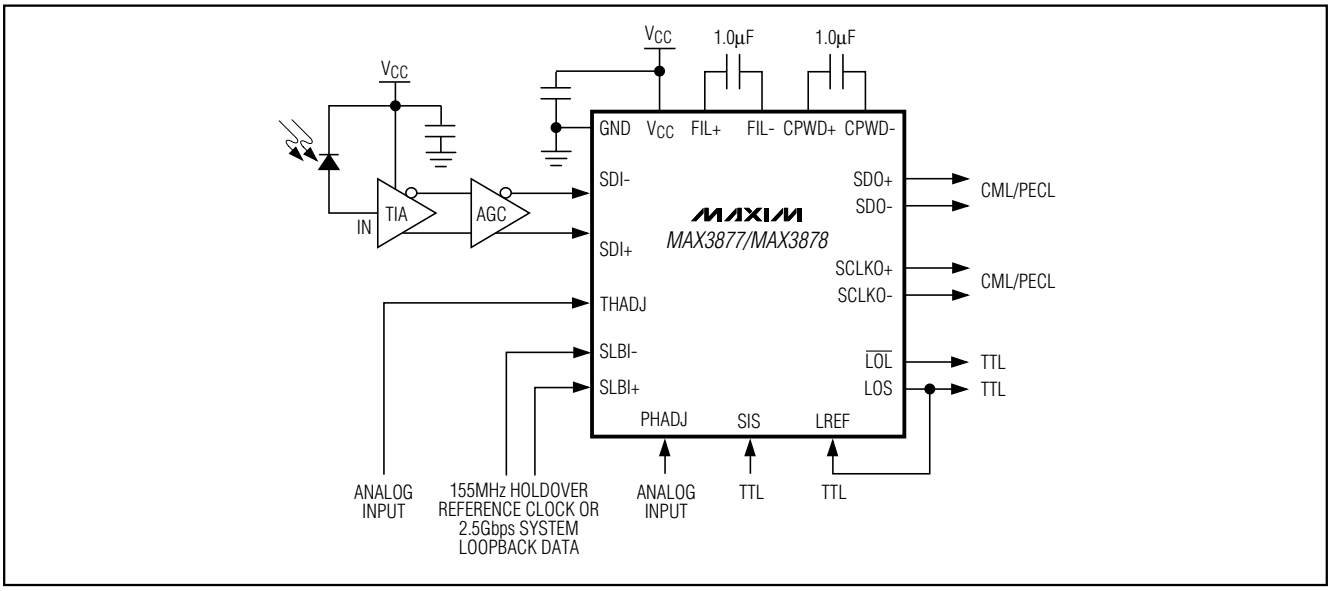
TRANSISTOR COUNT: 1561

PROCESS: BiPOLAR

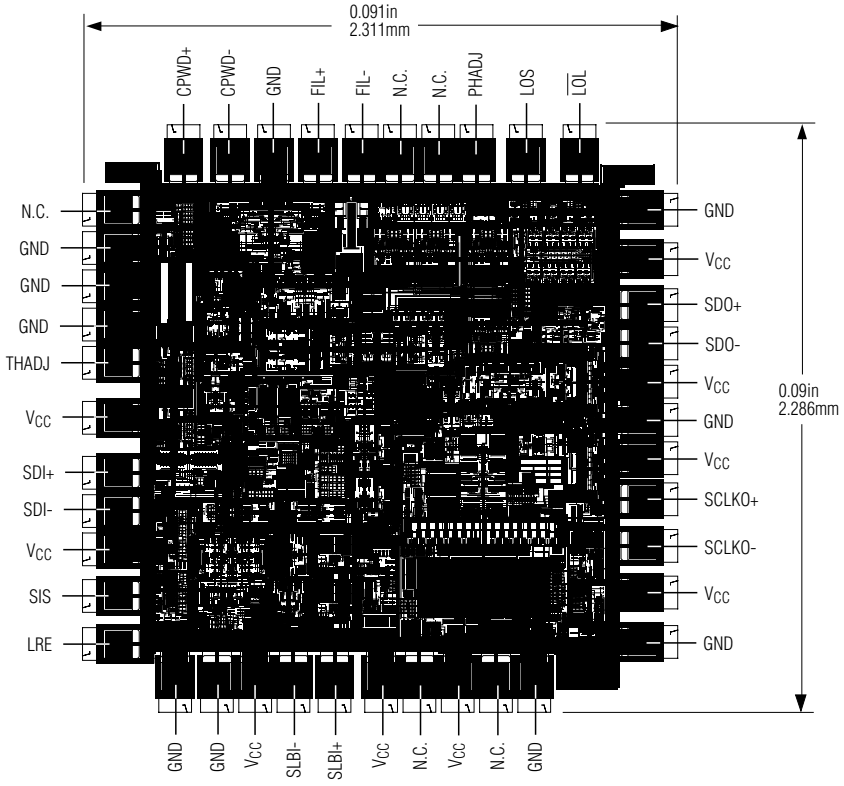
SUBSTRATE CONNECTED TO GND

2.5Gbps, +3.3V Clock and Data Retiming ICs with Vertical Threshold Adjust

Typical Application Circuit

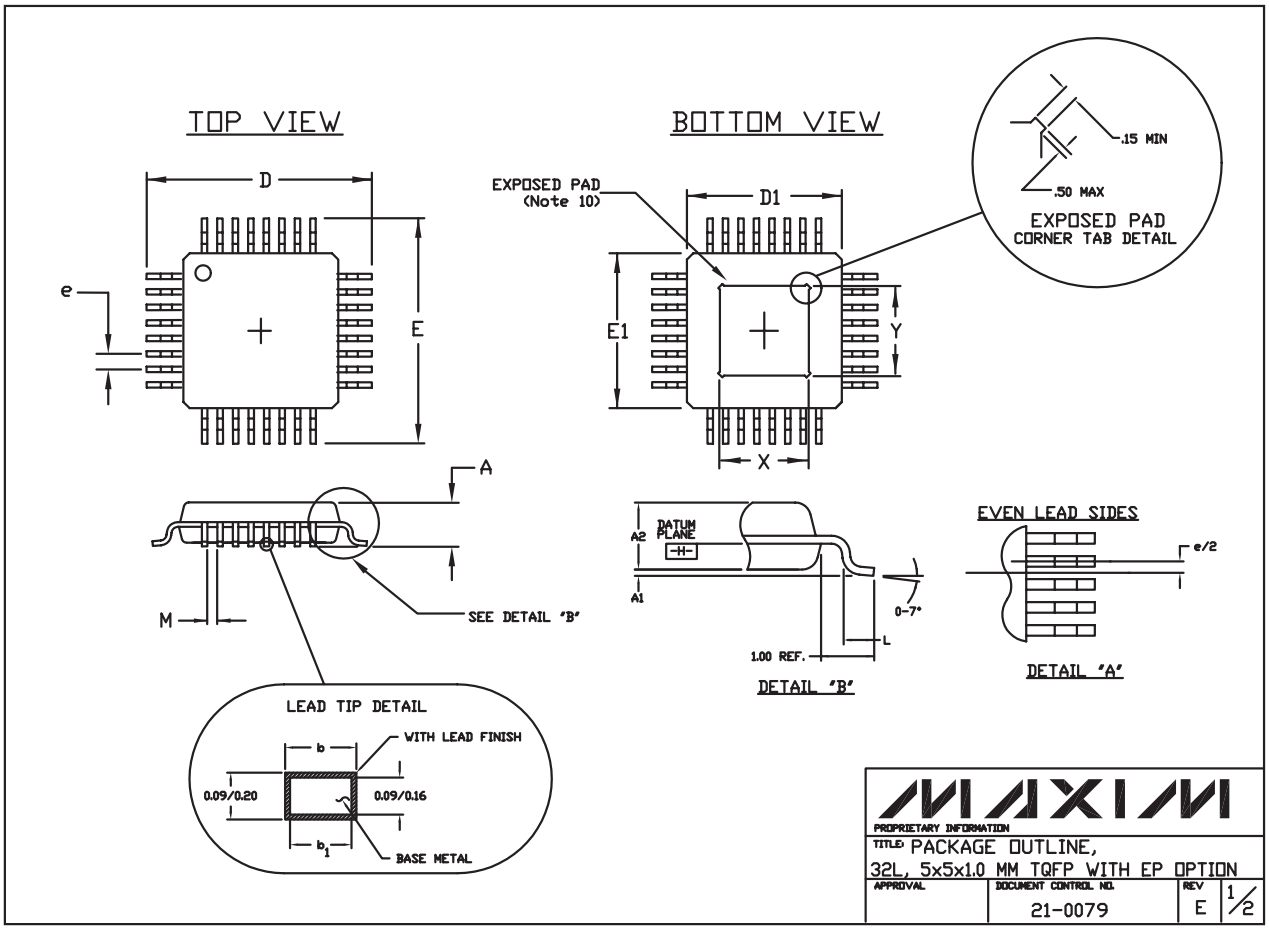


Chip Topography



Package Information

32L,TQFP.EPS



2.5Gbps, +3.3V Clock and Data Retiming ICs with Vertical Threshold Adjust

Package Information (continued)

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE ⊟H⊟ IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MO-136.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 2 MILS (.05 MM).
10. DIMENSIONS X AND Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY. SEE INDIVIDUAL PRODUCT DATASHEET TO DETERMINE IF A PRODUCT USES EXPOSED PAD PACKAGE.

	JEDEC VARIATIONS DIMENSIONS IN MILLIMETERS			
	AA		AA-EP*	
	5x5x1.0 MM		5x5x1.0 MM	
	MIN.	MAX.	MIN.	MAX.
A	~~~	1.20	~~~	1.20
A_1	0.05	0.15	0.05	0.15
A_2	0.95	1.05	0.95	1.05
D	7.00 BSC.		7.00 BSC.	
D_1	5.00 BSC.		5.00 BSC.	
E	7.00 BSC.		7.00 BSC.	
E_1	5.00 BSC.		5.00 BSC.	
L	0.45	0.75	0.45	0.75
M	0.15	~~~	0.15	~~~
N	32		32	
e	0.50 BSC.		0.50 BSC.	
b	0.17	0.27	0.17	0.27
b1	0.17	0.23	0.17	0.23
*X	N/A	N/A	2.70	3.30
*Y	N/A	N/A	2.70	3.30

* EXPOSED PAD (Note 10)

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 32L, 5x5x1.0 MM TQFP WITH EP OPTION

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0079	E	2/2