AIT2139 Video Signal Processor (VSPro)™

VGA to NTSC/PAL Encoder **Patent Pending**

General Description

The AIT2139 video signal processor converts the non-interlaced analog RGB and syncs (vertical, horizontal or composite) signal from a standard VGA source into a broadcast quality NTSC or PAL video signal. In addition to the S-Video and Composite outputs, the AIT2139 provides optional interlaced analog RGB or analog Y/P_rP_b output formats. Advanced digital signal processing and *Flic-Free*™ digital filter technology provide a clean and stable video display.

The AIT2139 is a master-mode-only video signal processor. Scan rate conversion is accomplished through an external SDRAM or EDO memory which allows the AIT2139 to accept VGA input not necessarily synchronized with TV timing. The AIT2139 accepts multi-sync inputs, supporting resolutions from 640x480 (up to 85 Hz refresh rate) to 1024x768 (60 Hz). A proprietary digital scaler fits the computer image, with borders and menu bars visible for all of the above resolutions, into an underscaned TV-Size image for both NTSC and PAL video standards. The AIT2139 also provides Zoom, Freeze, Pan, and Scroll capabilities.

The AIT2139 can be controlled from pins or via I^2C. All video processing is done in the digital domain with no tuning circuits. Oversampling techniques in the digital encoder result in very simple and inexpensive analog output filters. The output DACs generate standard video-level signals into a 50Ω load (150Ω termination at the source and 75Ω load at the video monitor).

The AIT2139 requires an absolute minimum of external components. Precision timing is derived from a 27 MHz crystal or clock reference. The AIT2139 conserves power by supporting the VESA DPMS, as well as a complete chip power-down mode. The AIT2139 is fabricated in a sub-micron CMOS process and packaged in 128-lead MQFP. Performance is guaranteed from 0°C to 70°C (T_A).

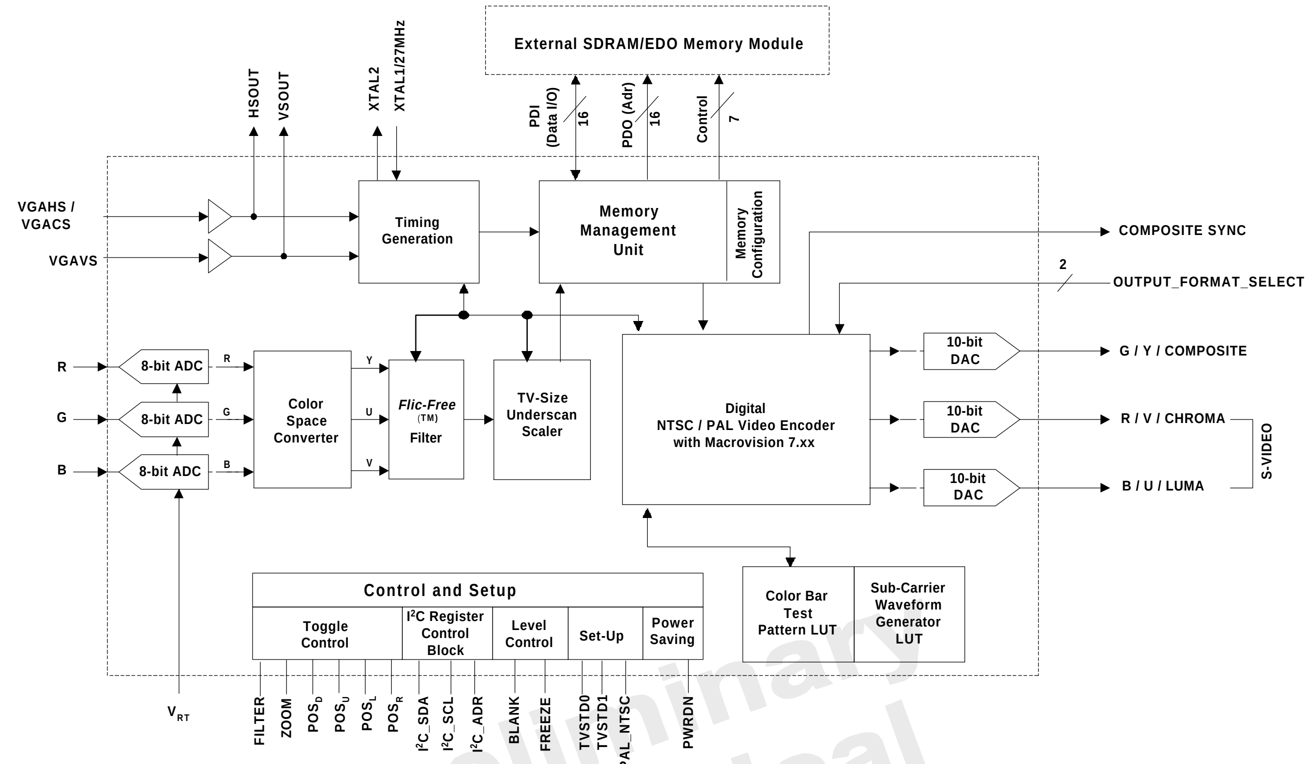
Features

- Supports Macrovision™ 7.X anti-copy protection
- Single-chip, crystal-controlled, all-digital Video Signal Processing
- Simultaneous display on Monitor, LCD and TV
- Multiple frequency input formats:
  640x480, up to 85 Hz
  800x600, up to 85 Hz
  1024x768, up to 60 Hz
- Underscan, Freeze, Zoom, Pan and Scroll
- Supports NTSC, NTSC-EIAJ, and PAL B/D/G/H/I/M/N standards
- Supports Macintosh, NEC-PC98 and PC
- Line-21 and Line-284 Closed Captioning Support
- 3-Channel 8-Bit ADC inputs for true 16.7 million color conversion
- 3-Channel 10-bit DAC outputs
- Proprietary memory compression reduces external memory size
- External EDO (256K X 16-Bit) memory interface
- External SDRAM (1M X 16-Bit) memory interface
- Fully programmable through I^2C port or hardware (pin-based) controls
- *Flic-Free*™ filter
- Selectable TV output format - Composite, S-Video, Y/P_rP_b or RGB/SCART
- Auto detect input video mode
- Auto detect the presence of the TV
- Single +5V power supply

Applications

- Computer Compatible TV
- Internet Appliances / TV / Set-top Box
- Advanced VGA to Video Scan Converter
- DVD movie playback

AIT2139 Block Diagram



Functional Description

The AIT2139 comprises all of the circuitry necessary to convert analog RGB signals from a graphic controller or RAMDAC into standard base band video signal adhering to worldwide NTSC and PAL standards.

The AIT2139 is a stand-alone VGA-to-TV video processor with user selectable RGB, Y/P_rP_b, S-Video or Composite output. The AIT2139 is a master mode only video converter. Using external SDRAM or EDO memory, the input timing and output video timing become independent. The AIT2139 has the capability to accept VGA input not necessarily synchronized with TV timing, to manipulate the image and to generate extremely accurate video output signals. The internal line cache provides anti-flicker conversion.

The AIT2139 provides additional image control such as Zoom by 2, positioning and panning. A built-in digital scaler scales down the computer image vertically and horizontally to generate an underscan TV-size display image.

The AIT2139 operates entirely in the digital domain between A/D conversion of graphic input signals and D/A conversion of Composite, S-Video, RGB or YUV output signals.

Operation

The analog VGA signal is digitized by three 8-bit A/D converters operating up to 48 MHz. The standard signal range is from 0 to 0.85V, but other values can be accommodated by varying the reference voltage.

Clocks for the input portion of the AIT2139 are generated by an internal phase-locked loop with an integral divide-by-N counter. This clock generator uses the VGA horizontal sync or composite sync as its input reference frequency. The clock generated by the PLL and counter is locked to the incoming line rate and is used to digitize a fixed number of pixels per line.

With the external SDRAM or EDO memory, the sampled data is stored and retrieved by the video signal processor. The clock for the processor portion of the AIT2139 is crystal-controlled at 27 MHz. It is generated by connecting a standard 27 MHz oscillator or crystal to an internal oscillator circuit. As a result of de-coupling the input and output, the stable time-base ensures adherence to the television standards.

Input A/D conversion

Eight-bit A/D converters are used on each of the red, green, and blue input video signals at up to 48MHz sampling rate. HSYNC and VSYNC are buffered by Schmitt trigger gates. Typical RGB signal range is from 0 to 0.85V. A different reference voltage can be applied to V_{RT} in order to override the internal reference to accommodate different input signal ranges. This externally supplied reference voltage should be higher or equal to the maximum RGB signal range.

Converting from RGB to Components

Digital video processing within the AIT2139 is done with common YUV color components. The output of the RGB-to-YUV matrix operates in 24-bit with the YUV data decimated to 4:2:2 format.

Flicker Filtering

A finite impulse response digital filter is used to reduce flicker due to single line elements of the graphic input image and the interlaced structure of NTSC and PAL video. This is constructed using proprietary AITech algorithms.

Scan Conversion Operation

Video scan-rate and timing are generated by the control logic based on the input VGA-compatible graphic signal.

The AIT2139 front end comprises all the circuitry in the signal path from the A/D converters to the vertical filter network. All front-end circuits operate at the phase-locked clock frequency. This means that digital video pixels (16-bits of YUV 4:2:2) are written into the external FIFO or SDRAM or EDO memory at the same rate as the pixel clock frequency.

Master Mode

In master-mode operation, the processor internally generates all the timing and sync signals, and provides the Horizontal Sync, Vertical Sync, and an internal Pixel Data Clock to the external memory devices. The processor is capable of accepting the multi-sync inputs in the master mode operation. The processor provides a clock and an odd/even signal to the FIFO or the external memory devices. The VGA data read-in time is not necessary to be synchronized with the write-out time to the processor. Depending on the memory configuration, the AIT2139 supports VGA 640 x 480, SVGA 800 x 600, XGA 1024 x 768, Mac 640 x 480, 832 x 624, and NEC 640 x 400 underscan modes.

Positioning

Four positioning function pins allow the encoded graphic image to be shifted up/down and left/right in case the video image needs to be centered or repositioned.

Zooming and Panning

The Zoom feature doubles the video image size in both the horizontal and vertical directions. Each VGA pixel will become an equivalent of 4-pixels displaying to video. In the Zoom mode, the positioning function pins will act as panning control to pan the zoom-window across the expanded VGA image.

Internal Digital Video Encoder

The processor section of the AIT2139 accepts the digital video data at the external memory device I/O port in YUV 4:2:2 format. The processor input is separated into the luminance and chrominance components. The chrominance signals are modulated by a digitally synthesized subcarrier. The luminance and chrominance signals are separately interpolated to twice the pixel rate, and converted into analog S-Video signals by two 10-bit D/A converters. The analog Composite video signal is output by a third 10-bit D/A converter. The AIT2139 also provides pin-selectable analog Y/P_rP_b(Sync on Y) or RGB output format for applications that demand the highest quality display. A Color Space Converter is used to convert Y/P_rP_b to RGB format.

Encoder Timing

The processor operates from a single clock at 27 MHz. Different preset timing parameters are selected with the format control pins. These pins configure the AIT2139 for NTSC, NTSC-EIAJ, and PAL-B/D/G/H/I/M/N television standards.

Blanking

The AIT2139 is designed to blank the video screen to blue by setting BLANK control input to High.

Power Conservation

The AIT2139 supports the VESA DPMS power down mode to conserve power. The operational state of the AIT2139 is controlled by the pulse activity on VGA HSync and VSync according to *Table 3*. I^2C can also be used to detect the present of HSync and Vsync. When the AIT2139 is not in use, it can further conserve power by using the PWRDN pin or via I^2C.

Package Interconnections

Signal Type	Name	Function	Type/Value	Package/Pin MQFP
Clock	$XTAL_{1-2}$	Subcarrier Reference Crystal/Clock	-	61, 62
Global Controls	$TVSTD_{1-0}$	Video Output Standard Select	TTL	90, 98
	PAL_NTSC			103
	FIL	Flicker Filter Select	TTL	104
	RESET\	Reset	TTL	3
	PHASE	Sampling Phase Control	TTL	120
	YUV_OUT	YUV output Select	TTL	106
	RGB_OUT	RGB output Select	TTL	107
	FREEZE	Video Image Freeze Select	TTL	123
	ZOOM	Video Image Zoom Select	TTL	102
	OVRSCN	Overscan and Underscan Select	TTL	105
	$POS_{U, L, R, D}$	Video Image Position Controls	TTL	113, 112, 111, 110
Encoder Controls	CVIDEN	Composite Video D/A Control	TTL	67
	SVIDEN	S-Video D/A Control	TTL	66
	BLANK	Blank Screen Generator	TTL	122
	EN_RST\	Encoder Reset	TTL	86
Video Inputs	R, G, B	Analog RGB Inputs	V_{RT}	83, 88, 94
	V_{TIN}	A/D Converter Reference Input, Buffered	+0.85V	80
	V_{TOUT}	A/D Converter Reference Output, Buffered	+0.85V	81
	V_{RT}	A/D Converter Reference Input, Unbuffered	+0.85V	93
	HSRAW	VGA Horizontal Sync	TTL	125
	VSRAW	VGA Vertical Sync	TTL	127
Video Outputs	COMPOSITE	NTSC/PAL Video Output	1 V p-p	75
	LUMA	Luminance-only Video	1 V p-p	72
	CHROMA	Chrominance-only Video	1 V p-p	77
	HSOUT	Buffered VGAHS Output	TTL	126
	VSOUT	Buffered VGAVS Output	TTL	128
	CSYNC	Composite Synchronization Signal Output	TTL	82
Encoder Reference	V_{REF}	D/A Voltage Reference Input/Output	+1.235V	74
	R_{REF}	Current-setting Resistor	140Ω	70
SDRAM Memory I/O	$PDI_{0\sim15}$	Bi-directional Data I/O from/to memory	TTL	37, 38, 39, 40, 41, 43, 44, 45, 46, 47, 48, 49, 50, 51, 53, 54
	$PDO_{0\sim11}$	Address Output Pins from memory	TTL	17, 18, 20, 21, 22, 23, 24, 25, 26, 27, 28,30
	PDO_12	CAS\, Column Address Strobe	TTL	31
	PDO_13	RAS\, Row Address Strobe	TTL	32
	PDO_14	DQM, Data Input/Output mask	TTL	33

	PDO_15	MWR\, Memory Read/Write Input	TTL	34
	MW_CLK	CLK, Clock Signal	TTL	14
	MW_RST	CKE, Enable/Disable Clock Signal	TTL	15
	MW_EN	CS\, Enable/Disable Command Decoder	TTL	16
	SDR	SDRAM Memory Select	TTL	121
EDO Memory I/O	PDI$_{0\sim15}$	Bi-directional Data I/O from/to memory	TTL	37, 38, 39, 40, 41, 43, 44, 45, 46, 47, 48, 49, 50, 51, 53, 54
	PDO$_{0\sim8}$	Address Output Pins from memory	TTL	17, 18, 20, 21, 22, 23, 24, 25, 26
	PDO_12	CAS\, Column Address Strobe	TTL	31
	PDO_13	RAS\, Row Address Strobe	TTL	32
	PDO_14	MOE\, Memory Output Enable	TTL	33
	PDO_15	MWR\, Memory Read/Write Input	TTL	34
I^{2}C-bus	I^{2}C_SDA	I^{2}C Serial Data Input (logic “high” or logic “low”)	TTL Tri-Stat	118
	I^{2}C_SCL	I^{2}C Serial Data Input (<400KHz)	TTL	116
	I^{2}C_ADR	Slave Device Address Select	TTL	117
Power	$V_{DD\_3.3}$	SDRAM I/O Power Supply	+3.3V	13, 36, 58*
	V_{DD}	Digital Power Supply	+5.0 V	1, 6, 9, 59, 71, 92, 101, 115, 100,109
	V_{DDA}	Analog Power Supply	+5.0 V	96, 91, 85, 78, 79, 65
	VDDPLL	A/D Phase Locked Loop Power	+5.0 V	12
Ground	GNDPLL	A/D Phase Locked Loop Ground	0.0 V	10
	DGND	Digital Ground	0.0 V	2, 7, 19, 29, 42, 52, 63, 87, 97, 114, 119, 124
	AGND	Analog Ground	0.0 V	64, 76, 84, 89, 95, 108
No Connect	NC	Do Not Connect	-	4, 8, 35, 60, 68, 99, 55, 56, 57
MISC	T_EN	Testing ONLY. Must Tie to Low	TTL	5
	PLL_LPF	PLL Low Pass Filter	Analog	11
	C_COMP	Compensation Capacitor	Analog	69
PWRDN	PD_EN	Power down enable	TTL	73

Note: * PIN13, 36, 58 also can be connected to V_{DD}

Signal Definitions

A/D Converter Interface

R, G, B Red, Green, Blue analog input from graphic card/computer. The expected voltage range of these input signals is from 0.0 to 0.85 Volts.

HSRAW Horizontal sync input from Graphic controller. The polarity of graphic HS is internally corrected to active Low whether the incoming graphic HS is active High or active Low.

VSRAW Vertical sync input from Graphic controller. The polarity of graphic VS is internally corrected to active Low whether the incoming graphic VS is active High or active Low.

V_{RT} A/D reference in, unbuffered. This pin should be connected to a voltage follower or V_{TOUT} pin.

V_{TIN} Input to top reference voltage buffer. External 0.1 uF bypass capacitor should be used.

V_{TOUT} Top reference voltage buffer output that may be connected to V_{RT} to supply current to A/D converter reference resistors. In power down mode, V_{TOUT} drops to zero.

Clock Generators

$XTAL_{1-2}$ Connection points for the 27 MHz oscillator or crystal. If an oscillator is used, its output should be fed into $XTAL_1$. If a crystal is used, it should be connected across $XTAL_1$ and $XTAL_2$ along with the proper resistors and/or capacitors, as required by the crystal manufacturer. Use only a fundamental type crystal.

AIT2139 Controls

$TVSTD_{1-0}$ Video output standard select. The AIT2139 has preprogrammed timings, sub-carrier frequencies

PAL_NTSC and phase data that corresponds to worldwide NTSC and PAL standards. These input select pins direct the appropriate timing and sub-carrier data to the processor for set-up (refer to *Table 1*).

FIL Vertical Filter Mode selects (state machine). The 3-line flicker reduction filter may be configured for 3-line filtering, 2-line filtering, and no vertical filtering modes with these pins. Pulsing the FIL control pin will cycle through the different filtering modes as shown in *Table 2.*

YUV_OUT When High, the AIT2139 is configured for YUV output, the COMPOSITE, LUMA, and CHROMA output pins will output Y, U, and V respectively. When Low, YUV output is disabled.

RGB_OUT When High, the AIT2139 is configured for RGB output, the CHROMA, COMPOSITE, and LUMA output pins will output R, G, and B respectively. When Low, RGB output is disabled.

FREEZE When brought to High, writing to the external field store devices stops on the next falling edge of VSYNC\. When brought to Low, writing to the external field store devices resumes on the next falling edge of VSYNC\.

ZOOM A pulse triggering pin, i.e., a pulse toggles the state of zoom in /out. The video image size can be doubled in both the horizontal and vertical directions (note: this makes the image 4x larger) during zoom in. The video image displays can be set back to the normal size by toggling this pin.

POS_D, POS_R, POS_U, POS_L — The position controls change the processor timing relative to incoming video so that the viewed image may be shifted right or down, to reveal portions of the image that may be found near the edges or in the overscan areas. Vertical position is adjusted 2 lines per frame, total of 128 lines. Horizontal position is moved 2 pixels per frame, total 128 pixels. Only POS_D, POS_R are used during 2_POS = 1 (High). When in the two-toggle positioning mode, upon reaching the end, the video image will revert to the most upper left position. In the 4-toggle positioning mode (2_POS = 0 or Low), reversion is not supported and all 4 positioning controls have to be used in order to scroll back the image. During Zoom operation, the 4 positioning controls remains available, and are used for panning the image across the active video area. All four positioning control pins are level sensitive pins. POS_D and POS_R are active Low. POS_U and POS_L are active High.

OVRSCN — A toggle input. Internally pulled-low (equal to logic "0" or Low). The video output is toggled between underscan and overscan. OVRSCN is only available at 640 X 480 resolution.

Table 1. TV Standard Control

Television Standard	PAL_NTSC	TVSTD0	TVSTD1
NTSC	0	0	0
NTSC – EIA	0	1	0
PAL - M	0	0	1
PAL – N	1	0	0
PAL – BDGHI	1	1	0
PAL – Combination N	1	1	1

Table 2. FIL Filter Mode Select Sequence

FIL	Filter Mode
↓ ⌉	3-line
↓ ↑	2-line
↓ ↑	No filter
⌊ ↑	Color bars

Encoder Controls

CVIDEN — Composite video D/A control. When High, the Composite D/A converter is always enabled. When Low, the Composite D/A converter is disabled when TV is not connected to the Composite port, vice versa. The Composite D/A status can be readback from the Output Control Register, OCR[4], through I^2C.

SVIDEN — S-Video D/A control. When High, the CHROMA and LUMA D/A converters are always enabled. When Low, the CHROMA and LUMA D/A converters are disabled when TV is not connected to the S-Video port, vice versa. The CHROMA and LUMA D/A status can be readback from the Output Control Register, OCR[3] and OCR[5] respectively, through I^2C.

BLANK — When High, BLUE screen is displayed on the screen until BLANK goes Low.

EN_RSTN — When Low, the all timing for the encoder will be reset. This is applicable when sync with an external video source.

Encoder Interface

V_{REF} — The voltage reference pin is the output of an internal 1.2 Volt band-gap type voltage reference. If this pin is left unconnected (except for a 0.1 microfarad capacitor to ground for noise de-coupling) the internal reference will be used for the three D/A converters. If an externally generated voltage reference of +1.2 Volts is applied to the V_{REF} pin, it will override the internal voltage reference and become the new reference for the D/A converters.

R_{REF} — A resistor of 140 Ohms is connected between the R_{REF} terminal and ground to set up the reference current for the three internal D/A converters. The value of this resistor determines the full-scale output current (and therefore the peak video level) of the D/A converters.

COM-POSITE — This analog base band composite video output can drive a 1 V_{PP} video into a 50Ω (150//75) terminated line. The composite signal contains all the sync, sub-carrier and active video information to drive monitors, projectors, VCRs or other video input devices. This pin will output the Y(with sync)/G component of YUV/RGB, when YUV_OUT/RGB_OUT pin is pulled High.

LUMA — This analog base band monochrome video output can drive a 1 V_{PP} video into a 50Ω (150//75) terminated line. The luminance signal contains all sync and active video information necessary to drive black-and-white video input devices. This pin will output the U/B component of YUV/RGB, when YUV_OUT/RGB_OUT pin is pulled High.

CHROMA — This analog chrominance video output drives a 50 Ohm terminated line. The CHROMA signal, when combined with the LUMA output signal comprises an S-Video two-wire video signal and is suitable for driving monitors, projectors, VCRs and other S-Video input devices. This pin will output the V/R component of YUV/RGB, when YUV_OUT/RGB_OUT pin is pulled High.

CSYNC — Composite synchronization signal output for the converted video signal. In general, this pin is left not connected except for GENLOCK or other purposes.

SDRAM Memory I/O

PDI_{0-15} — Pixel Data Input/Output pins for YUV digital component video to/from the external line store devices.

PDO_{0-10} — Memory address output pin.

PDO_12 — CAS\, Column Address Strobe.

PDO_13 — RAS\, Row Address Strobe.

PDO_14 — DQM, Data Input/Output Mask.

PDO_15 — MWR\, Memory Read/Write Enable.

MW_CLK — CLK, Clock Signal.

MW_RST — CKE, Enable/Disable Clock Signal.

MW_EN — CS\, Enable/Disable Command Decorder.

SDR — SDRAM memory select pin. When High SDRAM memory configuration is selected. This pin is not connected when EDO memory is used instead of SDRAM.

EDO Memory I/O

PDI_{0-15} Pixel Data Input/Output pins for YUV digital component video to/from the external line store devices.

PDO_{0-8} Memory address output pin.

PDO_12 CAS\, Column Address Strobe.

PDO_13 RAS\, Row Address Strobe.

PDO_14 MOE\, Memory Output Enable.

PDO_15 MWR\, Memory Read/Write Enable.

Power and Ground

V_{DD} +5 Volt power to the internal digital circuits.

V_{DDA} +5 Volt power to the internal analog circuits. V_{DD} and V_{DDA} must come from the same source.

V_{DDPLL} +5 Volt power to the internal A/D phase locked loop. It should originate from the same power plane but not to share the same via with any other power supplies.

GND_{PLL} Ground point for the internal A/D phase locked loop. It should originate from the same ground plane but not to share the same via with other ground points.

DGND Ground point for the internal digital circuits.

AGND Ground point for the internal analog circuits. D_{GND} and A_{GND} should be connected to the same ground plane.

DPMS

VESA DPMS power-down mode is controlled by the pulse activity on HSRAW and VSRAW according to the following table:

Table 3. DPMS Power Down Select

DPMS State	VGAHS	VGAVS	AIT2139 state
On	active	active	On, video active
Stand-by	inactive	active	Stand-by, blue screen displayed
Suspend	active	inactive	Suspend, blue screen displayed
Off	inactive	inactive	Off, AIT2139 powered-down

The VGAHS and VGAVS signal can be readback from the Output Control Register (OCR[1:0]) through I^2C. This function will allow other devices in the application to support the standard VESA DPMS so as to conserve more power.

I^2C-Interface Operation

The AIT2139 provides an I^2C interface capability, which simplifies both the design and operation of the product. The AIT2139 I^2C bus uses two bi-directional wires, serial data (SDA) and serial clock (SCL) to transfer information between devices connected to the bus.   Each device is recognized by a unique address. The AIT2139 I^2C interface is only for slave mode so that the clock for synchronizing data transfer is generated by an I^2C master. There are ten accessible I^2C control registers. Writing to this control registers will override all other hardware or software control. Asserting chip reset causes the AIT2139 to regain set-up controls via hardware or software.

I^2C Interface Characteristics

1. Serial data and clock rate up to 100K Hz.
2. Always in slave mode.
3. All registers can be read/write.
4. Each access must include an 8-bit sub-address.
5. No response to general calls.

I^2C Input Pin

The AIT2139 I^2C interface is controlled by three hardware pins.

- I^2C_SDA : I^2C serial data input pin.
- I^2C_CLK : I^2C serial clock input pin.
- I^2C_ADR : This pin select one of the slave device addresses.

I^2C Device Address

The I^2C interface responds to the slave device address selected by the I^2C_ADR pin.

I^2C_ADR	Slave Device Address
0	10001000 (88h)
1	10001010 (8Ah)

I^2C Sub-Address

The I^2C Interface writes to one of the ten control registers. These control registers control various functions of the chip. The control register data will override current hardware or software settings. Each I^2C access must include one of these sub-addresses as defined in the following. The user must use the correct sub-address; otherwise the AIT2139 might lock into the wrong operating state.

Sub-Address	Mode	Register Definition
0	R	Status register
1	R/W	LSBs of 11-bit P1 term
2	R/W	MSBs of 16-bit P2 term
3	R/W	LSBs of 16-bit P2 term
4	R/W	MSBs of 16-bit P3 term
5	R/W	LSBs of 16-bit P3 term
7	R/W	Vertical Position Register
8	R/W	Encoder Control register
9	R/W	Input Control Register
A	R/W	MSBs of 11-bit P1term & MSBs of 11-bit subcarrier phase adjust
B	R/W	PLL control register
C	R/W	LSBs of PLL modulus
D	R/W	Input Mode Detect Register
E	R/W	Aperture correction register

11	R/W	Output Control Register
16	R/W	Horizontal Position Register
1D	R/W	LSBs of sub-carrier phase adjustment
20	R/W	Macrovision™ CPS0 byte
21	R/W	Macrovision™ CPS1 and CPS2
22	R/W	Macrovision™ CPS3 and CPS4
23	R/W	Macrovision™ CPS5 and CPS6
24	R/W	Macrovision™ CPS7 and CPS8
25	R/W	Macrovision™ CPS9 and CPS10
26	R/W	Macrovision™ CPS11 and CPS12
27	R/W	Macrovision™ CPS13 and CPS14
28	R/W	Macrovision™ CPS15 and CPS16
29	R/W	Macrovision™ CPS17 and CPS18
2A	R/W	Macrovision™ CPS19 and CPS20
2B	R/W	Macrovision™ CPS21 and CPS22
2C	R/W	Macrovision™ CPS23 and CPS24
2D	R/W	Macrovision™ CPS25 and CPS26
2E	R/W	Macrovision™ CPS27 and CPS28
2F	R/W	Macrovision™ CPS29 and CPS30
30	R/W	Macrovision™ CPS31 and CPS32
38	R/W	Close Caption first byte odd field
39	R/W	Close Caption second byte odd field
3A	R/W	Close Caption first byte even field
3B	R/W	Close Caption second byte even field
3D	R	Device ID register
3E	R/W	Macrovision™ control byte
3F	R/W	Macrovision™ control byte verify register

I^{2}C Write Cycle Format

The AIT2139 I^{2}C interface supports read and write cycle operations by the master device. I^{2}C WRITE and READ access has the following transfer protocol (continuous write mode is also supported):

[Write]

Start	Device Addr	Write	Ack	Sub Addr	Ack	Data (N)	Ack (N)	Stop

[Read]

Start	Device Addr	Write	Ack	Sub Addr	Ack	Start	Device Addr	Read	Ack	Data	Ack	Stop

Start: The start condition is defined as the falling edge of the SDA signal while SCL (serial clock) is high.

Slave Address: The 7-bit slave device address used by the AIT2139. Once communication is established, the AIT2139 expects a device address ID from the master device. This device address is determined by the state of the I^{2}C_ADR pin.

Write: This bit is "0" for I^{2}C write operation and "1" for I^{2}C read operation.

Ack: This bit is the acknowledge bit. The AIT2139 pulls the SDA data line to logic "low" to acknowledge successful reception of the 8-bit data.

Sub Address: The 8-bit sub-address for accessing to one of the control registers.

Data: The 8-bit value to be written into the control register.

Stop: The stop condition is initiated to terminate the I^2C communication. It is defined as the rising edge of SDA signal while SCL is logic "high".

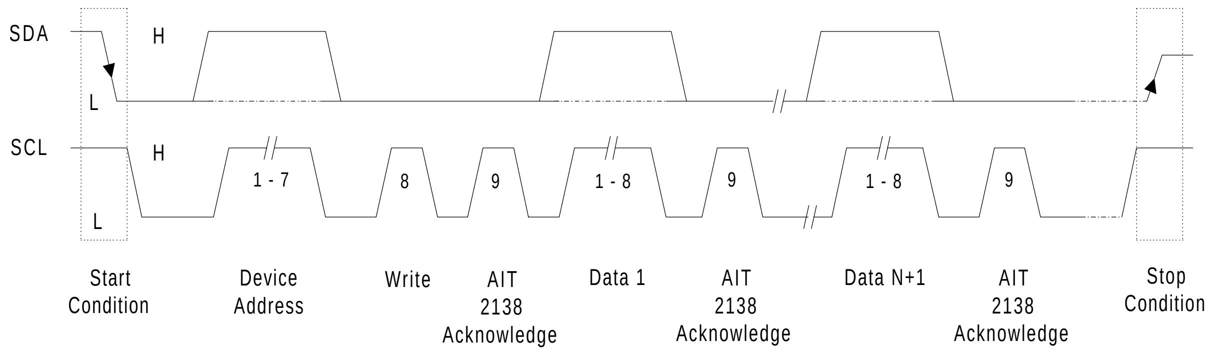


Figure 1. An I^2C interface transfer protocol of the AIT2139 for WRITE operation.

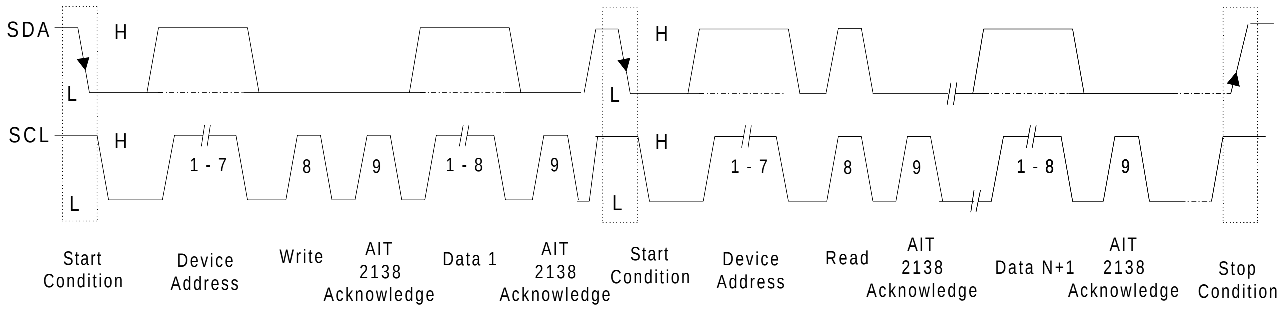


Figure 2. An I²C interface transfer protocol of the AIT2139 for READ operation.

Once the I²C interface updates a control register. The contents of the control register will override other external hardware or software controls. Once written, the I²C control information can only be changed by writing new information via the I²C port or by asserting the reset pin of the AIT2139. Access to each control register must start with the START condition and end with the STOP condition.

I²C Register Definition

Status Register (SR) — **Address : 00H** — **Bits : 8**

Bit	7	6	5	4	3	2	1	0
Type	Reserve	Reserve	R	R	R	R	R	R

Bit 7 RESERVED
Bit 6 RESERVED
Bit 5:2 VGA INPUT MODE
Bit 1 LINE 21 CAPTION
1 = Bytes not sent
0 = Bytes had been sent
Bit 0 LINE 284 CAPTION
1 = Bytes not sent
0 = Bytes had been sent

P1 LSB Register (P1) — **Address: 01H** — **Bits: 8**

Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7:0 P1 TERM LSB P1[7:0]

The P1 term is an 11-bit number. The least significant 8-bit is in this register. The most significant 3-bit is located at sub-address A. The P1, P2, and P3 terms control the color sub-carrier frequency.

P2 MSB Register (P2) **Address: 02H**
Bits: 8

Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7:0 P2 TERM MSB P2[15:8]

The P2 term is a 16-bit number. The most significant 8-bit is in this register. The least significant 8-bit is located at sub-address 3. The P1, P2, and P3 terms control the color sub-carrier frequency.

P2 LSB Register (P2) **Address: 03H**
Bits: 8

Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7:0 P2 TERM LSB P2[7:0]

The P2 term is a 16-bit number. The least significant 8-bit is in this register. The most significant 8-bit is located at sub-address 2. The P1, P2, and P3 terms control the color sub-carrier frequency.

P3 MSB Register (P3) **Address: 04H**
Bits: 8

Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7:0 P3 TERM MSB P3[15:8]

The P3 term is a 16-bit number. The most significant 8-bit is in this register. The least significant 8-bit is located at sub-address 5. The P1, P2, and P3 terms control the color sub-carrier frequency.

P3 LSB Register (P3) **Address: 05H**
Bits: 8

Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7:0 P3 TERM LSB P3[7:0]

The P3 term is a 16-bit number. The least significant 8-bit is in this register. The most significant 8-bit is located at sub-address 4. The P1, P2, and P3 terms control the color sub-carrier frequency.

Vertical Position Register (VPR) **Address: 07H**
Bits: 8

Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7:0 VERTICAL POSITION

The 8-bit binary value defines the vertical position of the output video image. The 8-bit value is a 2-compliments signed number. Each input mode has its own startup default value. Subtracting from the start up default value will move the screen downward. Adding to the start up default value will move the screen upward. Each step represents 1 pixel. Since VPR is a signed-value, the most significant bit of this register is the sign bit.
Note that writing into this control register will override the current setting. The vertical position hardware pins are disabled until the chip is being reset.

Encoder Control Register (ECR) **Address: 08H**
Bits: 8

Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 COLOR BAR ENABLE
1 = Enable color bar output
0 = Normal output

Bit 6 BLANK
1 = Blank output
0 = Normal output

Bit 5,2,4 TV OUT FORMAT
000 = NTSC (7.5 IRE setup)
001 = NTSC (no setup) (NTSC-EIA)
010 = PAL-N
011 = PAL I,G,H,B,D
100 = PAL-M
101 = NTSC (no setup) (NTSC-EIA)
110 = PAL I,G,H,B,D
111 = PAL combination N

Bit 3 UV_SEL
0 = Swap U, V color processing
1 = Normal color processing

Bit 1 NO_ROMS
Must be zero

Bit 0 NO_V_DT
Must be zero

This register controls the encoder function. For PAL TV out format, the input process control register IPCR[4] must be set to 1.

Input Process Control Register (IPCR) **Address: 09H**
Bits: 8

Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 ZOOM
1 = Enable Zoom output
0 = Normal output
Bit 6 OVERSCAN
1 = Enable Overscan output (only at 640x480)
0 = Normal output
Bit 5 FREEZE
1 = Freeze output
0= normal output
Bit 4 PAL SELECT
1 = PAL output
0 = NTSC output
Bit 3:2 FILTER TYPE
00 = 3 lines filter
01 = 2 lines filter
10 = No flicker filter
Bit 1:0 HORIZONTAL FILTER
2 = high bandwidth low pass filter
1 = low bandwidth low pass filter
0 = no horizontal low pass filter

Sub-Carrier Misc Register (SCMR) **Address: 0AH**
Bits: 8

Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	Reserved	R/W	R/W	R/W

Bit 7 RESET SUB-CARRIER PHASE
1 = Reset phase every 8 frames
0 = No reset
Bit 6:4 MSB OF SUB-CARRIER PHASE SCPR[10:8]
Bit 3 Reserved
Bit 2:0 MSB OF P1 TERM P1[10:8]

PLL Control Register (PCR) **Address: 0BH**
Bits: 8

Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7:6 MSB OF PLL MODULUS PMR[9:8]
Bit 5:4 INTERNAL CLOCK DELAY ADJUST
Bit 3 PLL PRE_D2 CONTROL
Bit 2 PLL OUT_D2 CONTROL
Bit 1 PLL FEB1_D2 CONTROL
Bit 0 RESET

PLL Modulus Register (PMR) **Address: 0CH**
Bits: 8

Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7:0 LSB OF PLL MODULUS PMR[7:0]

Input Mode Detect Register (IMDR) **Address: 0DH**
Bits: 8

Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reserved

Bit 7 V FREQ
1 = within range of V Freq > 63 Hz
Bit 6 V LINE COUNT
1 = More than 470 vertical lines
Bit 5 V LINE COUNT
1 = More than 530 vertical lines
Bit 4 V LINE COUNT
1 = More than 700 vertical lines
Bit 3 V FREQ
1 = within range of 63 Hz < V freq < 69 Hz
Bit 2 V FREQ
1 = within range of 69 Hz < V freq < 73 Hz
Bit 1 V FREQ
1 = within range of 73 Hz < V freq < 79 Hz
Bit 0 RESERVED

Aperture Control Register (ACR) **Address: 0EH**
Bits: 8

Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 LINE 21 CLOSE CAPTION ENABLE
Bit 6 LINE 284 CLOSE CAPTION ENABLE
Bit 5:4 Y-CHANNEL DELAY
00 = No delay
01 = 1clock delay
10 = 1 clock delay
11 = 2 clock delay
Bit 3 MAXIMUM CORRECTION
Bit 2 CORRECTION/2
Bit 1 CORRECTION/4
Bit 0 CORRECTION/8

Output Control Register (OCR) **Address: 11H**
Bits: 8

Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit 7 POWER DOWN
1 = Enable power down
0 = normal operation
Bit 6 POWER DOWN CLOCK
1= Enable power down clock generator
0 = normal operation
Bit 5 DISABLE Y DAC
1 = Disable Y DAC
0 = Enable Y DAC
Bit 4 DISABLE COMPOSITE DAC
1 = Disable composite DAC
0 = Enable composite DAC
Bit 3 DISABLE C DAC
1 = Disable C DAC
0 = Enable C DAC
Bit 2 CHROMA LOW PASS FILTER BANDWIDTH CONTROL
1 = High
0 = Low
Bit 1 HSYNC
1 = Present
0 = Absent
Bit 0 VSYNC
1 = Present
0 = Absent

The OCR bit-3, 4 and 5 is used to enable/disable the Y, Composite and C DAC respectively. On readback, it can be used to detect the present of TV connection to the S-Video or Composite port (CVIDEN and SVIDEN pins must be tied to Low).

Horizontal Position Register (HPR) **Address: 16H**
Bits: 8

Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7:0 HORIZONTAL POSITION

The 8-bit binary value defines the horizontal position of the output video image. The 8-bit value is a 2-compliments number. Each operating mode has its own startup default value. Subtracting from the start up default value will move the screen to the right. Adding to the start up default value will move the screen to the left. Each step represents 2-pixels. Since HPR is a signed-value, the most significant bit of this register is the sign bit.
Note that writing into this control register will override the current setting. The horizontal position hardware pin is disabled until the chip is being reset.

Sub-Carrier Phase Register (SCPR)

Address: 1DH
Bits: 8

Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7:0 LSB OF THE 11-BIT SUB-CARRIER PHASE REGISTER SCPR[7:0]

The most significant bits of the sub-carrier phase register is located at sub-address A. This adjustment is a 11-bit number with the range of 0 through 2048 representing 0 through 360 degree of phase adjustment.

Macrovision™ Control Registers (MVCR)

Address: 20H~30H
Bits: 8

Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Refer to the I^2C registers summary for the definition of these registers. For detail description of these registers, please refer to the Macrovision™ 7.01 specification.

Close Caption Data Register (CCDR)

Address: 38H~3BH
Bits: 8

Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sub-address 38h and 39h contain the first byte and second byte of the Line 21 Caption respectively. Odd parity for each byte is automatically generated during transmission. Before writing to these two registers, the users should check the Line 21 Caption flag in sub-address 0 (SR) bit 1 is clear. This flag is set automatically when the sub-address 38h is written. Writing into the sub-address 39h will not set this flag. Sub-address 3Ah, 3Bh contain the first byte and second byte of the Line 284 Caption respectively. Odd parity for each byte is automatically generated during transmission. . Before writing to these two registers, the users should check the Line 284 Caption flag in sub-address 0 (SR) bit 0 is clear. This flag is set automatically when sub-address 38h is written. Writing into sub-address 3Bh will not set this flag.

Device ID Register (IDR)

Address: 3DHBits: 8

Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

This register contains the device ID number. The value for this revision is 11 hex.

Macrovision™ Control Register (MVCR2)

Address: 3EH
Bits: 8

Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 AGC ENABLE
Bit 6 RESERVED
Bit 5 PSUEDO-SYNC ENABLE

Bit 4 BACK PORCH AGC ENABLE
Bit 3 COLOR STRIPS ENABLE
Bit 2 RESERVED
Bit 1 REDUCE HORIZONTAL SYNC
Bit 0 REDUCE VERTICAL SYNC

The MVVR[5:0] registers must be set to 3E hex before accessing this register(MVCR2).

Macrovision™ Verification Register (MVVR) Address: 3FH Bits: 8

Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 RESERVED
Bit 6 RESERVED
Bit 5:0 MACROVISION™ ACCESS MVID[5:0]

The MVID term is a 6-bit value that must be set to 3E hex before accessing the Macrovision™ Control Registers (MVCR2), writing any other value will lock the Macrovision™ Control Registers (MVCR2).

Closed Captioning

The AIT2139 supports closed captioning conforming to the standard Television Synchronizing Waveform for Color Transmission in Subpart E, Part 73 of the FCC Rules and Regulations and EIA-608. Closed captioning and text are transmitted during the blanked active line-time portion of Line 21.

The AIT2139 also supports the extended data services (EDS or XDS), which is transmitted during the blanked active line-time portion of Line 284. XDS is responsible for program name, start time, end time, call sign, etc.

Closed captioning consist of a 7-cycle sinusoidal burst that is frequency-locked and phase-locked to the caption data. After which the blanking level is maintained for two data bits, followed by a “1” start bit. The start bit is followed by 2 bytes of 16 bit data comprised of two 7 bit & 1 odd parity ASCII characters. The data for close captioning is stored in the Close Caption Data register (CCDR) 38h ~ 3Bh.

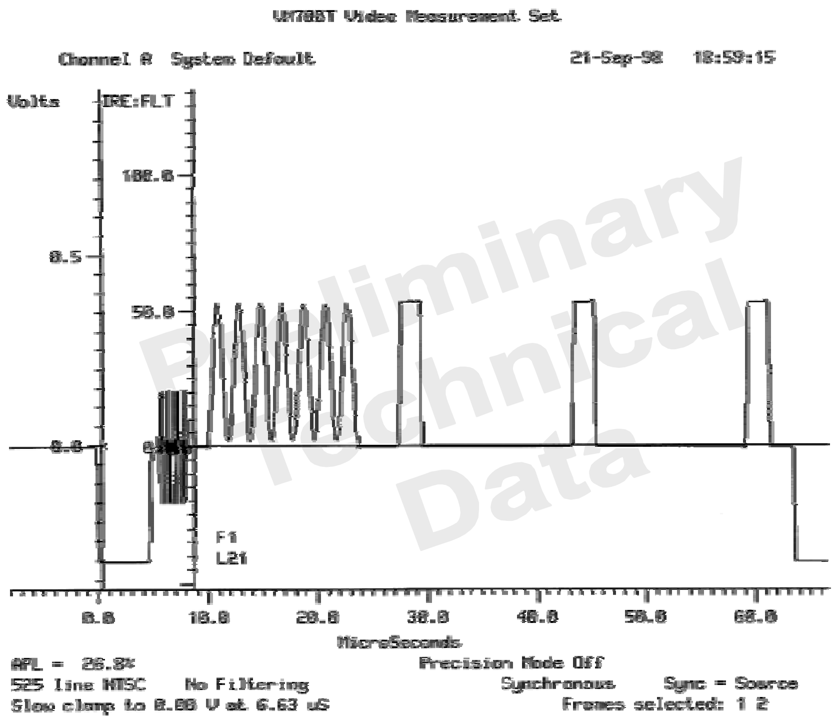


Figure 3. Closed Captioning Waveform (NTSC).

Video Measurements and Waveforms

The following displays the video measurements and waveforms of the AIT2139 for NTSC(M), NTSC(EIA) and PAL(B,D,G,H,I). These measurements and waveforms were used for quantifying signal distortions and rating the performance of the AIT2139. A Tektronix VM700T Video Measurement Set, a sophisticated test and measurement instrument that digitizes the video signal and automatically analyzes it in the digital domain, were used to obtain these measurements and waveforms.

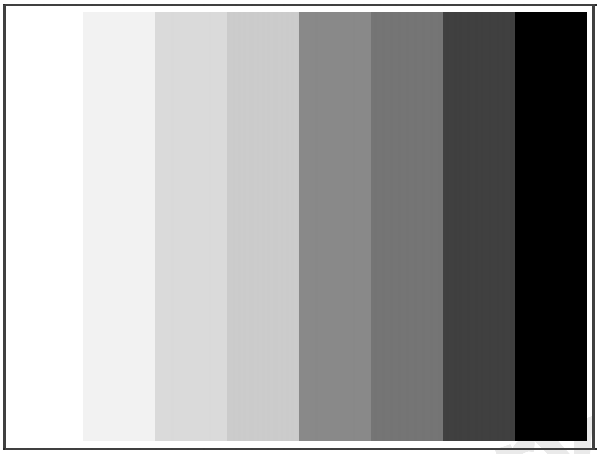


Figure 4. Color Bar (75% Amplitude, 100% Saturation) with white, yellow, cyan, green, magenta, red, blue, and black colors (from left to right) were used in the tests.

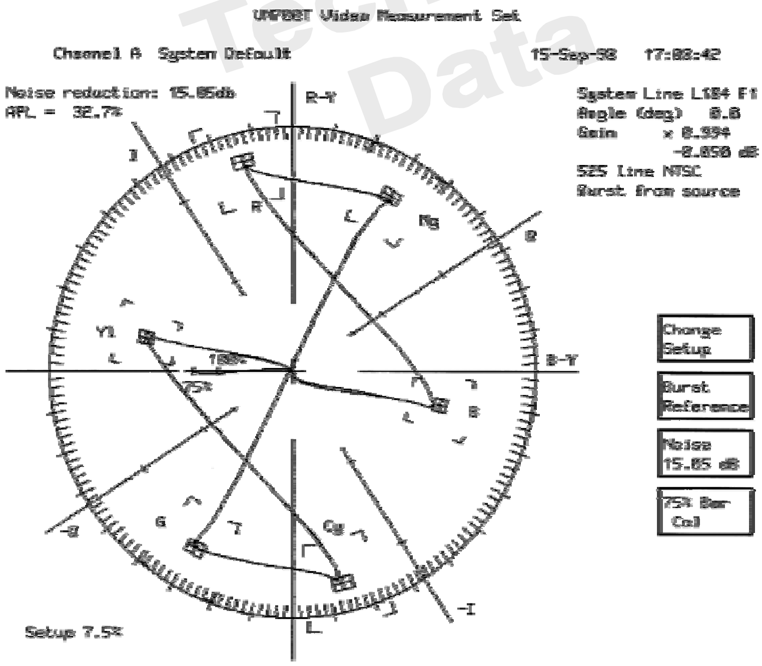


Figure 5. Vector Scope Display for NTSC Full-screen 75% Amplitude, 100% Saturation Color Bars.

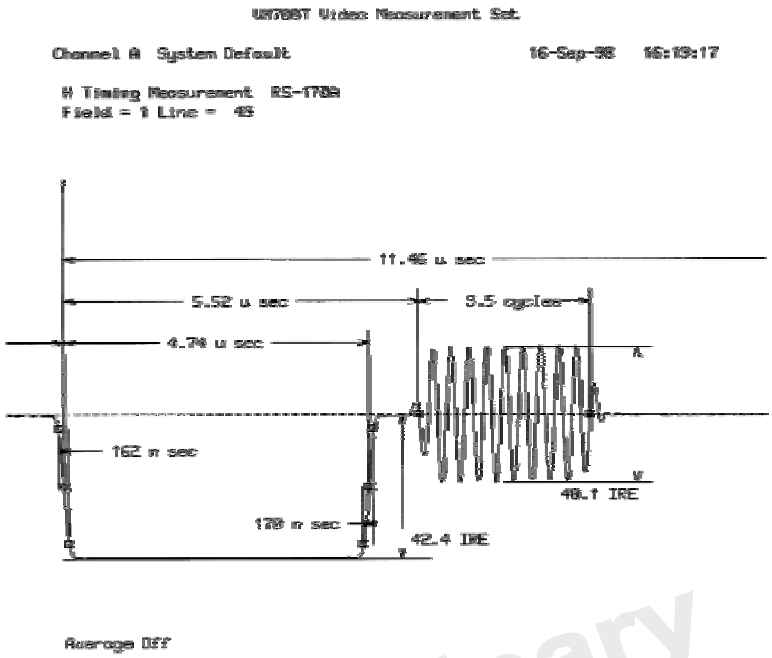


Figure 6. Horizontal Sync and Burst Interval Detail for NTSC.

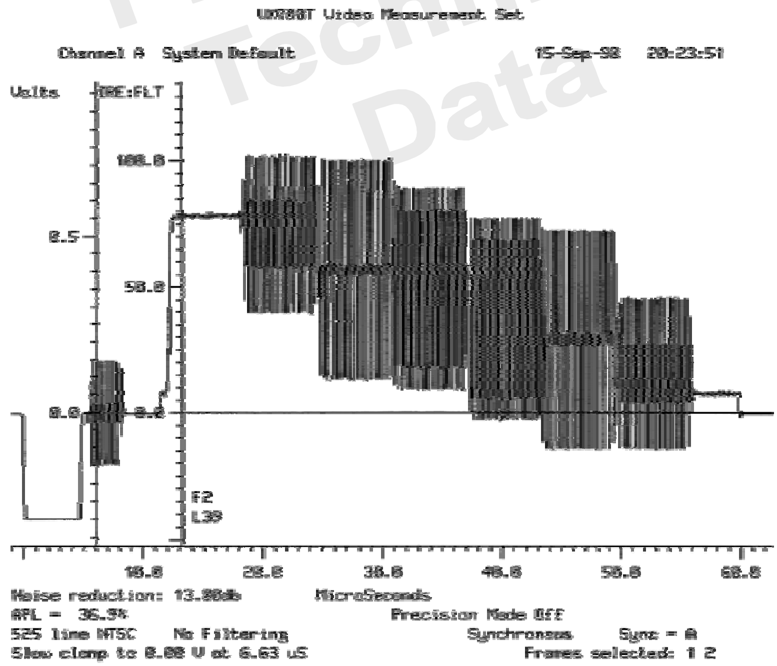


Figure 7. NTSC (M) Composite Video Signal for
75% Amplitude, 100% Saturation Color Bars.

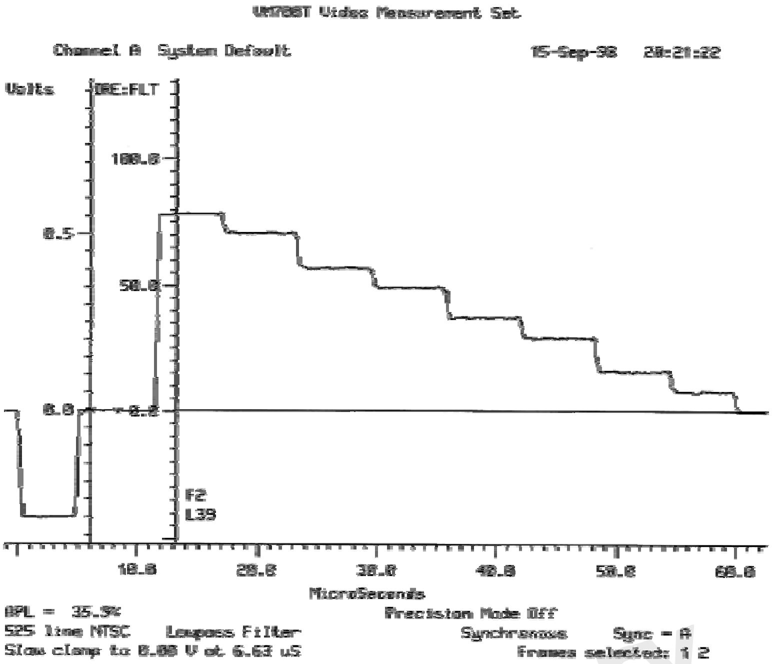


Figure 8. NTSC (M) Composite Video Signal for
75% Amplitude, 100% Saturation Color Bars (Luminance Only).

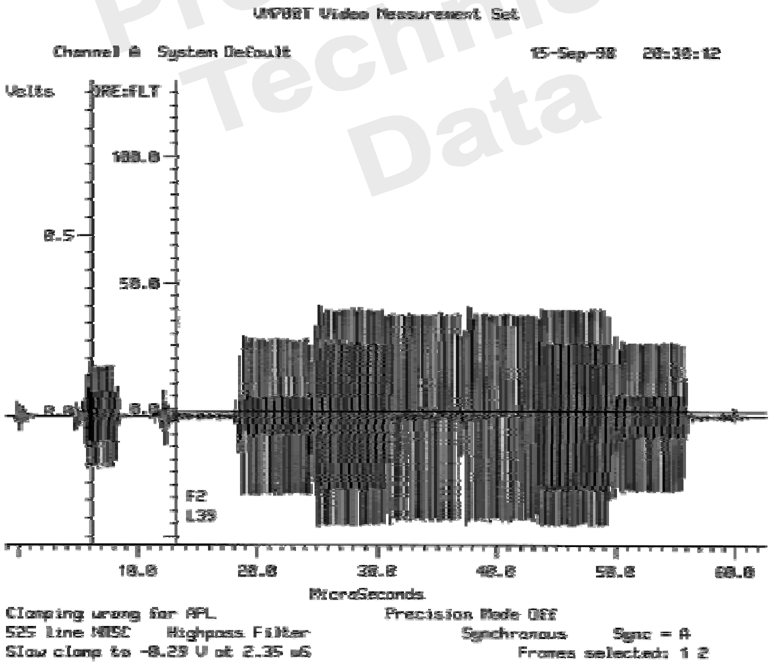


Figure 9. NTSC (M) Composite Video Signal for
75% Amplitude, 100% Saturation Color Bars (Chrominance Only).

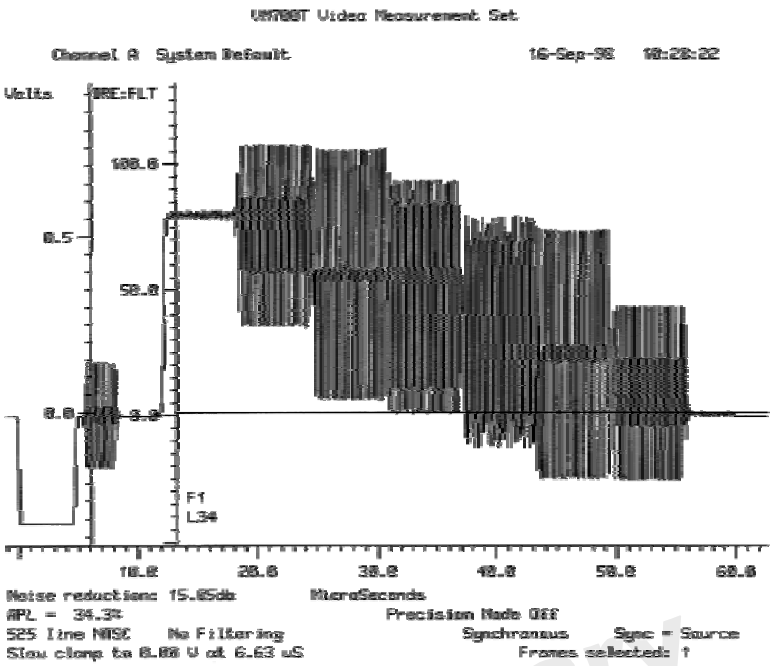


Figure 10. NTSC (EIA) Composite Video Signal for
75% Amplitude, 100% Saturation Color Bars.

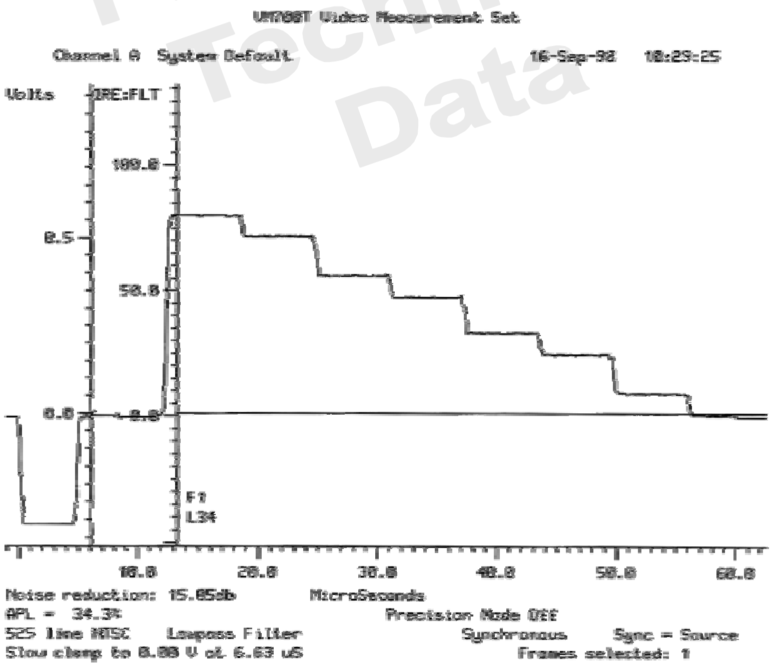


Figure 11. NTSC (EIA) Composite Video Signal for
75% Amplitude, 100% Saturation Color Bars (Luminance Only).

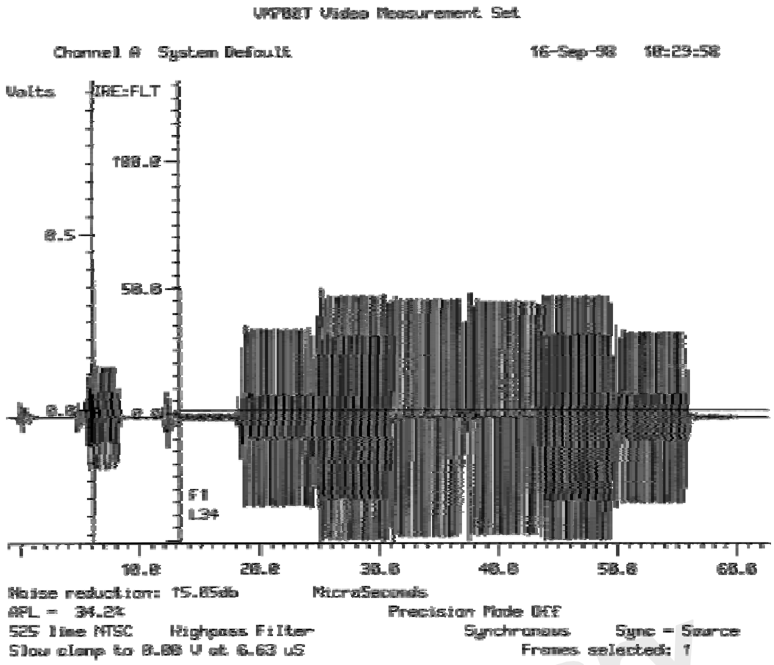


Figure 12. NTSC (EIA) Composite Video Signal for
75% Amplitude, 100% Saturation Color Bars (Chrominance Only).

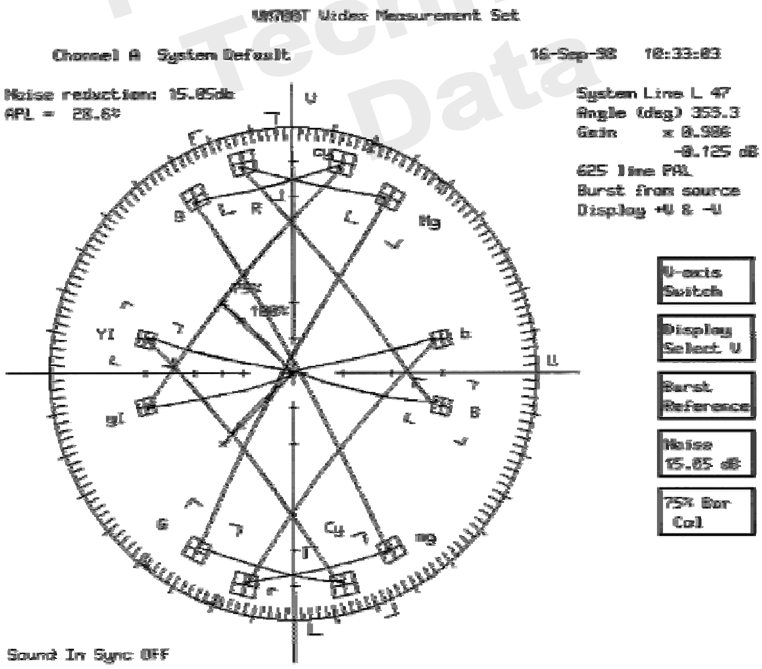


Figure 13. Vectorscope Display for PAL (B,D,G,H,I) Full-screen
75% Amplitude, 100% Saturation Color Bars.

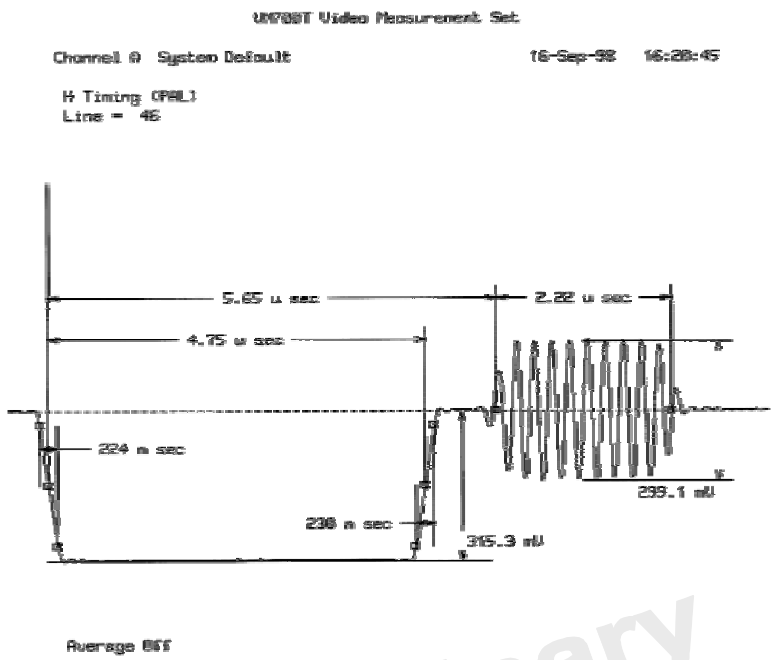


Figure 14. Horizontal Sync and Burst Interval Detail for PAL (B,D,G,H,I).

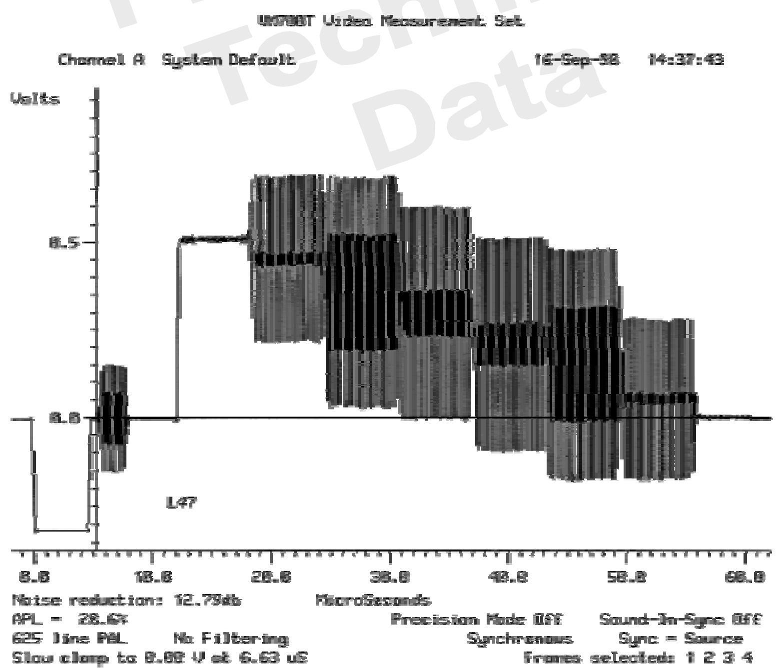


Figure 15. PAL (B,D,G,H,I) Composite Video Signal for
75% Amplitude, 100% Saturation Color Bars.

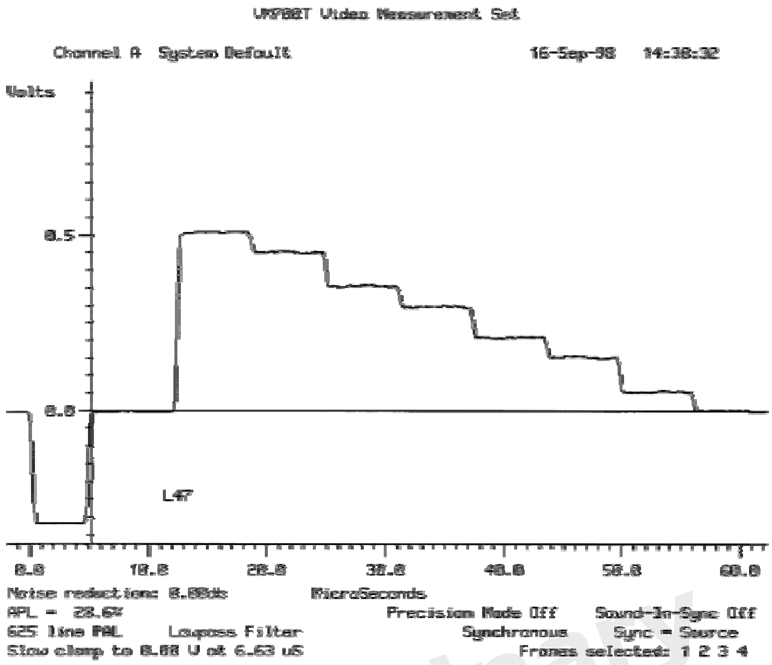


Figure 16. PAL (B,D,G,H,I) Composite Video Signal for
75% Amplitude, 100% Saturation Color Bars (Luminance Only).

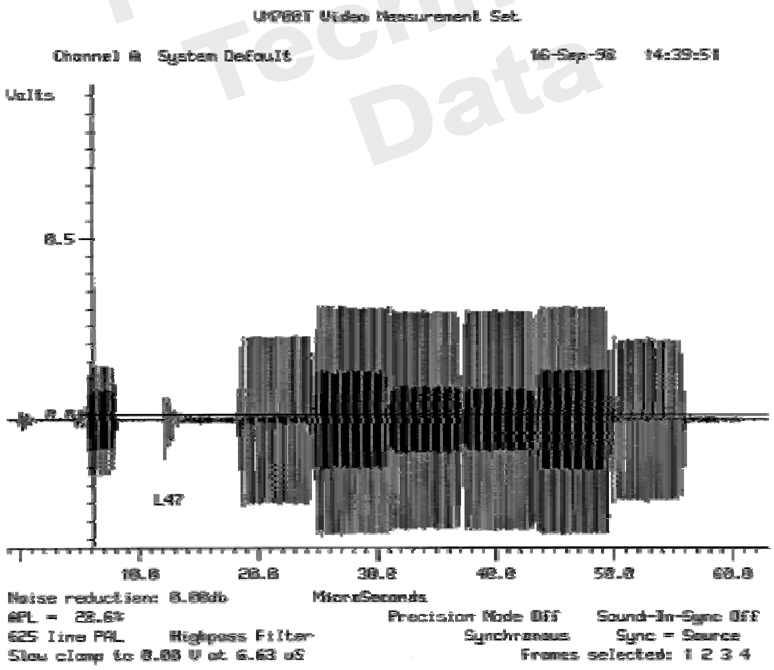


Figure 17. PAL (B,D,G,H,I) Composite Video Signal for
75% Amplitude, 100% Saturation Color Bars (Chrominance Only).

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter	Rating
Power Supply Voltages	
V_{DDA} (Measured to AGND)	-0.5 to +7.0V
V_{DD} (Measured to DGND)	-0.5 to +7.0V
V_{DDA} (Measured to VDD)	-0.5 to +0.5V
A_{GND} (Measured to DGND)	-0.5 to +0.5V
Digital Inputs	
Applied Voltage (Measured to DGND)[2]	-0.5 to V_{DD}+0.5V
Forced current [3, 4]	-10.0 to +10.0 mA
Analog Inputs	
Applied Voltage (Measured to AGND)[2]	-0.5 to V_{DDA}+0.5V
Forced current [3, 4]	-10.0 to +10.0 mA
Outputs	
Applied voltage (Measured to DGND)[2]	-0.5 to V_{DD} + 0.5V
Forced current [3, 4]	-6.0 to +6.0 mA
Short circuit duration (single output in High state to ground)	1 second
Temperature	
Operating, ambient	0 to 70°C
junction	+150°C
case	+140°C
Storage	-20 to +70°C
Electrostatic Discharge[5]	±150 V

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.
5. EIAJ test method.

Operating Conditions

Parameter		Min	Nom	Max	Units
V_{DD}	Digital Power Supply Voltage	4.00	5.0	5.50	V
$V_{DD\_3.3}$	SDRAM I/O Supply Voltage	3.00	3.3	3.60	V
V_{DDA}	Analog Power Supply Voltage	4.00	5.0	5.50	V
A_{GND}	Analog Ground (Measured to D_{GND})	-0.1	0	0.1	V
F_{xtal}	Crystal/Reference Clock Frequency		27.0000		MHz
f_{XTOL}	Crystal/Reference Clock Frequency Tolerance	0	±300	±1350	Hz
f_H	VGAHS Frequency	31.5		53.7[1]	KHz
f_V	VGAVS Frequency	50.0		85.0[2]	Hz
t_{PWH}	Reference Clock Pulse Width, High		18.5		ns
t_{PWL}	Reference Clock Pulse Width, Low		18.5		ns
t_{PWHS}	VGAHS Pulsewidth	2			µs
t_{VS-HS}	VGAVS to VGAHS Delay	0			ns
t_S	Control Input Pulse Width, High		50		ns
t_H	Control Input Pulse Width, Low		50		ns
V_{RT}	Reference Voltage, Top	0.5	0.85	2.0	V
V_{IN}	Analog Input Range	0		V_{RT}	V
V_{REF}	External Reference Voltage		1.25		V
I_{REF}	D/A Converter Reference Current ($I_{REF} = V_{REF}/R_{REF}$, flowing out of the R_{REF} pin)		8.92		mA
R_{REF}	Reference Resistor, V_{REF} = Nom		140		Ω
R_{OUT}	Total Output Load Resistance		50		Ω
V_{IH}	Input Voltage, Logic High	2.0			V
V_{IL}	Input Voltage, Logic Low			0.8	V
I_{OH}	Output Current, Logic High			-2.0	mA
I_{OL}	Output Current, Logic Low			4.0	mA
T_A	Ambient Temperature, Still Air	0		70	°C
T_C	Case Temperature, Still Air	30		105	°C

Note:

1. For 800 X 600, 85Hz
2. Resolution for 1024 X 768 supports up to 70Hz only.

Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Units
I_{DD}	Power Supply Current, Operating	CVIDEN=H, SVIDEN=H		300	400	mA
I_{DDSV}	S-Video Active	CVIDEN=L, SVIDEN=H		250	350	mA
I_{DDCV}	Composite Video Active	CVIDEN=H, SVIDEN=L		200	270	mA
I_{DDS}	Standby	CVIDEN=L, SVIDEN=L		80		mA
I_{DDQ}	Power Supply Current, Power-Down	V_{DD} = Max, PWRDN = Low		35		mA
V_{RO}	Voltage Reference Output		0.988	1.235	1.482	V
Z_{RO}	V_{REF} Output Impedance			3		KΩ
C_{AI}	Input Capacitance, A/D	ADCLK = Low		4		pF
		ADCLK = High		12		pF
R_{IN}	Input Resistance		500	1000		KΩ
I_{CB}	Input Current, Analog				±15	µA
C_I	Digital Input Capacitance			5	10	pF
C_O	Digital Output Capacitance			10		pF
I_{IH}	Input Current, High	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{IL}	Input Current, Low	V_{DD} = Max, V_{IN} = 0 V			±10	µA
I_{OS}	Short-Circuit Current		-20		-80	mA
V_{OH}	Output Voltage, High	I_{OH} = Max	2.4			V
V_{OL}	Output Voltage, Low	I_{OL} = Max			0.4	V

Switching Characteristics

Parameter		Conditions	Min	Typ	Max	Units
t_{DS}	Sync Output Delay	VGA Sync to Sync Out		100		ns
t_{DOV}	Analog Output Delay	PXCK Out to Video Out			15	ns
t_R	D/A Output Current Risetime	10% to 90% of Full Scale		2		ns
t_F	D/A Output Current Falltime	90% to 10% of Full Scale		2		ns

Input System Performance Characteristics

Parameter		Conditions	Min	Typ	Max	Units
E_{LI}	A/D Integral Linearity Error, Independent	V_{RT} = 2.0V		±0.3	±0.5	LSB
E_{LD}	A/D Differential Linearity Error	V_{RT} = 2.0V		±0.3	±0.5	LSB
E_{AP}	Aperture Error			30		ps
E_{OT}	Offset Voltage, Top	R_T - V_{IN} for most positive code transition	-20	45	80	mV
E_{OB}	Offset Voltage, Bottom	V_{IN} for most negative code transition	30	65	110	mV

Note: Values shown in Typ column are typical for V_{DD} = V_{DDA} = +5V and T_A = 25°C.

Output System Performance Characteristics

Parameter		Conditions	Min	Typ	Max	Units
RES	D/A Converter Resolution		10	10	10	Bits
dp	Differential Phase	PXCK = 27 MHz, 40 IRE Ramp		0.5		degree
dg	Differential Gain	PXCK = 27 MHz, 40 IRE Ramp		1.5		%
CNLP	Chroma Nonlinear Phase	NTC-7 Combination			±1.25	degree
CNLG	Chroma Nonlinear Gain	NTC-7 Combination			±1.0	%
PSRR	Power Supply Rejection Ratio	C_{BYP} = 0.1 µF, f = 1 KHz		0.5		% / $\%V_{DD}$

Notes:
1. Noise Level is unified weighted, 10 kHz to 5.0 MHz bandwidth, with Tilt Null ON measured using VM700 "Measure Mode."
2. Noise Level is unified weighted, 10 kHz to 5.0 MHz bandwidth, measured using VM700 "Auto Mode".

Table 18. AIT2139 MQFP Package - Pin Assignments

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{DD}	33	PDO_14	65	V_{DDA}	97	DGND
2	DGND	34	PDO_15	66	SVIDEN	98	TVSTD0
3	RESET\	35	NC	67	CVIDEN	99	NC
4	NC	36	* $V_{DD\_3.3}$	68	NC	100	VDD
5	T_EN	37	PDI_0	69	C_COMP	101	V_{DD}
6	V_{DD}	38	PDI_1	70	R_{REF}	102	ZOOM
7	DGND	39	PDI_2	71	V_{DD}	103	PAL_NTSC
8	NC	40	PDI_3	72	LUMA	104	FILTER
9	V_{DD}	41	PDI_4	73	PWRDN	105	OVRSCN
10	GNDPLL	42	DGND	74	V_{REF}	106	YUV_OUT
11	PLL_LPF	43	PDI_5	75	COMP	107	RGB_OUT
12	VDDPLL	44	PDI_6	76	AGND	108	AGND
13	* $V_{DD\_3.3}$	45	PDI_7	77	CHROMA	109	V_{DD}
14	MW_CLK	46	PDI_8	78	V_{DDA}	110	POS_D
15	MW_RST	47	PDI_9	79	V_{DDA}	111	POS_R
16	MW_EN	48	PDI_10	80	V_{TIN}	112	POS_L
17	PDO_0	49	PDI_11	81	V_{TOUT}	113	POS_U
18	PDO_1	50	PDI_12	82	CSYNC	114	DGND
19	DGND	51	PDI_13	83	R	115	V_{DD}
20	PDO_2	52	DGND	84	AGND	116	I^2C_SCL
21	PDO_3	53	PDI_14	85	V_{DDA}	117	I^2C_ADR
22	PDO_4	54	PDI_15	86	EN_RST\	118	I^2C_SDA
23	PDO_5	55	NC	87	DGND	119	DGND
24	PDO_6	56	NC	88	G	120	PHASE
25	PDO_7	57	NC	89	AGND	121	SDR
26	PDO_8	58	* $V_{DD\_3.3}$	90	TVSTD1	122	BLANK
27	PDO_9	59	V_{DD}	91	V_{DDA}	123	FREEZE
28	PDO_10	60	NC	92	VDD	124	DGND
29	DGND	61	XTAL1	93	V_{RT}	125	HSRAW
30	NC	62	XTAL2	94	B	126	HSOUT
31	PDO_12	63	DGND	95	AGND	127	VSRAW
32	PDO_13	64	AGND	96	V_{DDA}	128	VSOUT

Note: NC should be open, not connected to ground or VCC.
* This Pin also can be connected to VDD.

Figure 19. 128 Lead Metric Quad Flat Pack (MQFP) Outline

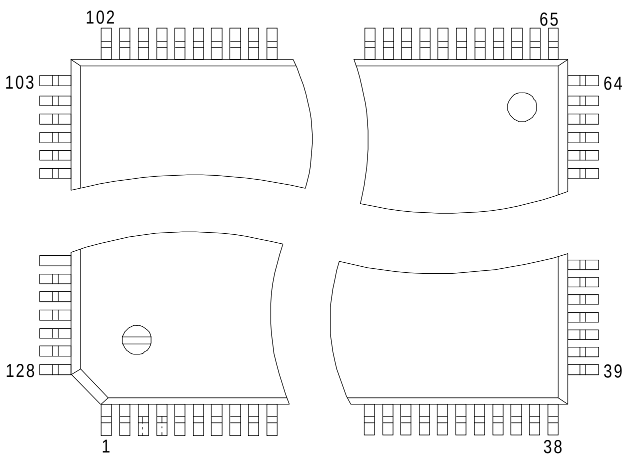
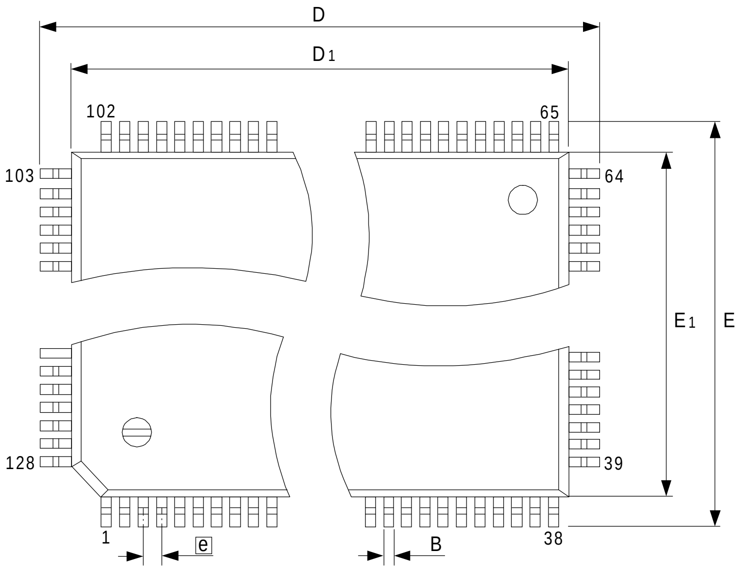


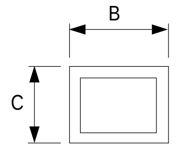
Figure 20. AIT2139 128-Lead Metric Quad Flat Pack (MQFP) Dimensions

NOTE:

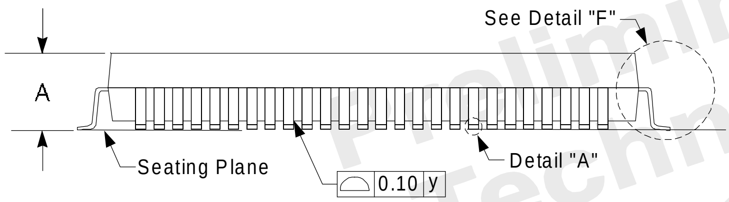
1. DIMENSIONS D_1 AND E_1 DO NOT INCLUDE MOLD PROTRUSION. BUT MOLD MISMATCH IS INCLUDED. ALLOWABLE PROTRUSION IS .25MM PER SIDE.
2. DIMENTION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION .08MM TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
3. CONTROLLING DIMENSION: MILLIMETER.

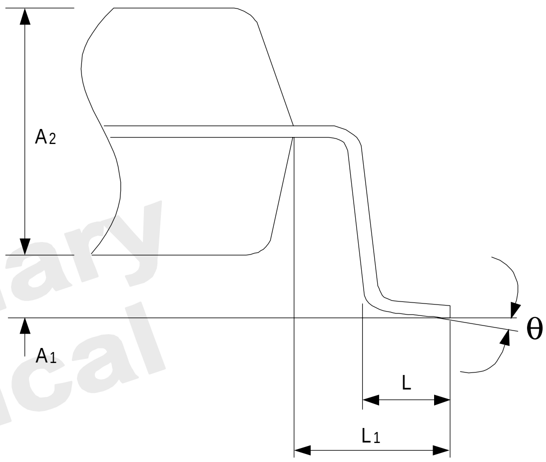
Symbol	Dimension (mm)		
	Min	Nom	Max
A	---	---	3.40
A_1	0.25	---	---
A_2	2.73	2.85	2.97
B	0.17	0.22	0.27
C	0.09	---	0.20
D	23.00	23.20	23.40
D_1	19.90	20.00	20.10
E	17.00	17.20	17.40
E_1	13.90	14.00	14.10
e	0.5 BSC		
L	0.73	0.88	1.03
L_1	1.60 BSC		
Y	---	---	0.10
θ	0°	---	7°





Detail "A"





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