

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74AC374P, TC74AC374F, TC74AC374FW, TC74AC374FT
TC74AC534P, TC74AC534F, TC74AC534FW

OCTAL D - TYPE FLIP - FLOP WITH 3 - STATE OUTPUT

TC74AC374P/F/FW/FT NON - INVERTING
 TC74AC534P/F/FW INVERTING

(Note) The JEDEC SOP (FW) is not available in Japan.

The TC74AC374 and TC74AC534 are advanced high speed CMOS OCTAL FLIP - FLOPS fabricated with silicon gate and double - layer metal wiring C²MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These 8 - bit D - type flip - flops are controlled by a clock input (CK) and an output enable input (\overline{OE}).

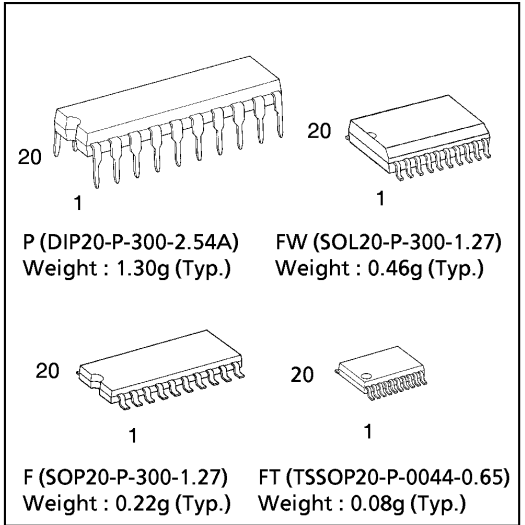
When the \overline{OE} input is high, the eight outputs are in a high impedance state.

The TC74AC374 has non - inverting outputs, and TC74AC534 has inverting outputs.

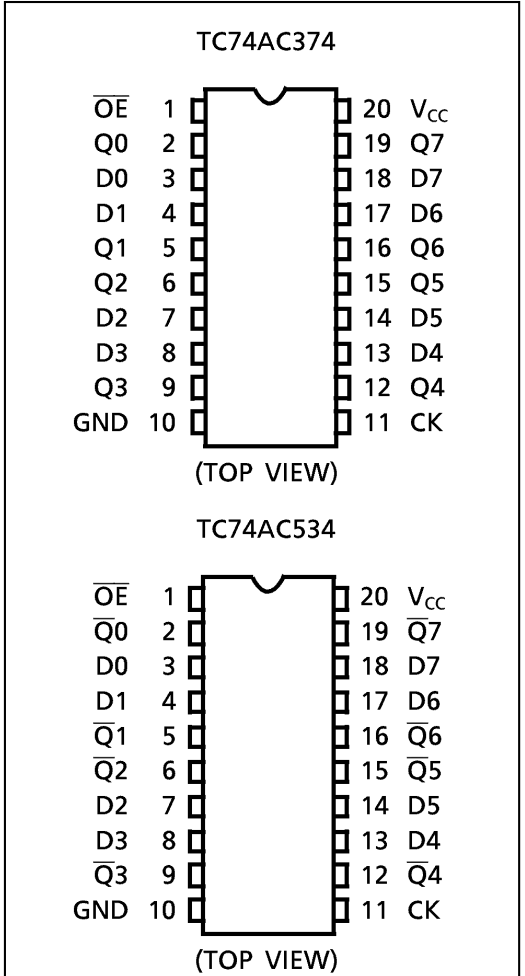
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

- High Speed..... $f_{MAX} = 200MHz$ (typ.)at $V_{CC} = 5V$
- Low Power Dissipation..... $I_{CC} = 8\mu A$ (Max.)at $T_a = 25^\circ C$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- Symmetrical Output Impedance $|I_{OH}| = I_{OL} = 24mA$ (Min.)
 Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range..... V_{CC} (opr) = $2V \sim 5.5V$
- Pin and Function Compatible with 74F 374/534



PIN ASSIGNMENT

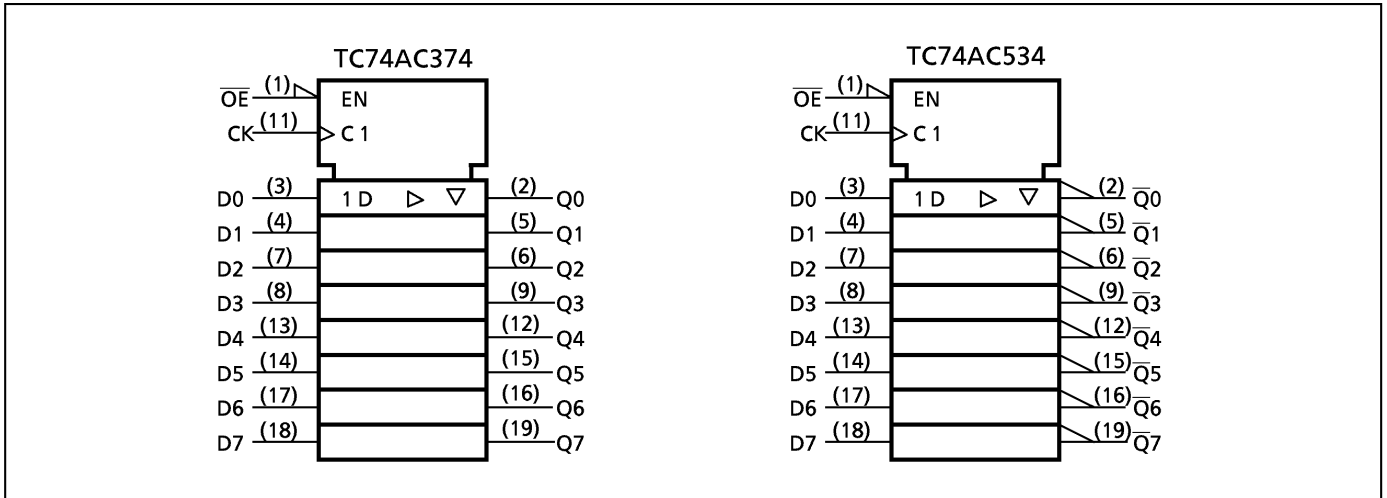


TRUTH TABLE

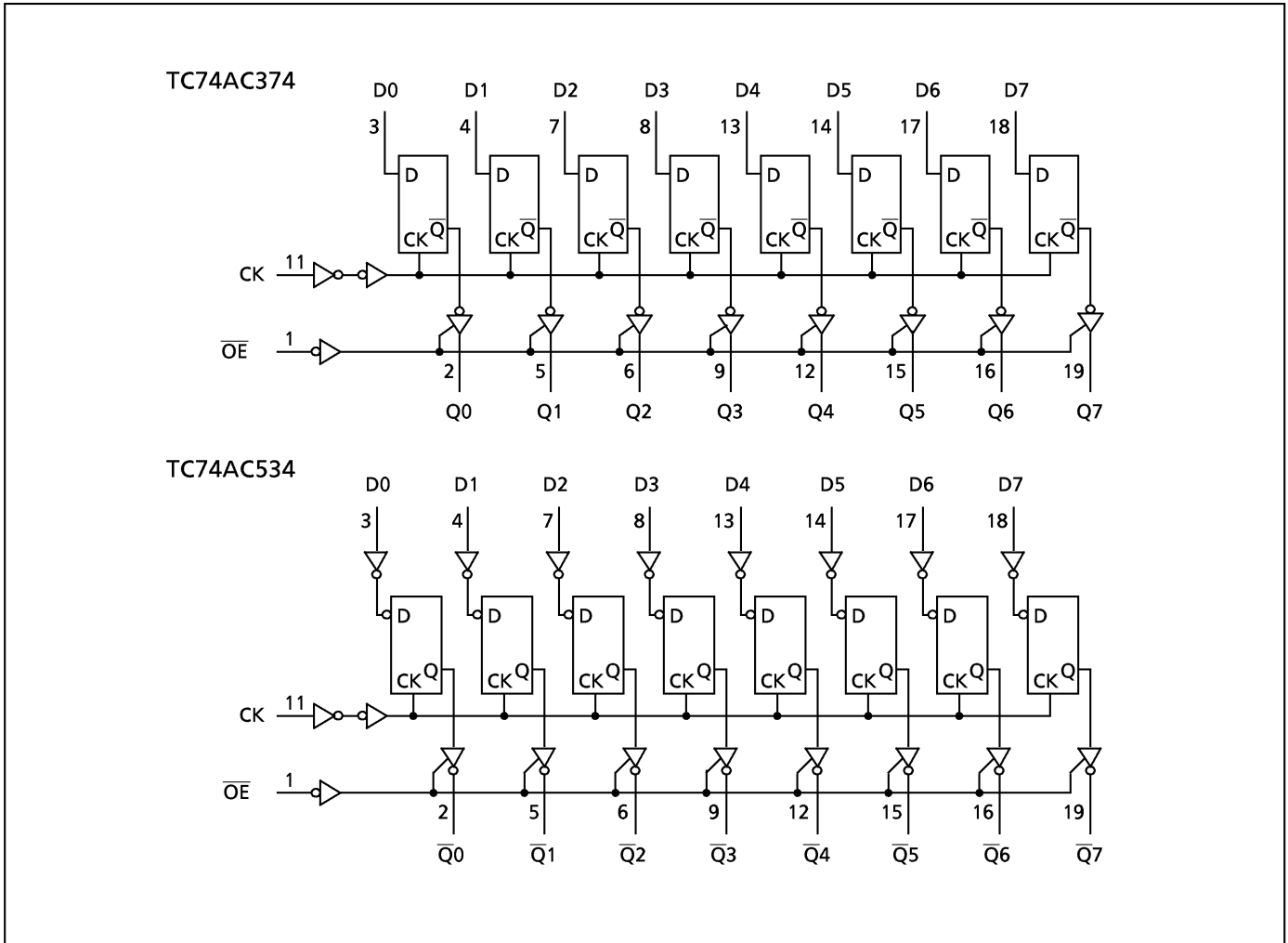
INPUTS			OUTPUTS	
\overline{OE}	CK	D	Q(374)	\overline{Q} (534)
H	X	X	Z	Z
L		X	Q_n	\overline{Q}_n
L		L	L	H
L		H	H	L

X : Don't Care
 Z : High Impedance
 $Q_n(Q_n)$: No Change

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~ $V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC} /Ground Current	I_{CC}	± 200	mA
Power Dissipation	P_D	500 (DIP)*/ 180 (SOP/TSSOP)	mW
Storage Temperature	T_{stg}	-65~150	°C

*500mW in the range of $T_a = -40^{\circ}C \sim 65^{\circ}C$. From $T_a = 65^{\circ}C$ to $85^{\circ}C$ a derating factor of $-10mW/^{\circ}C$ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	dt / dV	0~ 100 ($V_{CC} = 3.3 \pm 0.3V$) 0~ 20 ($V_{CC} = 5 \pm 0.5V$)	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^{\circ}C$			$T_a = -40 \sim 85^{\circ}C$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V_{IH}		2.0 3.0 5.5	1.50 2.10 3.85	— — —	— — —	1.50 2.10 3.85	— — —	V	
Low - Level Input Voltage	V_{IL}		2.0 3.0 5.5	— — —	— — —	0.50 0.90 1.65	— — —	0.50 0.90 1.65	— — —	V
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —	V
			$I_{OH} = -4mA$	3.0	2.58	—	—	2.48	—	
			$I_{OH} = -24mA$ $I_{OH} = -75mA^*$	4.5 5.5	3.94 —	— —	— —	3.80 3.85	— —	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\mu A$	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			$I_{OL} = 12mA$	3.0	—	—	0.36	—	0.44	
			$I_{OL} = 24mA$ $I_{OL} = 75mA^*$	4.5 5.5	— —	— —	0.36 —	— —	0.44 1.65	
3 - State Output Off - State Current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	5.5	—	—	± 0.5	—	± 5.0	μA	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	± 0.1	—	± 1.0		
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	8.0	—	80.0		

* : This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		Ta = -40~85°C		UNIT
			V _{CC} (V)	LIMIT	LIMIT	LIMIT	
Minimum Pulse Width (CK)	t _{W(H)}		3.3 ± 0.3	7.0	7.0	7.0	ns
	t _{W(L)}		5.0 ± 0.5	5.0	5.0	5.0	
Minimum Set - up Time	t _s		3.3 ± 0.3	9.0	9.0	9.0	
			5.0 ± 0.5	5.0	5.0	5.0	
Minimum Hold Time	t _h		3.3 ± 0.3	0.0	0.0	0.0	
			5.0 ± 0.5	0.0	0.0	0.0	

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF , R_L = 500Ω , Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT	
			V _{CC} (V)	MIN.	TYP.	MAX.	MIN.		MAX.
Propagation Delay Time (CK-Q, Q)	t _{pLH} t _{pHL}		3.3 ± 0.3	—	8.5	15.8	1.0	18.0	ns
			5.0 ± 0.5	—	6.1	8.7	1.0	10.0	
Output Enable Time	t _{pZL} t _{pZH}		3.3 ± 0.3	—	7.5	14.0	1.0	16.0	
			5.0 ± 0.5	—	6.1	8.7	1.0	10.0	
Output Disable Time	t _{pLZ} t _{pHZ}		3.3 ± 0.3	—	5.5	12.3	1.0	14.0	MHz
			5.0 ± 0.5	—	4.7	7.0	1.0	8.0	
Maximum Clock Frequency	f _{MAX}		3.3 ± 0.3	55	120	—	55	—	MHz
			5.0 ± 0.5	100	160	—	100	—	
Input Capacitance	C _{IN}			—	5	10	—	10	pF
Output Capacitance	C _{OUT}			—	10	—	—	—	
Power Dissipation Capacitance	C _{PD(1)}			—	37	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per F/F)}$$

And the total C_{PD} when n pcs. of F/F operate can be gained by the following equation :

$$C_{PD} \text{ (total)} = 25 + 12 \cdot n$$

DIP 20PIN PACKAGE DIMENSIONS (DIP20-P-300-2.54A)

Unit in mm



SOP 20PIN (200mil BODY) PACKAGE DIMENSIONS (SOP20-P-300-1.27)

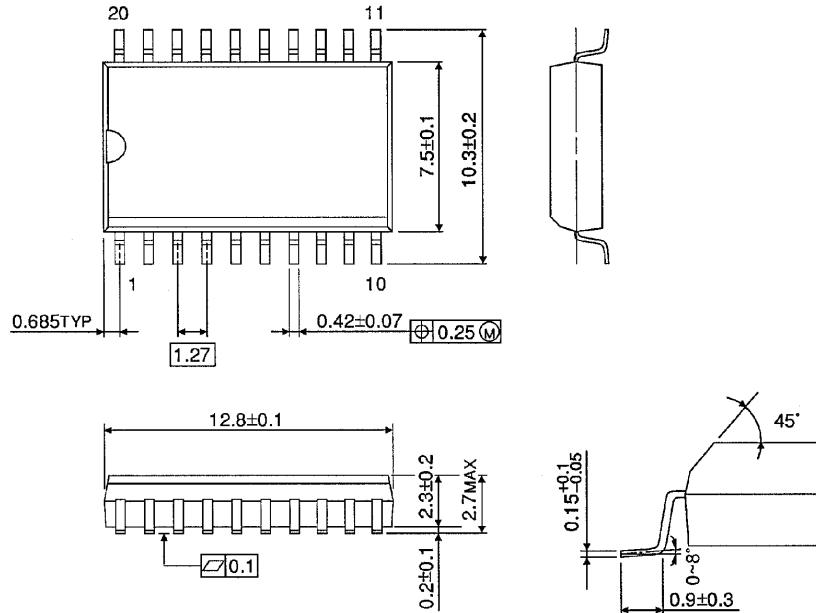
Unit in mm



SOP 20PIN (300mil BODY) PACKAGE DIMENSIONS (SOL20-P-300-1.27)

Unit in mm

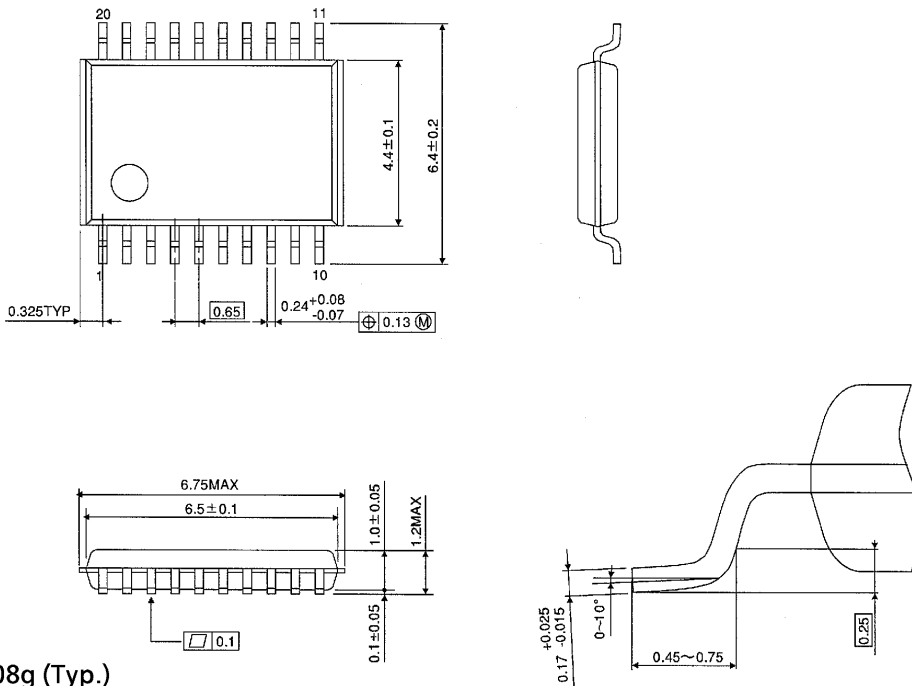
(Note) This package is not available in Japan.



Weight : 0.46g (Typ.)

TSSOP 20PIN PACKAGE DIMENSIONS (TSSOP20-P-0044-0.65)

Unit in mm



Weight : 0.08g (Typ.)

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000707EBA

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