SPLC100A1

40-CHANNEL SEG/COM LCD DRIVER

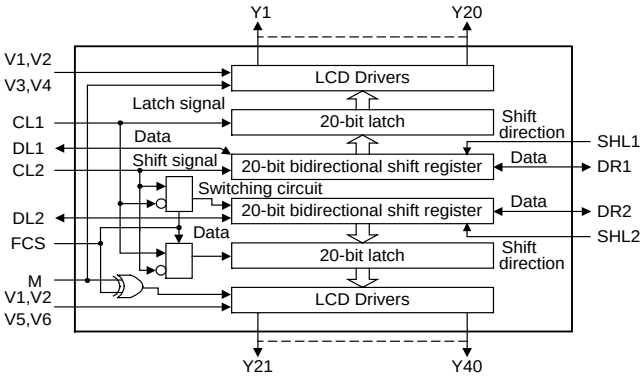
GENERAL DESCRIPTION

The SPLC100A1 is a Liquid Crystal Display driver that contains two sets of 20-bit bi-directional shift registers, 20 data latch flip-flops and 20 Liquid Crystal Display drivers. It also features 40-channel outputs that can be applied as common or segment driver. The SPLC100A1 receives serial display data from a display control LSI, converts it into parallel data and supplies liquid crystal display waveforms to the liquid crystal.

FEATURES

- Liquid Crystal Display driver with serial/parallel conversion function.
- Serial transfer facilitates board design.
- Capable of interfacing to liquid crystal display controllers: HD43160AH, HD61830, HD44780, HD44790, SPLC780
- 40 internal LCD drivers.
- Internal serial/parallel conversion circuits:
  - 20-bit shift register × 2
  - 20-bit latch × 2
- Power supply:
  - Internal logic: 2.7V – 5.5V
  - Liquid crystal display driver circuit: 3.0V – 11.0V
- CMOS process.

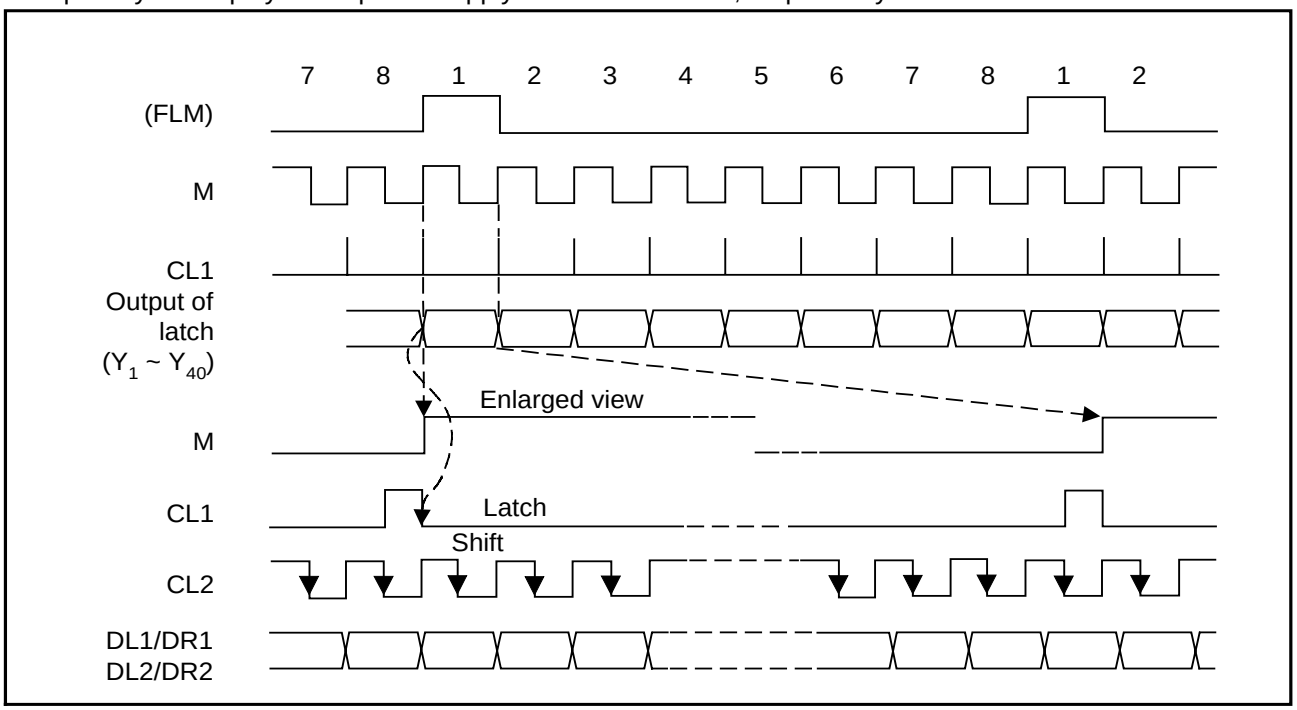
BLOCK DIAGRAM



FUNCTION DESCRIPTION

■ SEGMENT DRIVER

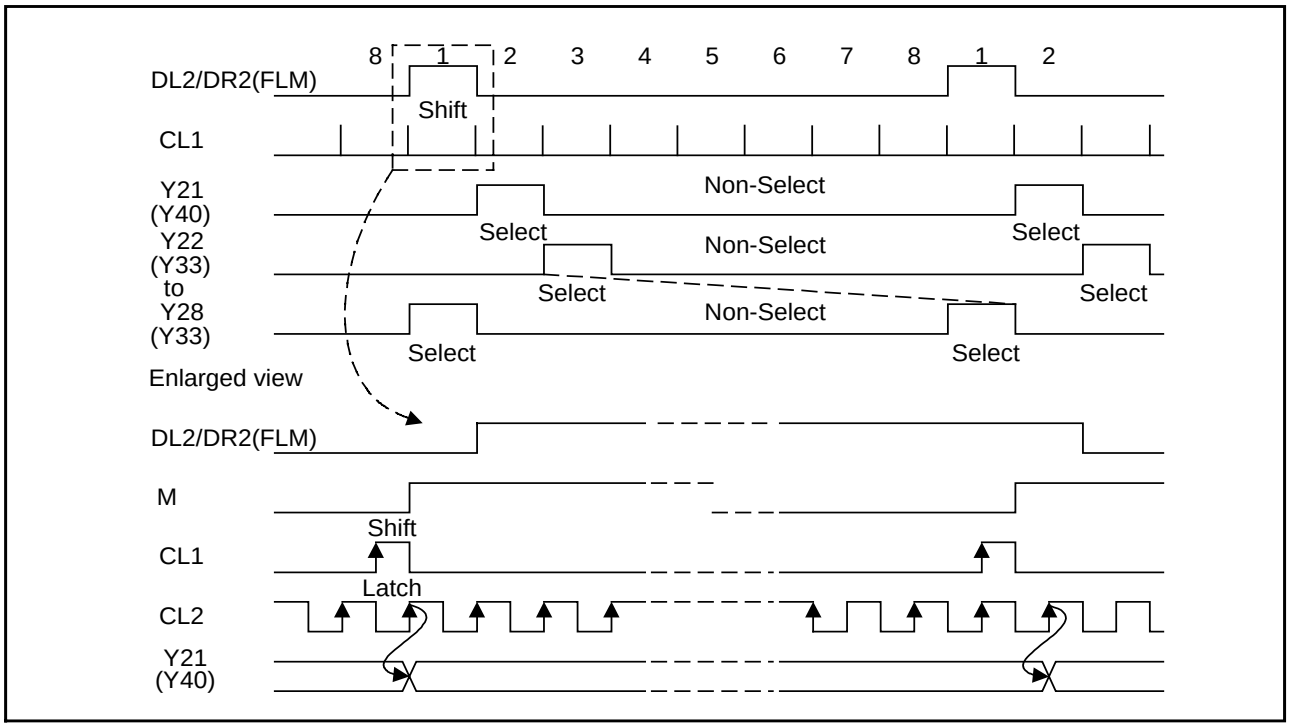
When SPLC100A1 is used as a segment driver, FCS is connected to VSS. In this case, both channel 1 and channel 2 shift data at the falling edge of CL2 and latch it at the falling edge of CL1. V3 and V5, V4 and V6 of the liquid crystal display driver power supply are short-circuited, respectively.



Segment data waveforms (A type waveforms, 1/8 duty cycle)

■ **COMMON DRIVER**

In this case, channel 1 is used as a segment driver and channel 2 as common driver. When channel 2 of SPLC100A1 is used as common driver, FCS is connected to VDD. In this case, channel 2 shifts data at the rising edge of CL1 and latches it at the rising edge of CL2.



Common data waveforms (A type waveforms of channel 2, 1/8 duty cycle)

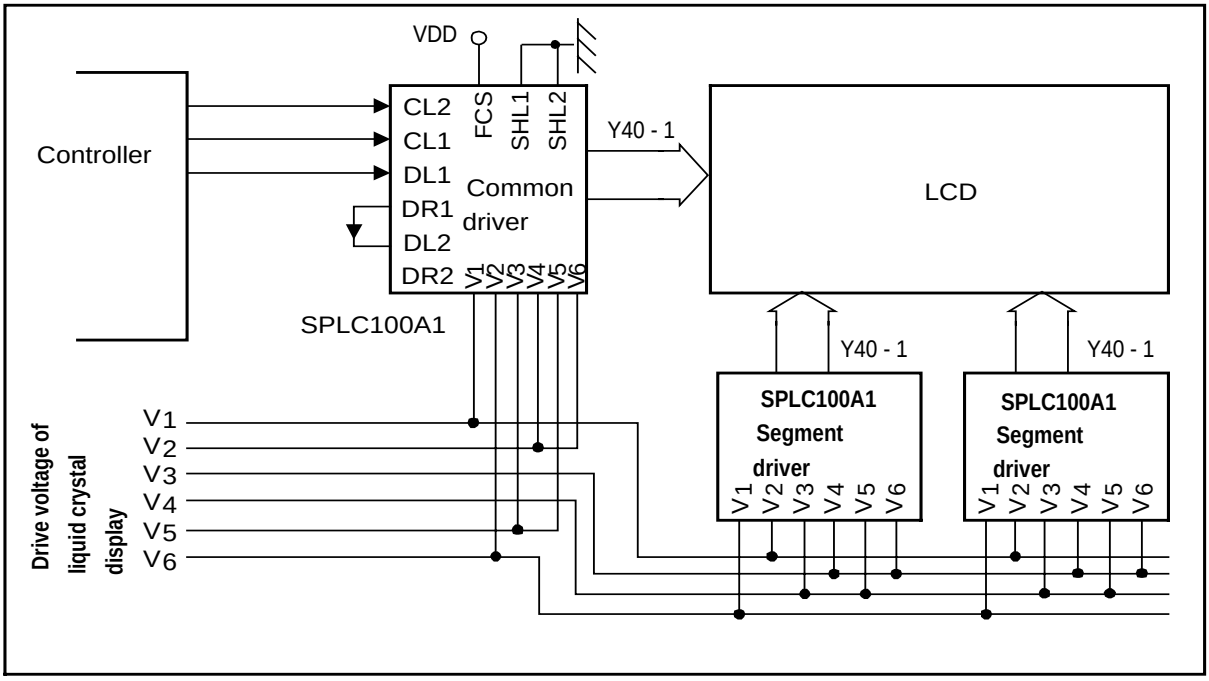
Both Channel 1 and Channel 2 Used as Common Drivers (FCS = VDD)

Common Drivers (FCS = VDD)

When both of channel 1 and channel 2 are used common drives, FCS is connected to VDD and the signals (CL1, CL2, FLM) from the controller are connected as following.

In this case, connection of the Liquid Crystal Display driver power supply is different from that of segment driver,

- V1,V2: Select level of segment and common
- V3,V4: Non-select level of segment
- V5,V6: Non-select level of common



PIN DESCRIPTION

<table>
<tr><th>Mnemonic</th><th>PIN No.</th><th>Type</th><th>Description</th></tr>
<tr><td>VDD</td><td>22</td><td>I</td><td>Positive power supply voltage input</td></tr>
<tr><td>VSS</td><td>32</td><td>I</td><td>Ground input</td></tr>
<tr><td>VEE</td><td>29</td><td>I</td><td>Power supply voltage for liquid crystal display drive</td></tr>
<tr><td>Y6 – 1
Y20 – 7</td><td>23-28
8-21</td><td>O</td><td>Liquid crystal driver output (Channel 1)</td></tr>
<tr><td>Y27 – 21
Y40 – 28</td><td>1-7
47-59</td><td>O</td><td>Liquid crystal driver output (Channel 2)</td></tr>
<tr><td>V1, V2</td><td>41,42</td><td>I</td><td>Power supply for liquid crystal display drive (Select level)</td></tr>
<tr><td>V3, V4</td><td>43,44</td><td>I</td><td>Power supply for liquid crystal display drive (Non-select level for channel 1)</td></tr>
<tr><td>V5, V6</td><td>45,46</td><td>I</td><td>Power supply for liquid crystal display drive (Non-select level for channel 2)</td></tr>
<tr><td>SHL1</td><td>38</td><td>I</td><td>Selection of the shift direction of channel 1 shift register
<table>
<tr><td>SHL1</td><td>DL1</td><td>DR1</td></tr>
<tr><td>VDD</td><td>Out</td><td>In</td></tr>
<tr><td>GND</td><td>In</td><td>Out</td></tr>
</table></td></tr>
<tr><td>SHL2</td><td>39</td><td>I</td><td>Selection of the shift direction of channel 2 shift register
<table>
<tr><td>SHL2</td><td>DL2</td><td>DR2</td></tr>
<tr><td>VDD</td><td>Out</td><td>In</td></tr>
<tr><td>GND</td><td>In</td><td>Out</td></tr>
</table></td></tr>
<tr><td>DL1, DR1</td><td>33,34</td><td>I/O</td><td>Data Input / Output of channel 1 shift register</td></tr>
<tr><td>DL2, DR2</td><td>35,36</td><td>I/O</td><td>Data Input / Output of channel 2 shift register</td></tr>
<tr><td>M</td><td>37</td><td>I</td><td>Alternated signal for liquid crystal driver output</td></tr>
<tr><td>CL1</td><td>30</td><td>I</td><td>Latch signal for channel 1 (⌐↓) *1
Used for channel 2 when FCS is GND</td></tr>
<tr><td>CL2</td><td>31</td><td>I</td><td>Shift signal for channel 1 (⌐↓) *1
Used for channel 2 when FCS is GND</td></tr>
<tr><td>FCS</td><td>40</td><td>I</td><td>Mode select signal of channel 2. FCS signal exchanges the latch signal and the shift of channel 2 and inverts M for channel 2.Thus, this signal exchanges the function of channel 2.
<table>
<tr><td rowspan="2">FCS Level</td><td colspan="2">Channel 2</td><td rowspan="2">M Polarity</td><td rowspan="2">Function</td></tr>
<tr><td>Latch signal</td><td>Shift signal</td></tr>
<tr><td>VDD</td><td>CL2 ⌐↑</td><td>CL1 ⌐↑</td><td>M</td><td>For common drive</td></tr>
<tr><td>GND</td><td>CL1 ⌐↓</td><td>CL2 ⌐↓</td><td>M</td><td>For segment drive</td></tr>
<tr><td></td><td>*1</td><td>*1</td><td></td><td>*2</td></tr>
</table></td></tr>
</table>

Notes: *1. ⌐↑ and ⌐↓ indicate the latches at rise and fall times, respectively.

*2. The output level relationship between channel 1 and channel 2 based on the FCS signal level as follows:

FCS	Data	M	Output Level	
			Channel 1(Y1 - Y20)	Channel 2(Y21 - Y40)
VDD (H)	H (Select)	H	V1	V2
		L	V2	V1
	L (Non-select)	H	V3	V6
		L	V4	V5
GND (L)	H (Select)	H	V1	V1
		L	V2	V2
	L (Non-select)	H	V3	V5
		L	V4	V6

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Ratings
Operating Voltage	V_{DD} *1	-0.3V to + 7.0V
LCD Driver Supply Voltage	V_{EE} *2	VDD - 13.5V to VDD+ 0.3V
Input Voltage 1	V_{IN1}	-0.3V to VDD + 0.3V
Input Voltage 2 (V1 - V6)	V_{IN2}	VDD + 0.3V to VEE -0.3V
Operating Temperature	T_{OPR}	-20℃ to + 75℃
Storage Temperature	T_{STG}	-55℃ to + 125℃

Note: 1.It will cause damage to IC if the supply voltage is greater than above.

2.Connect a protection resistor of 220Ω±5% to VEE.

DC CHARACTERISTICS

(VDD = 5V±10%,VEE = -5V±10%, VSS = 0V, Ta = -20 to + 75℃)

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Voltage (CL1, CL2, DL1, DL2, DR1, DR2, M, SHL1, SHL2, FCS)	V_{IH}	0.7VDD	-	VDD	V	
	V_{IL}	0	-	0.3VDD	V	
Output Voltage (DL1, DL2, DR1, DR2)	V_{OH}	VDD-0.4	-	-	V	I_{OH} = -0.4mA
	V_{OL}	-	-	0.4	V	I_{OL} = +0.4mA
LCD Driver Voltage	V_{LCD}	3.0	-	11.0	V	V_{DD} - V5
Vi-Yj Voltage Descending V(V6 - 1)-Y(Y40 - 1)	V_{D1}	-	-	1.1	V	I_{ON} = 0.1mA for one of Yj
	V_{D2}	-	-	1.5	V	I_{ON} = 0.05mA for each Yj
Input Leakage Current (CL1, CL2, DL1, DL2, DR1, DR2, M, SHL1, SHL2, FCS)	I_{IL}	-5.0	-	5.0	μA	V_{IN} = 0 to V_{DD}
Vi Leakage Current V6 - 1	I_{VL}	-10.0	-	10.0	μA	V_{IN} = V_{DD} - V_{EE} (Output Y40 - 1: floating)
Power Supply Current	I_{CC}	-	-	1.0	mA	F_{CL2} = 400KHz
	I_{EE}	-	-	10	μA	F_{CL1} = 1KHz

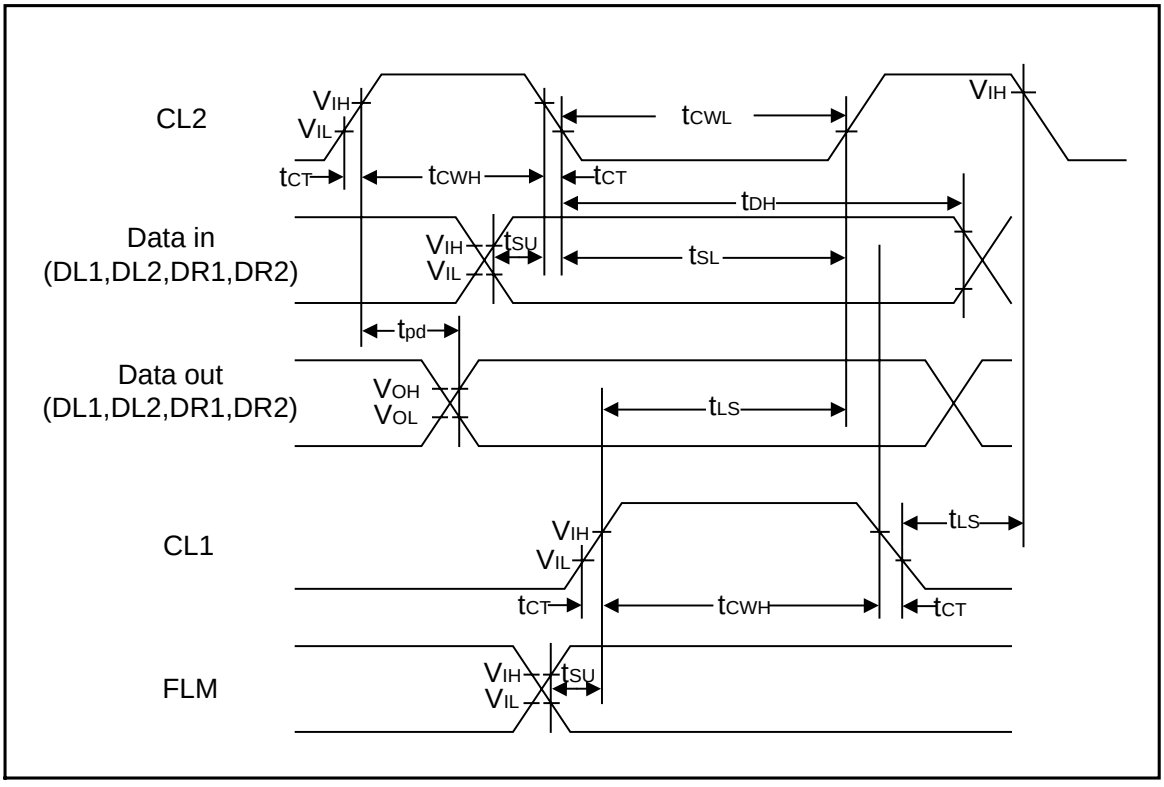
SPLC100A vs. SPLC100A1

(1) The test condition has been improved from I_{OH} = -0.35 mA (SPLC100A) to I_{OH} = -0.4mA (SPLC100A1)

(2) The minimum working voltage of SPLC100A is 4.5V. In contrast, the minimum working voltage of SPLC100A1 is improved to 3.0V.

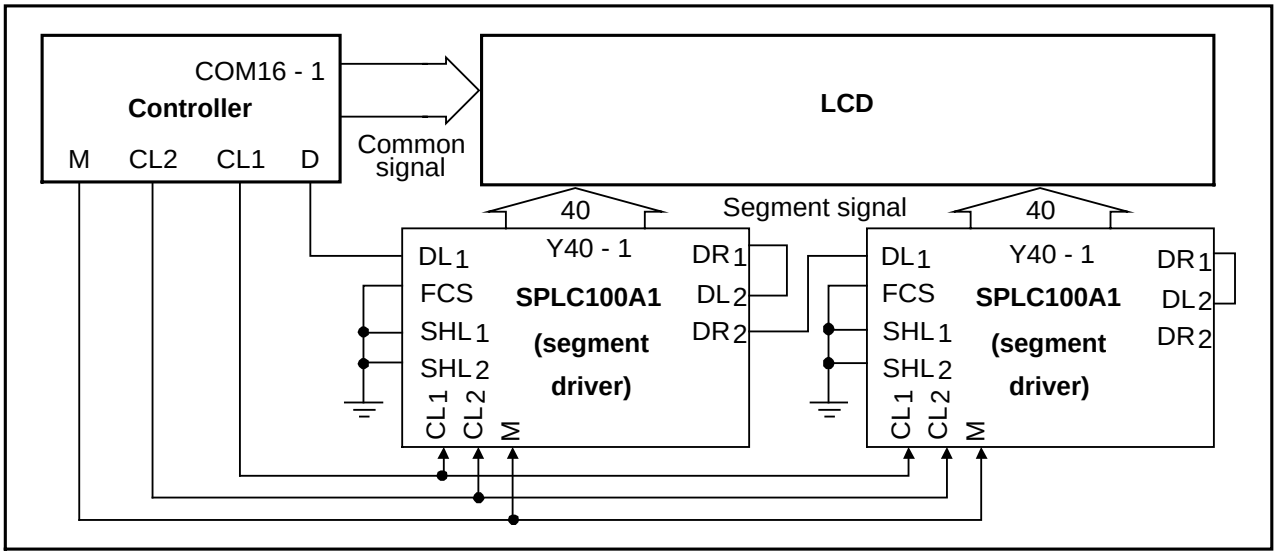
AC CHARACTERISTICS

Characteristics		Symbol	Min.	Typ.	Max.	Unit	Test Condition
Data Shift Frequency (CL2)		F_{CL}	-	-	400	KHz	
Clock Width	High Level (CL1, CL2)	t_{CWH}	800	-	-	ns	
	Low Level (CL2)	t_{CWL}	800	-	-	ns	
Data Set-up Time (DL1, DL2, DR1, DR2, FLM)		t_{SU}	300	-	-	ns	
Clock Set-up Time (CL1, CL2)		t_{SL}	500	-	-	ns	(CL2→CL1)
Clock Set-up Time (CL1, CL2)		t_{LS}	500	-	-	ns	(CL1→CL2)
Date Delay Time (DL1, DL2, DR1, DR2)		t_{PD}	-	-	500	ns	CL = 15pF
Clock Rise/Fall Time (CL1, CL2)		t_{CT}	-	-	200	ns	
Date Hold Time (DL1, DL2, DR1, DR2, FLM)		t_{DH}	300	-	-	ns	

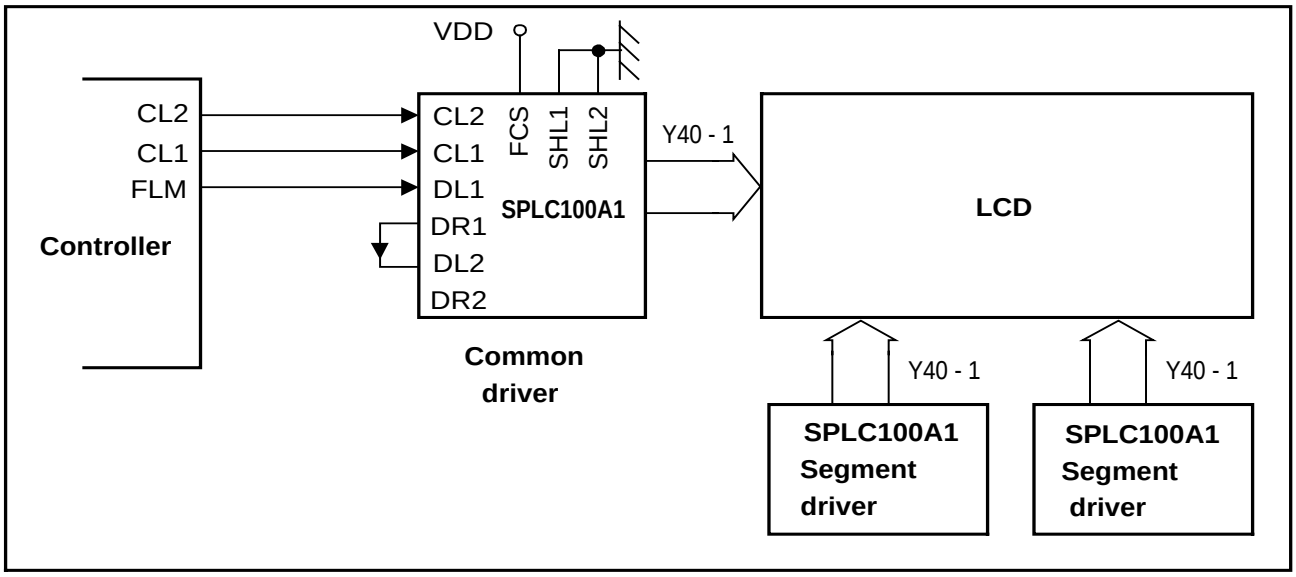


APPLICATION NOTES

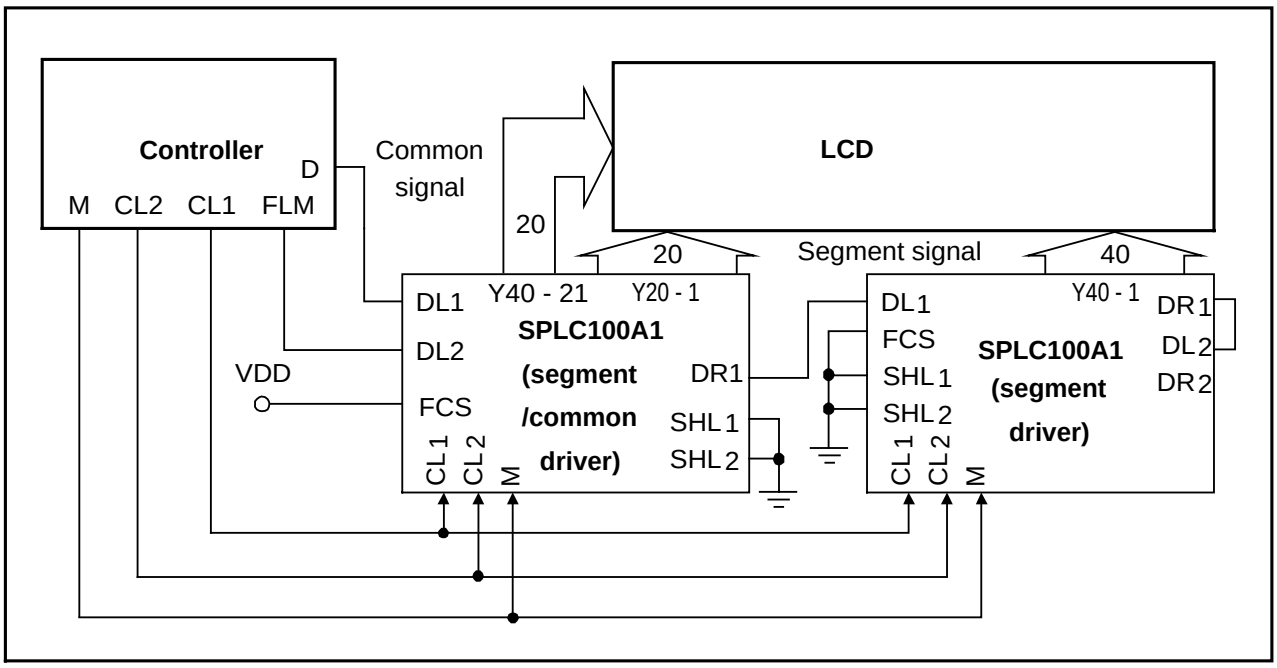
■ SEGMENT DRIVER



■ COMMON DRIVER

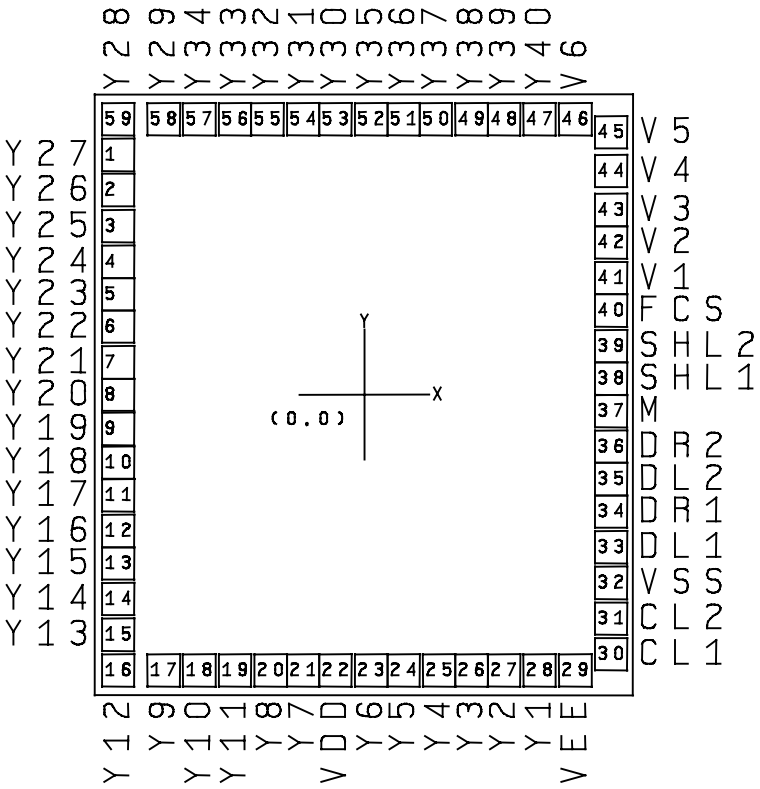


■ SEGMENT / COMMON DRIVER



PAD ASSIGNMENT AND LOCATIONS

■ PAD Assignment



Chip Size: 2152μm x 2380μm

This IC substrate should be connected to VDD

Note: To ensure IC function properly, please bond all of the VDD, VSS AVDD and AVSS pins.

Ordering Information

Product Number	Package Type
SPLC100A1-nnnnV-C	Chip form

Note1: Code number (nnnnV) is assigned for customer.

Note2: Code number (nnnn = 0000 - 9999); version (V = A - Z).

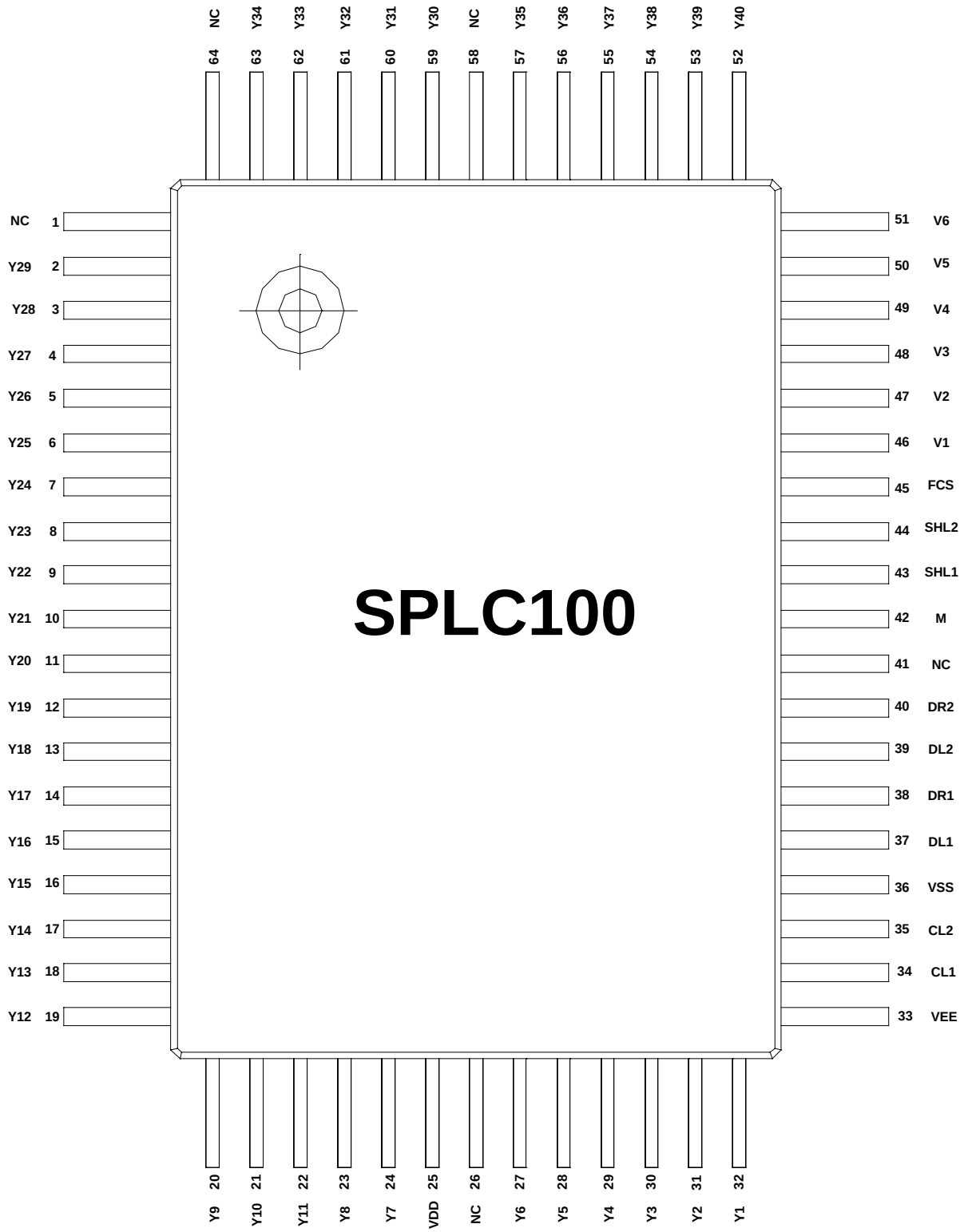
NOTE: SUNPLUS TECHNOLOGY GO., LTD reserves the right to make changes at any time without notice in order to improve the design and performance to supply the best possible product.

■ **PAD Locations**

Pad No	Pad Name	X	Y	Pad No	Pad Name	X	Y
1	Y27	-912	889	31	CL2	907	-826
2	Y26	-910	751	32	VSS	907	-690
3	Y25	-913	628	33	DL1	907	-565
4	Y24	-913	498	34	DR1	907	-434
5	Y23	-913	373	35	DL2	908	-312
6	Y22	-913	249	36	DR2	906	-188
7	Y21	-912	123	37	M	907	-63
8	Y20	-912	-2	38	SHL1	907	61
9	Y19	-912	-126	39	SHL2	907	186
10	Y18	-910	-249	40	FCS	907	309
11	Y17	-912	-373	41	V1	907	433
12	Y16	-912	-500	42	V2	907	561
13	Y15	-913	-628	43	V3	907	687
14	Y14	-912	-756	44	V4	907	825
15	Y13	-913	-891	45	V5	908	970
16	Y12	-912	-1023	46	V6	774	1020
17	Y9	-744	-1022	47	Y40	644	1021
18	Y10	-614	-1022	48	Y39	513	1021
19	Y11	-484	-1023	49	Y38	388	1021
20	Y8	-358	-1023	50	Y37	264	1022
21	Y7	-234	-1022	51	Y36	139	1021
22	VDD	-109	-1023	52	Y35	14	1022
23	Y6	16	-1023	53	Y30	-110	1021
24	Y5	139	-1023	54	Y31	-235	1022
25	Y4	265	-1022	55	Y32	-360	1021
26	Y3	390	-1023	56	Y33	-484	1021
27	Y2	513	-1023	57	Y34	-614	1022
28	Y1	642	-1023	58	Y29	-744	1022
29	VEE	772	-1023	59	Y28	-912	1022
30	CL1	908	-958				

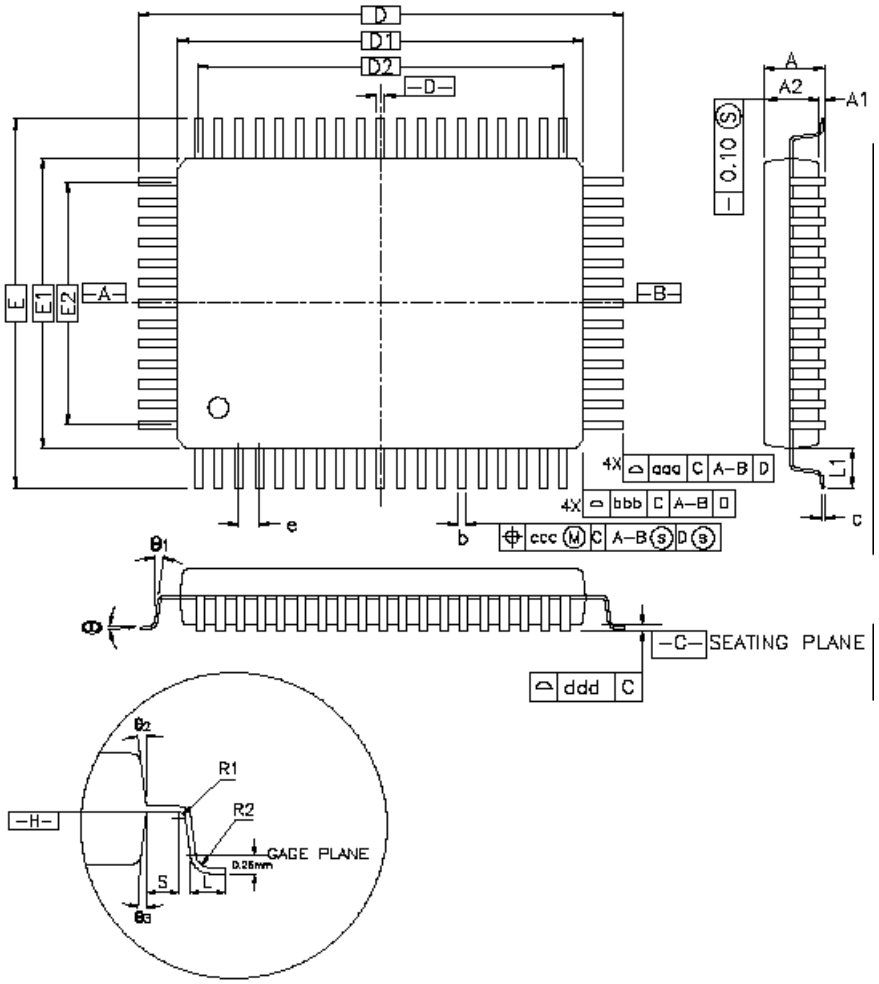
■ PACKAGE Configuration

QFP 64L Top View



■ PACKAGE Information

QFP 64L Outline Dimensions **Unit: inch/mm**



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	3.40	—	—	0.134
A1	0.25	—	—	0.010	—	—
A2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20 BASIC			0.913 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E	17.20 BASIC			0.677 BASIC		
E1	14.00 BASIC			0.551 BASIC		
R2	0.13	—	0.30	0.005	—	0.012
R1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ1	0°	—	—	0°	—	—
ALLOY 42 L/F θ2 , θ3	7° REF			7° REF		
COPPER L/F θ2 , θ3	15° REF			15° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—

SYMBOL	64L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.35	0.40	0.50	0.014	0.016	0.020
e	1.00 BSC.			0.039 BSC.		
D2	18.00 REF			0.709 REF		
E2	12.00 REF			0.472 REF		
aaa	0.25			0.010		
bbb	0.20			0.008		
ccc	0.20			0.008		
ddd	0.10			0.004		

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