

## Analog-Digital-Converter for Picture in Picture

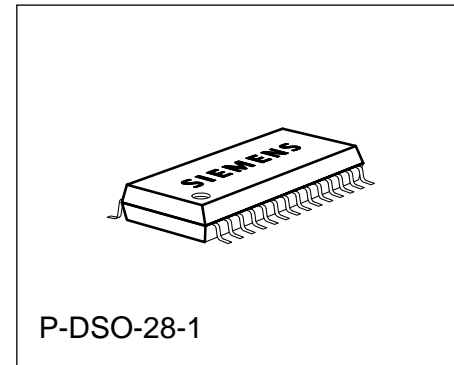
**SDA 9187-2X**

**Preliminary Data**

**MOS IC**

### Features

- 3 separate A/D-converters
- Resolution: 6 bit
- Sampling rate: 13.5 MHz, 3.375 MHz
- Clamping circuit for the input signals
- Adjustable delay for the luminance signal (8 steps)
- Color difference signals Y and V can be inverted
- Internal clock synchronization by sandcastle signal
- System clock generation for picture insertion processor



Type	Ordering Code	Package
SDA 9187-2X	Q67100-H5141	P-DSO-28-1 (300 mil)

The 9187-2X converts the analog output signals Y, U, V of any color decoder into the digital input signals of the PIP PLUS Processor SDA 9188-3X. A clock generator which is synchronized to the sync signals of the insert channel is integrated on this chip.

At the input for the channel of the inset picture an analog CVBS signal is required. An analog operating chroma decoder as well as a sync processor are generating the analog luminance- and chrominance signals Y, U, V and the horizontal and vertical sync signals of the inset picture.

Y, U and V are digitized by 6-bit flash converters and output in a format that matches the interface of the PIP-processor SDA 9188-3X. Furthermore, with the aid of PLL, the SDA 9187-2X generates the line locked clock LL3 (nominal 13.5 MHz) and the blanking signal BLN.

The luminance signal Y and the chrominance signals U, V are fed to the SDA 9187-2X by means of coupling capacitors. The color subcarrier must be filtered out of Y.

The sampling rate of the three 6-bit A/D-flash converters is the LL3 clock.

The dynamic range of the converter is the range between  $V_{REFH}$  and  $V_{REFL}$ .

The black level of Y is clamped to  $V_{REFL}$ .

The luminance information is generated as a 6-bit binary offset code. The digitized luminance signal Y can be delayed to compensate the different signal propagation times of the preceding decoder. This delay can be set in increments of two LL3 cycles in a range of 0 through 15 LL3 cycles (nominally 0 to 1.11) on pins YD0, YD1 and YD2.

The white level of U and V is clamped to  $0.5 \times (V_{REFH} + V_{REFL})$ . U, V are then converted into a 6-bit two's complement code.

The digitized U-, V-signals can be inverted via the CNEG-control input. A multiplexer selects every fourth U-, V-sample and applies this 10-bit information in four clock cycles in a nibble format to pins UV (0:3).

The horizontal PLL, consisting of a horizontal timer, phase comparator and VCO, generates the line-locked picture-in-picture system clock LL3 and the internal chip timing.

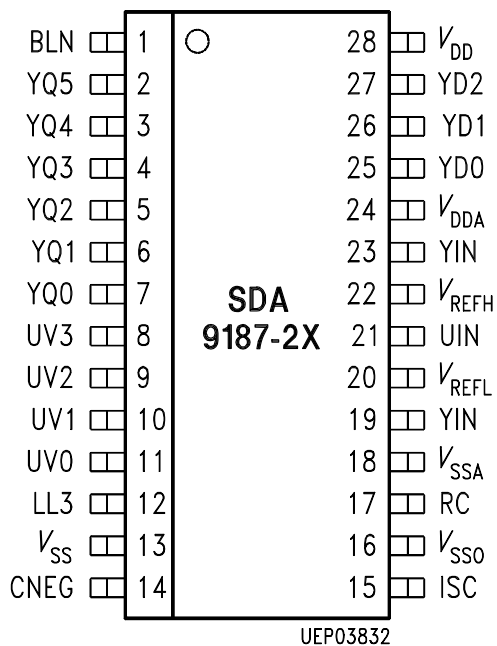
The horizontal timer divides the LL3-clock by 864 (the same for PAL and NTSC) and applies this signal as a horizontal reference signal to the phase comparator. The external horizontal signal is decoded from the sandcastle signal and matched in its pulse width (= 345 LL3-cycles) to the reference signal. The digital phase comparator is frequency- and phase-sensitive and produces current pulses at its output. The up/down pulses of the phase comparator are filtered on pin RC. The filtered signal is the control voltage of the VCO. The horizontal timer also determines the start time and the width of the clamping pulse as well as the location of the blanking signal BLN, which in turn defines the horizontal duration of the picture information on the Y output and should be synchronous with it. BLN is consequently delayed to the same degree as Y.

### Clamping

An internal clamping circuit is provided in each of the three analog channels.

The external clamping capacitance is loaded by on chip current sources during clamping (typ. 100  $\mu$ A). So the loading time depends on the values of the ext. clamping capacitor.

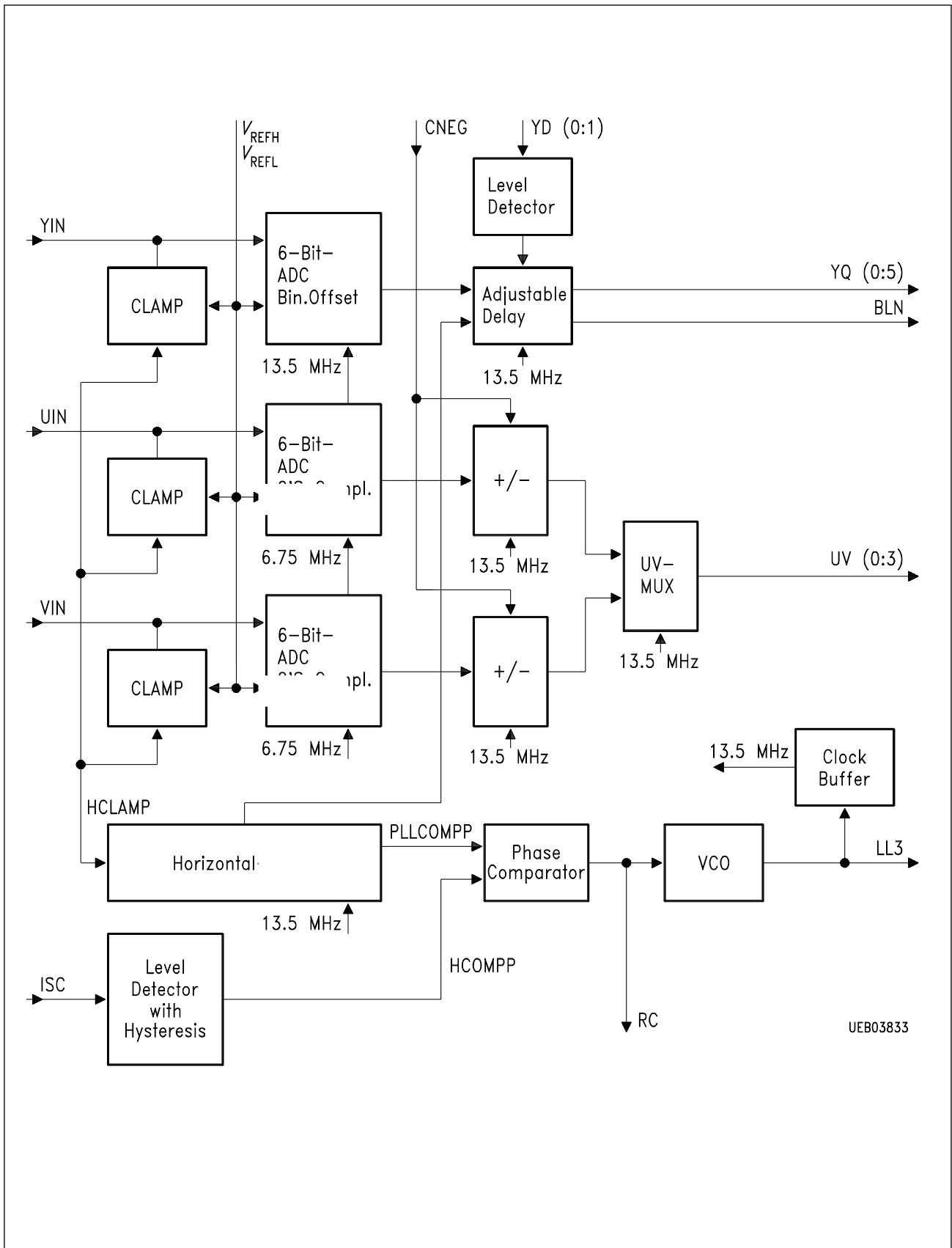
## Pin Configuration (top view)



## Pin Definitions and Function

Pin No.	Symbol	Function
1	BLN	Blanking signal output
2-7	YQ (5:0)	Digital Y-output signal (Index 0 = LSB)
8-11	UV (3:0)	Digital chrominance signal (nibble format)
12	LL3	Output of the line locked system clock (nom. 13.5 MHz)
13	$V_{SS}$	Digital ground
14	CNEG	Color negated. By H-level the chrominance signals are multiplied by $-1$ and are output. No wiring = H-level.
15	ISC	Input for the sandcastle synchronous signal of the gate signal
16	$V_{SSO}$	$V_{SS}$ connection for the oscillator
17	RC	Pin to the analog loop filter connection of the PLL
18	$V_{SSA}$	Analog ground
19	VIN	Analog input for the Y-signal
20	$V_{REFL}$	Low reference voltage for the A/D-converter
21	UIN	Analog input for the U-signal
22	$V_{REFH}$	High reference voltage for the A/D-converter
23 <sup>1)</sup>	YIN	Analog input for the Y-signal
24	$V_{DDA}$	Analog 5 V supply voltage
25, 26, 27	YD0, YD1, YD2	To adjust the Y-delay no connection = L-level
28 <sup>1)</sup>	$V_{DD}$	Digital 5 V supply voltage

<sup>1)</sup>  $V_{DD}$  must be applied before  $V_{DDA}$   
 $V_{DD}$  must not exceed  $V_{DDA}$



UEB03833

Block Diagram

## Absolute Maximum Ratings

**Note:** Maximum ratings cannot be exceeded without causing irreversible damage to the integrated circuit.

Ambient temperature  $T_A = 25\text{ °C}$  (all voltages refer to  $V_{SS}$ )

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	$V_{DD}$	- 0.3	6,5	V
	$V_{DDA}$	- 0.3	6,5	V
Voltages at I/O pins	$V_{IN}$	- 0.3	6,5	V
Voltages differences between $V_{REFH}$ and $V_{REFL}$	$\Delta V_{REF}$	- 4	4	V
Ambient temperature	$T_A$	- 20	70	°C
Storage temperature	$T_{stg}$	- 20	125	°C
Power dissipation	$P_{tot}$		0.8	W

## Operating Range

**Note:** Within the functional range, the integrated circuit operates as described; deviations from the characteristics data are possible (all voltages refer to  $V_{SS}$ )

Supply voltages	$V_{DD}$	4.5	5.5	V
	$V_{DDA}$	4.5	5.5	V
Ambient temperature	$T_A$	0	70	°C
Reference voltage <sup>1)</sup>	$V_{REFH}$	1.5	2.5	V
	$V_{REFL}$	0.5	1.5	V
Reference voltage difference	$V_{REFH} - V_{REFL}$	0.5	2	V

<sup>1)</sup> if the standard configuration is not used, additional external components are necessary (please refer to page 11, reference circuitry)

## Characteristics

**Note:** The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not stated otherwise, typical characteristics will apply at  $T_A = 25\text{ °C}$  and the listed supply voltage. (all voltages refer to  $V_{SS}$ )

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply voltages	$V_{DD}$ <sup>1)</sup>	4.5	5	5.5	V	
	$V_{DDA}$	4.5	5	5.5	V	
Current consumption	$I_{DD}$		40	80	mA	
	$I_{DDA}$		20	40		
Supply voltage differential	$V_{DDA} - V_{DD}$	0		0.5	V	

## Digital Outputs YQ (0:5), UV (0:3), BLN, LL3

Load capacitance	$C_L$	0		20	pF	
Low level	$V_{QL}$	0		0.4	V	$I_{QL} = 1.6\text{ mA}$
High level	$V_{QH}$	2.4		$V_{DD}$	V	$I_{QH} = -0.2\text{ mA}$
Delay to the positive transition of LL3	$t_d$	6	15	25	ns	LL3 = $V_{QL}$

## LL3 Pulse Form

Rise time	$t_{LL3R}$	0		7	ns	
Fall time	$t_{LL3F}$	0		5	ns	
H-pulse width	$t_{LL3H}$	28			ns	$T_{LL3} = 68\text{ ns}$
L-pulse width	$t_{LL3L}$	28			ns	$T_{LL3} = 68\text{ ns}$
LL3 period duration	$T_{LL3}$	< 68	74	< 80.6	ns	

## Digital Inputs

<b>CNEG</b>						
Low level	$V_{CNL}$			0.8	V	internal pull up for CNEG pin
High level	$V_{CNH}$	2.0			V	
Input current	$I_{CN}$			30	$\mu\text{A}$	$V_{CNH} = 5\text{ V}$

1)  $V_{DD}$  must not be applied before  $V_{DDA}$   
 $V_{DD}$  must not exceed  $V_{DDA}$

## Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
<b>YD (0, 1, 2)</b>						
Low level	$V_{YDL}$			0.8	V	internal pull down for YD0, YD1, YD2 pins
Mid level	$V_{YDM}$	2.0		$0.55 V_{DD}$	V	
High level	$V_{YDH}$	4.0			V	
Input current	$I_{YD}$			30	$\mu A$	$V_{YDH} = 5 V$

## Sandcastle Input ISC

Switching threshold for VHSC high level		$0.6 V_{DD} - 0.3 V$	$0.6 V_{DD}$	$0.6 V_{DD} + 0.3 V$		
Low level		$0.34 V_{DD} - 0.5 V^{(2)}$	$0.34 V_{DD}$	$0.34 V_{DD} + 0.5 V^{(2)}$		
Input current	$I_{SC}$	$-1 \mu A$		$1 \mu A$		$V_{SCH} = 5 V$ $V_{SCL} = 0 V$

## VCO

Frequency range		$< 12.7$	13.5	$> 14.3$	MHz	$V_{RC} = 1.0 V$ $V_{DD} = 4.5 V$ $T_A = 0 ^\circ C$
		$< 12.7$			MHz	
				$> 14.3$	MHz	$V_{RC} = 4.3 V$ $V_{DD} = 5.5 V$ $T_A = 70 ^\circ C$

## PLL Loop Filter <sup>1)</sup> (recommended value)

$R_1$			56		k $\Omega$	see application circuit
$C_1$			56		nF	
$C_2$			1		nF	

1) Design of the loop filter network of the PLL see page 14

2) Value has been increased from  $\pm 0.3 V$  to  $\pm 0.5 V$  compared to the SDA 9187X!



### Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Input capacitance	$C_{IN}$		5		pF
Leakage current at YIN, UIN, VIN				1	$\mu$ A
Start of the clamping pulse refer to the transmission of the horizontal ISC-pulse	$\tau_C$		0.5 <sup>1)</sup> 0.2 <sup>2)</sup>		$\mu$ s U/V channel $\mu$ s Y channel
Clamping pulse duration (3 pulses)	$t_{CPD}$		0.3 <sup>3)</sup>		$\mu$ s /pulse
Coupling capacitor for YIN, UIN, VIN	$C_U, C_V,$ $C_Y$		10		nF
Clamping current	$I_{clamp 1}$		100		$\mu$ A clamp level deviation > 2 LSB
	$I_{clamp 2}$		60		$\mu$ A clamp level deviation > 1 LSB < 2 LSB
	$I_{clamp 3}$		30		$\mu$ A clamp level deviation < 1LSB

### Dynamic Range of the Converter

Y-converter		0		63	
U-converter		- 31		31	
V-converter		- 31		31	

1) (= 7 LL3 period)

2) (= 3 LL3 period)

3) (= 4LL3 period)

## Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

## DC-Transfer Function of the A/D-converter

Integral non-linearity <sup>1)</sup>		- 1 LSB		1 LSB		$V_{REFH} = 2.0 \text{ V}$
Differential non-linearity <sup>1)</sup>		- 0,5 LSB		0.5 LSB		$V_{REFL} = 1.0 \text{ V}$

## Reference Voltage

$V_{REFH}, V_{REFL}$

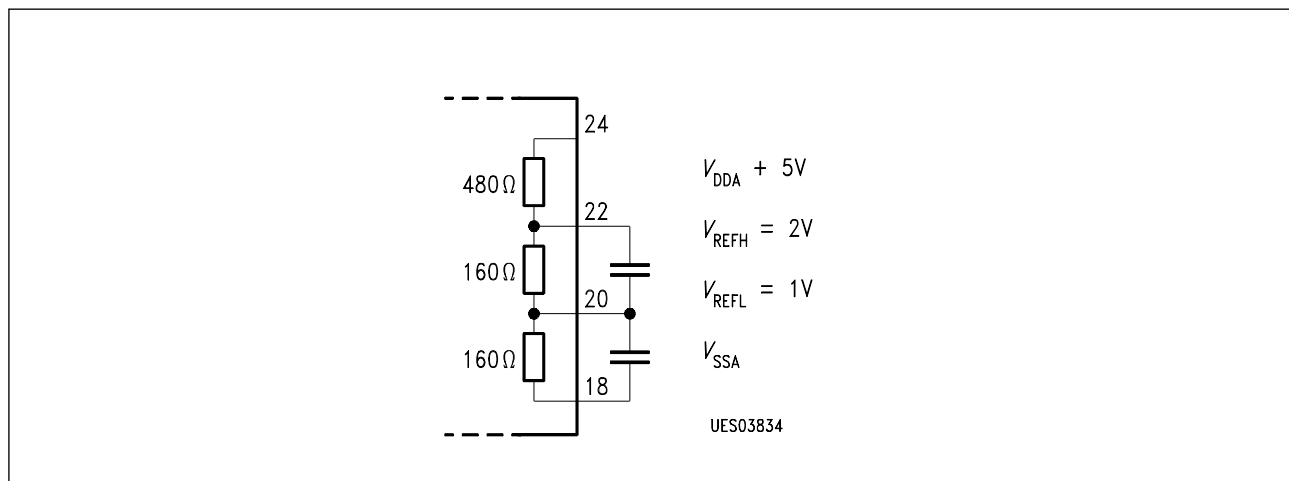
$V_{REFH}$		1.5	2.0	2.5	V	
$V_{REFL}$		0.5	1.0	1.5	V	

- 1) The absolute tolerance of the coupling level and the converter characteristic line are not influenced by the difference  $V_{REFH} - V_{REFL}$  (dynamic range of the converter). This increases the relative errors when  $V_{REFH} - V_{REFL} < 1 \text{ V}$ .

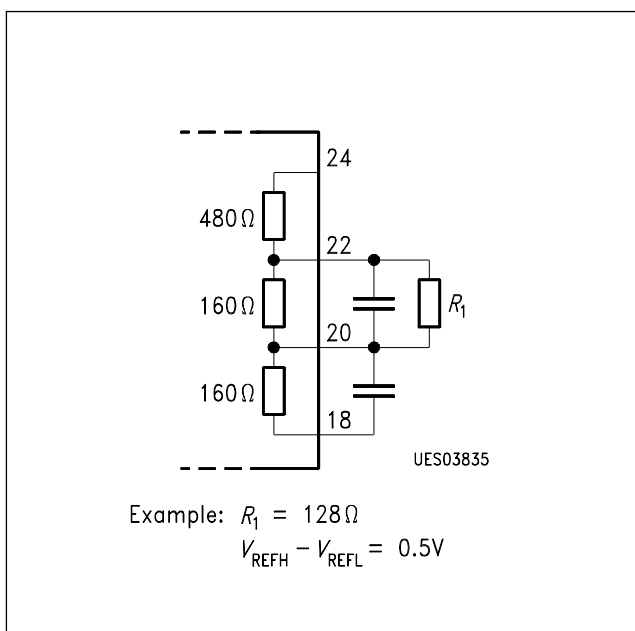
## Reference Circuitry

For the standard input signal ( $Y, U, V = 1 \text{ Vpp}$ ) the reference voltage is generated internally (**figure 1**).

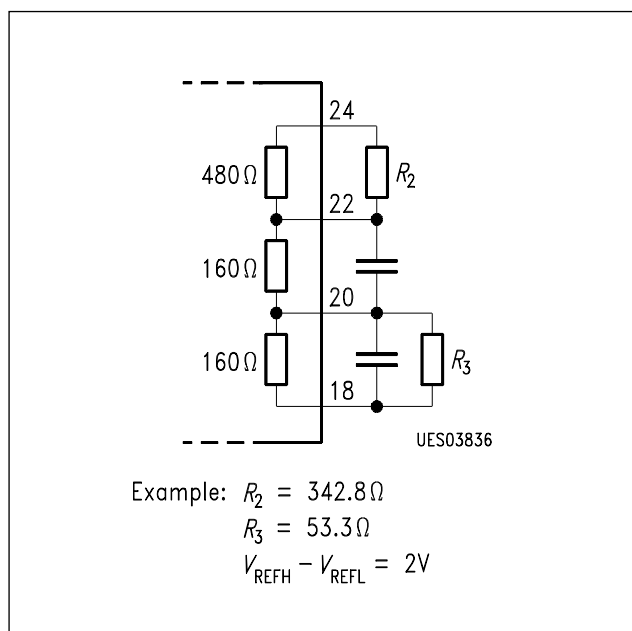
For all the other cases with input signals bigger or smaller than 1 Vpp the adjustment of the reference range can be done via an external resistor circuit (**figure 2, 3**).



**Figure 1**



**Figure 2**



**Figure 3**

the absolute tolerance of internal resistors is  $\pm 20\%$   
 the relative tolerance of internal resistors is  $\pm 2\%$

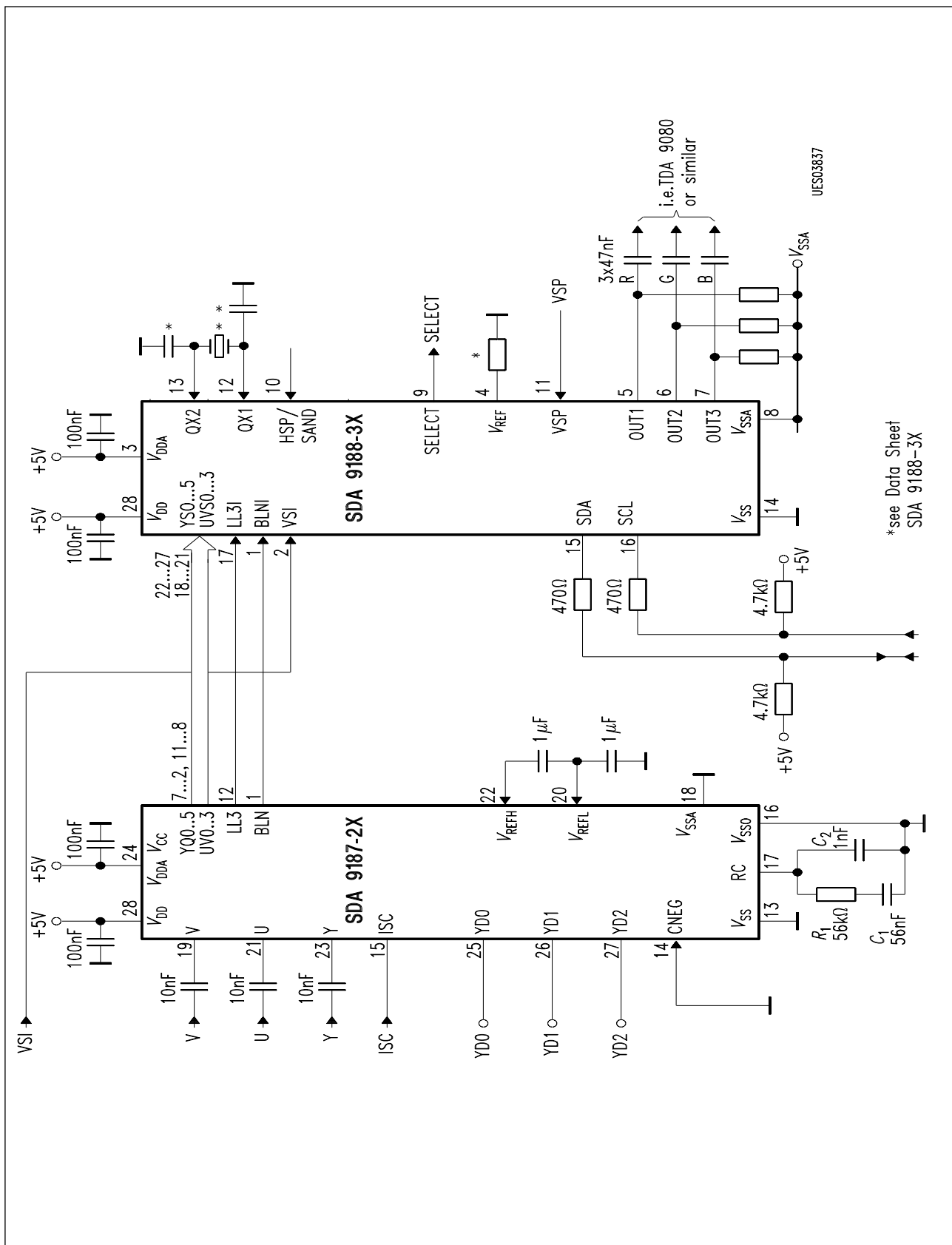
**Clamping**

For each analog channel there is an internal clamping circuit.

Analog inputs YIN, UIN and VIN are pulled to internally generated clamping levels. The clamping signals necessary for this are also generated internally (**see Fig. 7**).

Clamping levels:	Analog signal	Binary Code
	YIN	0 0 0 0 0 0
	UIN, VIN	1 0 0 0 0 0

The external clamping capacitor is charged to the appropriate clamping level every line for 42 CLK cycles by internal current sources.



\*see Data Sheet  
SDA 9188-3X

**Application Circuit**

## Design of the Loop Filter Network

For the calculation of the control response the following formulas can be applied.

Characteristic circuit frequency:

loop bandwidth

$$\omega_0 = (K/C_1)^{0.5}$$

damping factor

$$\zeta = 0.5 \times R \times (K \times C_1)^{0.5}$$

K = 0.52 typical

K = 0.75 maximum

The parallel capacitance  $C_2$  should not exceed 5 % of  $C_1$ .

Because of the discrete detection of the phase differences every 64  $\mu\text{s}$ , phase modulation of half the line frequency is superimposed on the transient response of the PLL. To make sure that this phase modulation is damped sufficiently.

$$1.74 > R_1 \times 47 \times 10^{-6} \times 1/\Omega \times (1 - 2 / (1 + e^{\alpha}))$$

with

$$\alpha = 64 \mu\text{s} / (R_1 \times C_2)$$

or approx. by

$$R_1 \times C_2 \ll 64 \mu\text{s}$$

$$1.74 > R_1 \times 47 \times 10^{-6} \times 1/\Omega$$

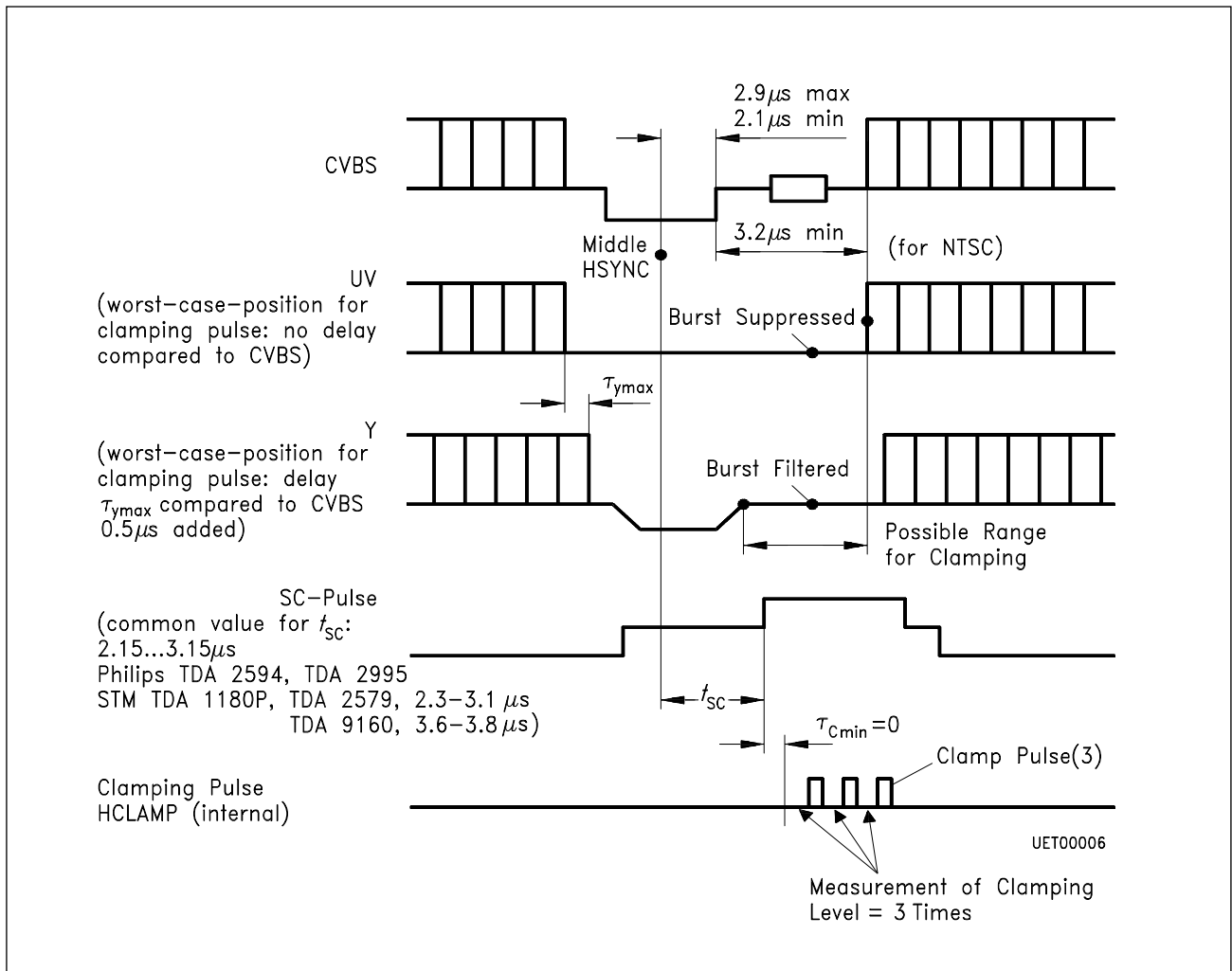
For the board layout it is important to

- a) block supply lines near the supply pins,
- b) keep the wiring of C2 short.



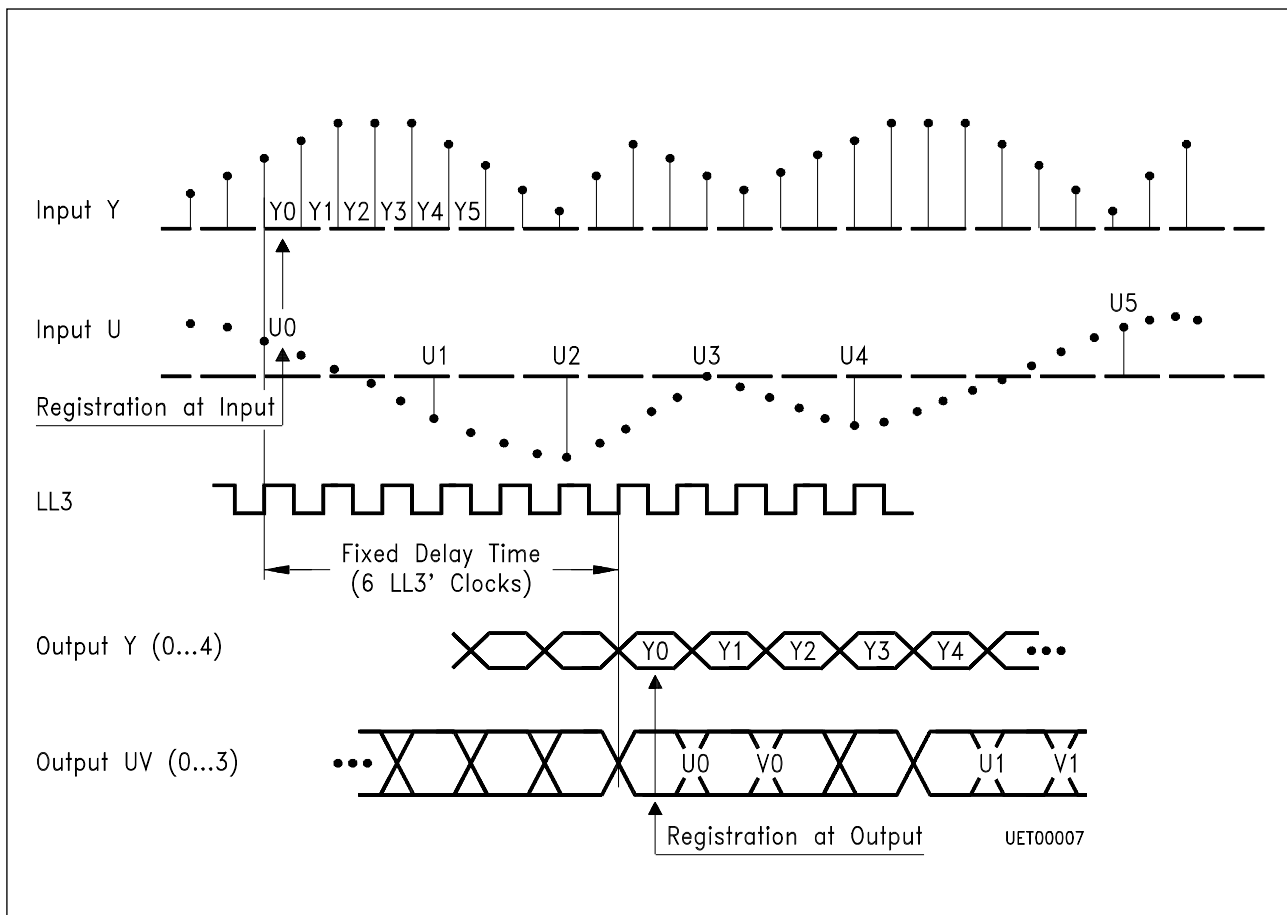
**Pulse Diagram**

Input Voltage Range of Y, U, and V and their Translation in Initial Values ("Digital Values")



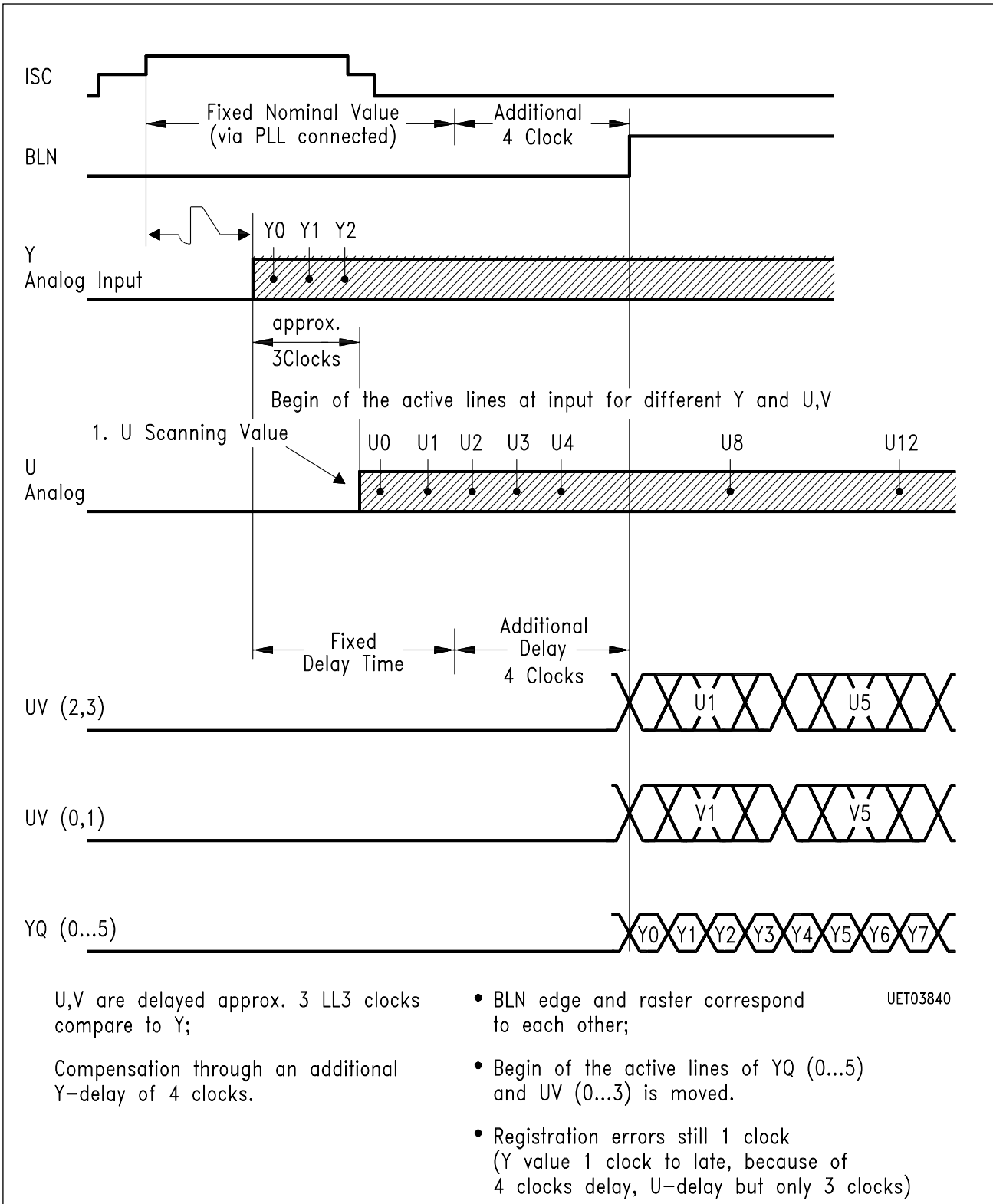
Clamping Pulse Timing





**Signal Delay Time for U, V and Y**  
(used indication: number of scanning values).

Additionally programmable delay time in DELAY-Block-0.

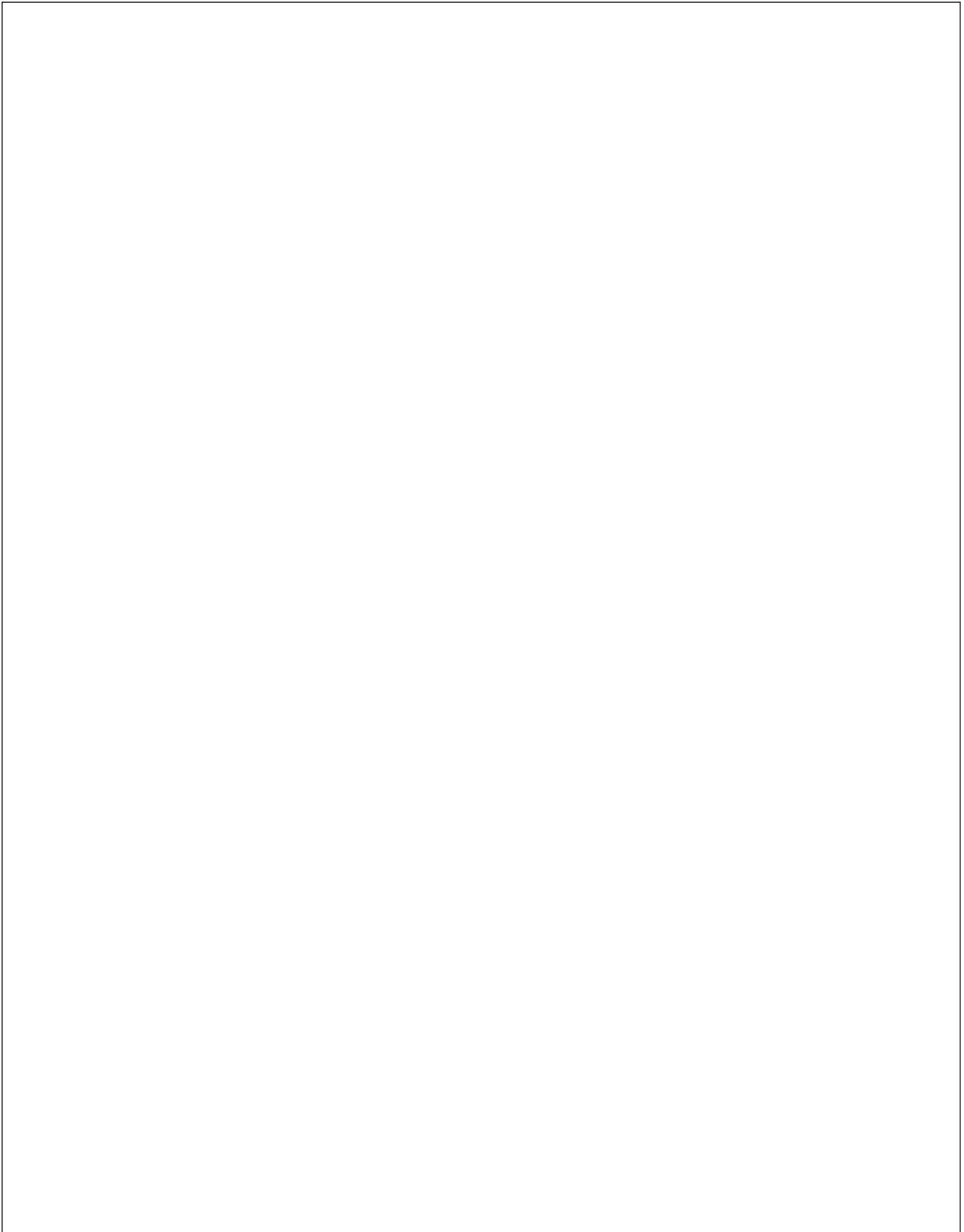


**Relation between SC, BLN and Y and UV**

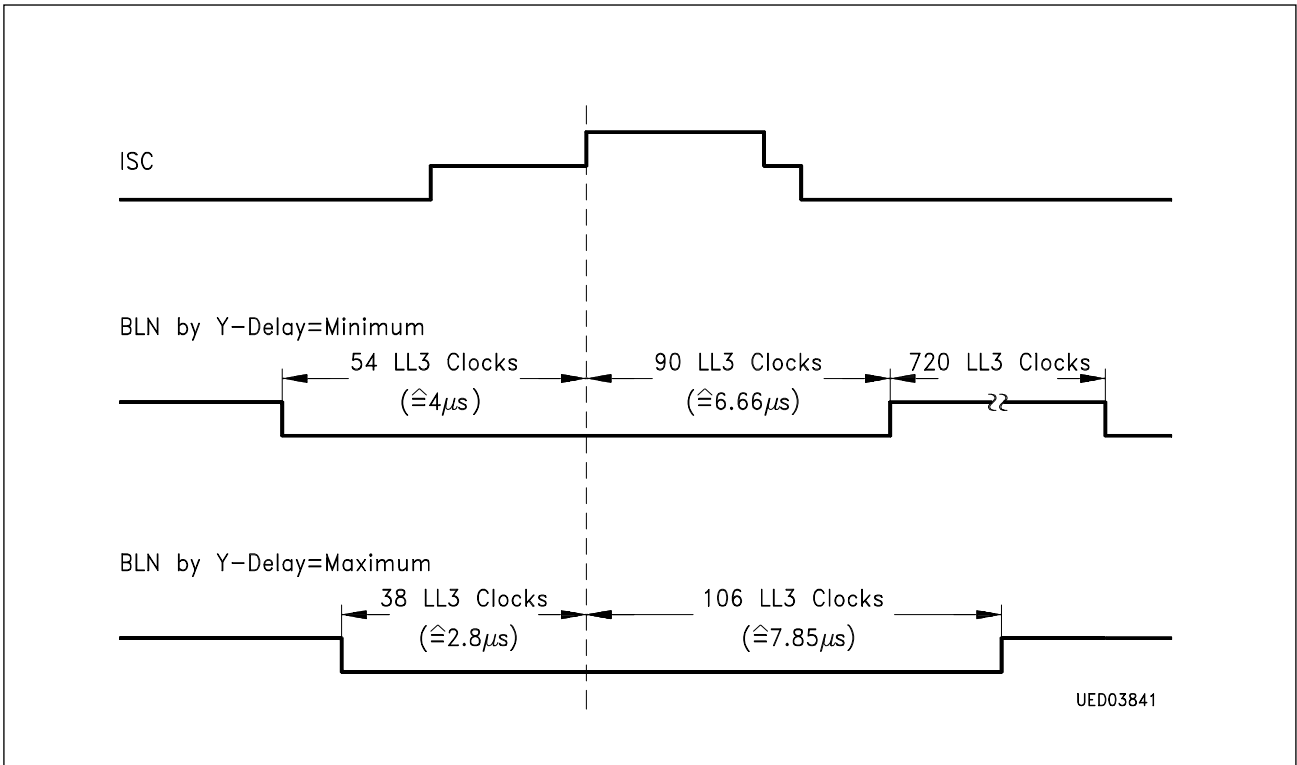
(used indication: number of pixels)

– Y, U, V have no delay time differences.

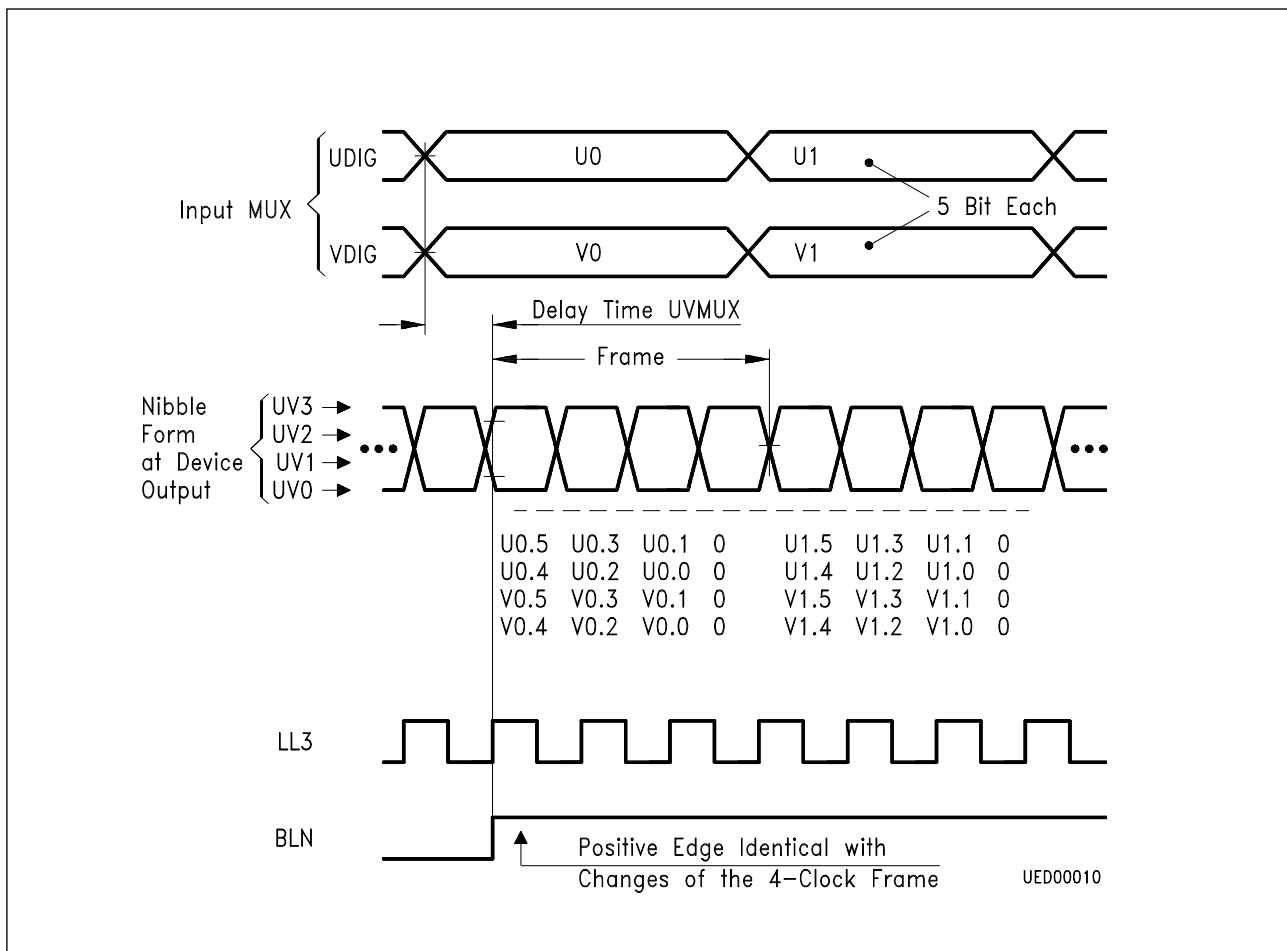
– Delay between SC and Y, U, V is smaller than provided for the optimal case.



**Relation between SC, BLN and Y and UV**  
(used indication: number of pixels)

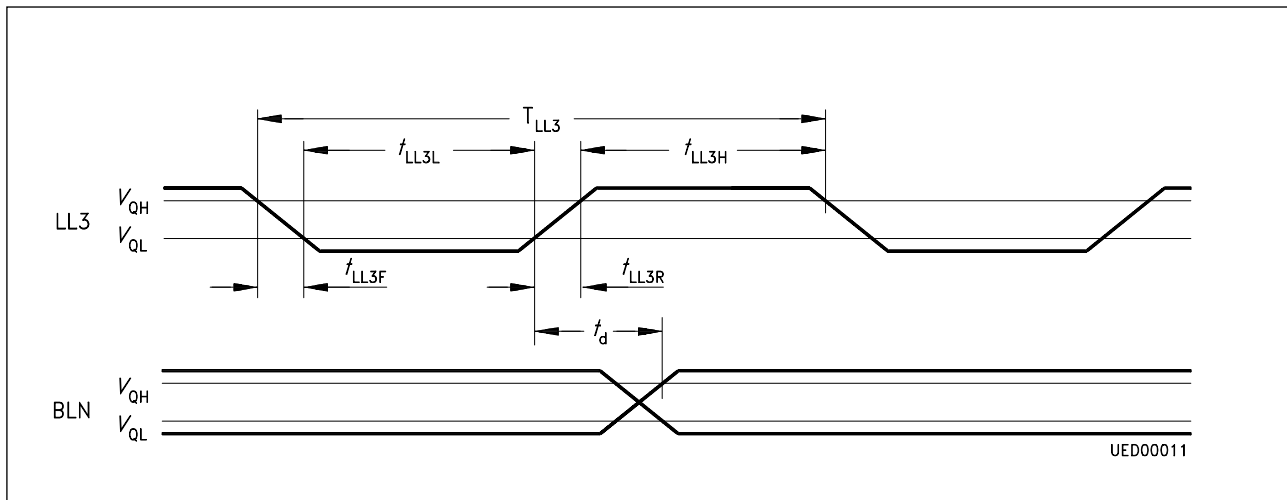


Relation between SC and BLN

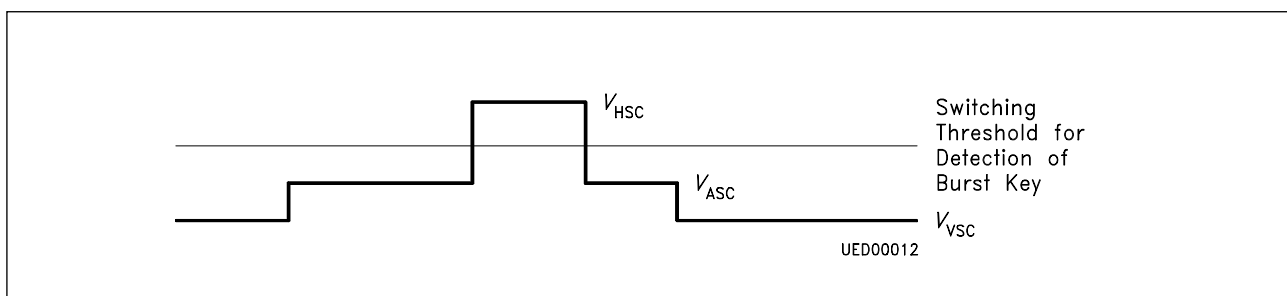


**Conversion of U and V in a Nibble Form with 13.5 MHz, 4 Bit**

- It means:
1. index: number of scanning value (pixels)
  2. index. number of bits; 5 = MSB



**Specification of Edges**



**Sandcastle Pulse**

**Adjusting of Y-Delay via YD0, YD1, YD2**

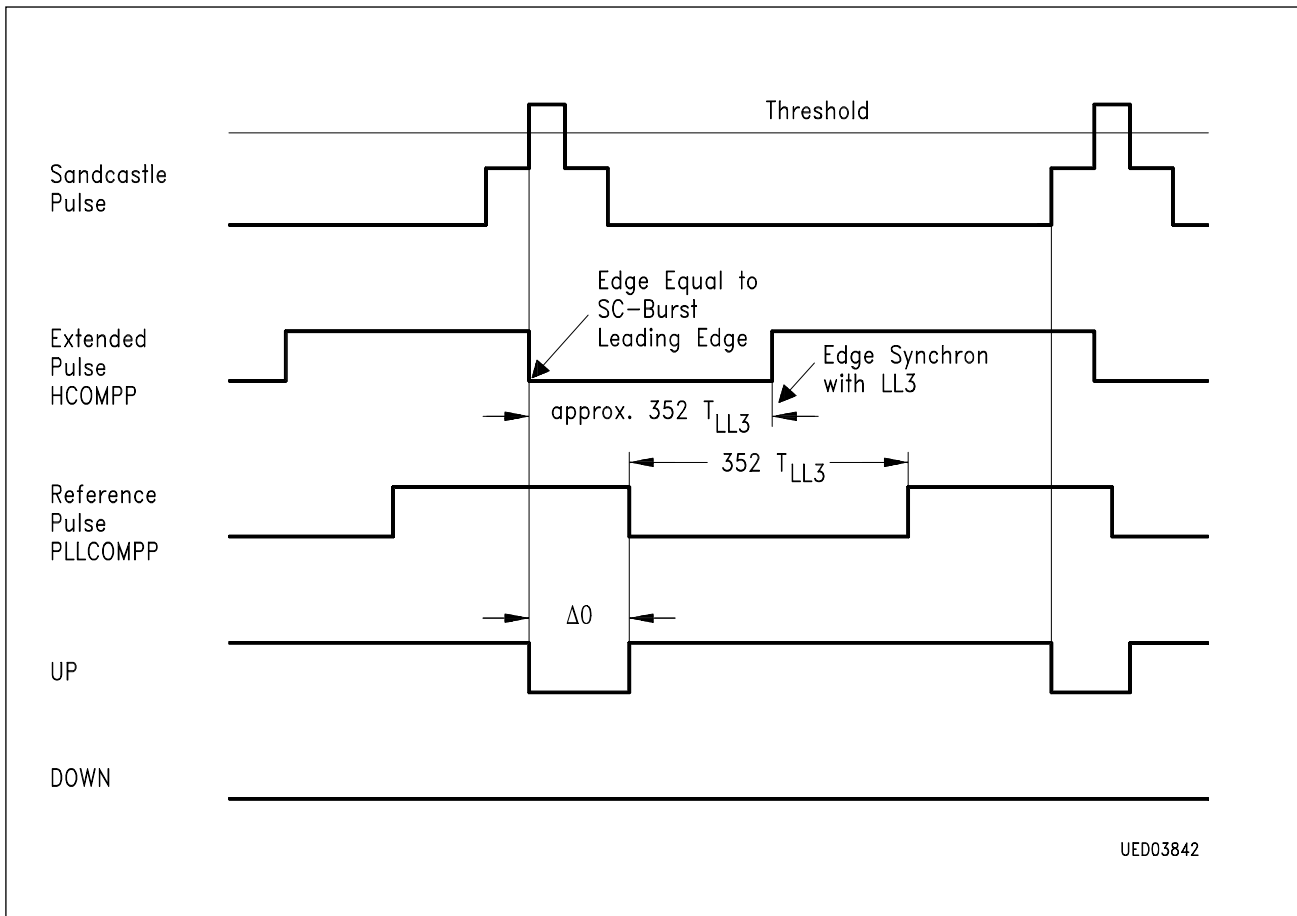
Level Range			Additional Delay for Y and BLN	
Pin YD2	Pin YD1	Pin YD0	LL3 clocks	typ. value
0	0	0	0	0
0	0	1	2	148 ns
0	1	0	4	296 ns
0	1	1	6	444 ns
1	0	0	8	592 ns
1	0	1	10	740 ns
1	1	0	12	888 ns
1	1	1	14	1.04 μs

No connection of YD0, YD1, YD2 = L-level!

Level range:

0 =  $V_{YDL}$

1 =  $V_{YDH}$



**Function of SC-Pulse Extention and Phase Comparison**  
 (PLL is unlocked, behind the external H-phase)