1 PRODUCT OVERVIEW

OVERVIEW

The S3C72E8/P72E8 is a SAM47 core-based 4-bit CMOS single-chip microcontroller. It has a timer/counter and LCD drivers.

The S3P72E8 is especially suited for use in data bank, telephone and LCD general purpose.

It is built around the SAM47 core CPU and contains ROM, RAM, 39 I/O lines, programmable timer/counter, buzzer output, enough LCD dot matrix, and segment drive pins.

The S3C72E8/P72E8 can be used for dedicated control functions in a variety of applications, and is especially designed for multi data bank, telephone and LCD game.

OTP

The S3C72E8 microcontroller is also available in OTP (One Time Programmable) version, S3P72E8. S3P72E8 microcontroller has an on-chip 8 K-byte one-time-programable EPROM instead of masked ROM. The S3P72E8 is comparable to S3C72E8, both in function and in pin configuration.

FEATURES SUMMARY

Memory

- 8192 × 8 bit program memory
- 5120 × 4 bit data memory in S3C72E8
- 108 x 5 bit display memory

39 I/O Pins

- Input: 6 pins
- I/O: 17 pins
- Output: maximum 16 pins for 1-bit level output (sharing with segment driver outputs)

8-Bit Basic Timer

- Four internal timer functions

8-Bit Timer/Counter 0

- Programmable 8-bit timer
- External event counter
- Arbitrary clock frequency output
- External clock signal divider

Watch Timer

- Time interval generation: 0,5ms, 3,9ms at 32768Hz
- 4 frequency (2/4/8/16 kHz) outputs to BUZ pin

Interrupts

- Three external vectored interrupts: INT0, INT1, INTP0
- Two internal vectored interrupts: INTB, INTT0
- Two quasi-interrupts: INTW, INT2

Memory Mapped I/O Structure

LCD Display

- 12 characters dot matrix display (5 x 7)
- 12 digit display (8 segments)
- 60 segments and 9 common pins

Power-Down Modes

- Idle mode (only CPU clock stops)
- Stop mode (Main-System clock and CPU clock stops)

Oscillation Sources

- Crystal, ceramic, or External RC for system clock
- Main-system clock frequency: 0.4 MHz - 6MHz
- Sub-system clock frequency: 32,768kHz
- CPU clock divider circuit (by 4,8, or 64)

Instruction Execution Times

- 0.67, 1.33, 10.7 µs at 6MHz
- 0.95, 1.91, 15.3 µs at 4.19 MHz
- 122 µs at 32.768 kHz

Operating Temperature

- -45 °C to 85 °C

Operating Voltage Range

- 1.8 V to 5.5 V

Package Type

- 100-pin QFP Package

BLOCK DIAGRAM

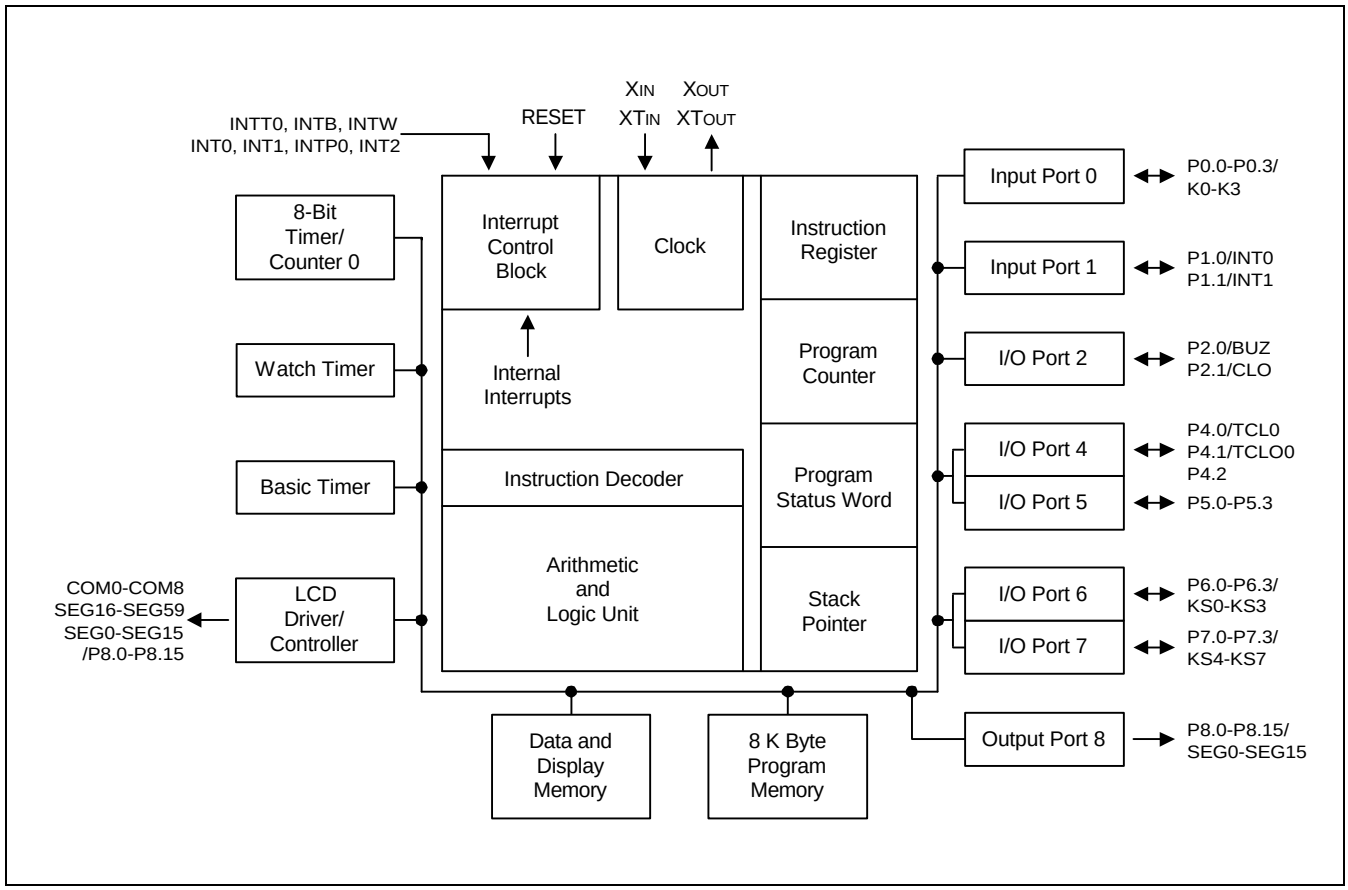


Figure 1-1. S3C72E8/P72E8 Specified Block Diagram

PIN ASSIGNMENTS

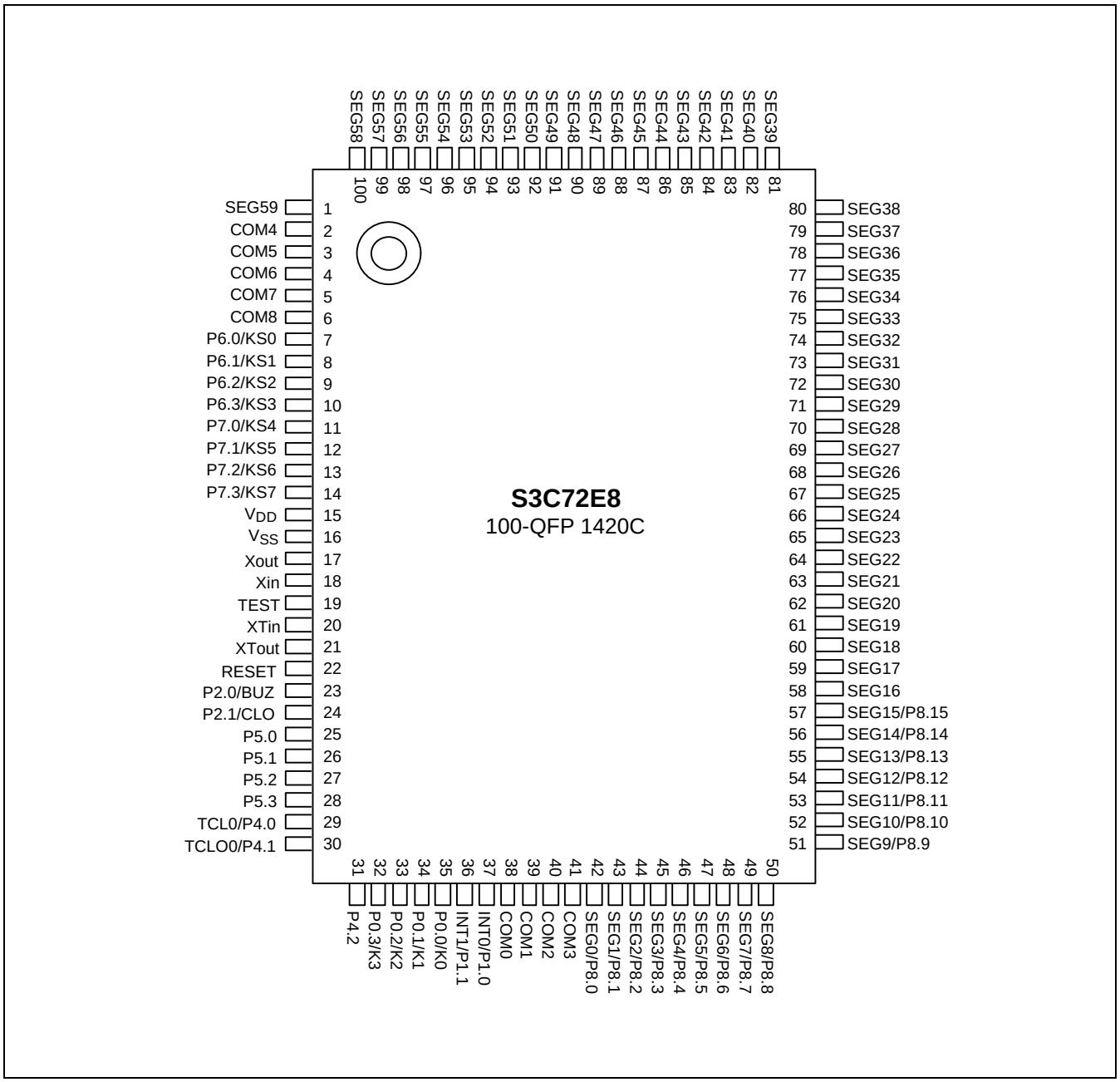


Figure 1-2. S3C72E8 Pin Assignment Diagram

PIN DESCRIPTIONS

Table 1-1. Pin Descriptions

Pin Name	Pin Type	Description	Circuit Type	Pin Number	Share Pin
P0.0 - P0.3	I	4-bit input port. 1 and 4-bit read, and test are possible. Pull-up registers.	A-1	35-32	K0-K3
P1.0 P1.1	I	2-bit Input port. 1 and 4-bit read, and test are possible, 2-bit pull-up resistors are assignable by software.	A-3	37 36	INT0 INT1
P2.0 P2.1	I/O	2-bit I/O port. 1 and 4-bit read/write, and test are possible. Each individual pin can be specified as input or output. 2-bit pull-up resistors are assignable by software. Pull-up resistors are automatically disabled for output pins.	D	23 24	BUZ CLO
P4.0 P4.1 P4.2 P5.0 - P5.3	I/O	4-bit I/O port. 1, 4, and 8-bit read/write, and test are possible. 4-pin unit can be specified as input or output. 4-bit pull-up resistors are assignable by software. Pull-up resistors are automatically disabled for output pins. Individual pins are software configurable as open-drain or push-pull output.	E E-1 E-1 E-1	29 30 31 25-28	TCL0 TCLO0
P6.0 - P6.3	I/O	4-bit I/O port. 1, 4,and 8-bit read/write, and test are possible. Each individual pin can be specified as input or output. 4-bit pull-up resistors are assignable by software. Pull-up resistors are automatically disabled for output pins.	D-1	7-10	KS0 - KS3
P7.0 - P7.3		4-bit I/O port. 1, 4, and 8-bit read/write, and test are possible. 4-pin unit can be specified as input or output. 4-bit pull-up resistors are assignable by software. Pull-up resistors are automatically disabled for output pins.		11-14	KS4 - KS7
P8.0 - P8.15	O	4-bit controllable output. (Dual function as segment output pins)	H-9	42-57	SEG0 - SEG15
SEG16-SEG59		LCD segment display signal output.	H-10	58-100 ,1	-
SEG0 - SEG15		LCD segment display signal output.	H-9	42-57	P8.0 - P8.15
COM0 - COM8		LCD common signal output.	H-11	38-41 2-6	-
INT0 - INT1	I	External interrupts. The triggering edge for INT0, and INT1 is selectable		37-36	P1.0 -P1.1
KS0 - KS7	I/O	Quasi-interrupt input for falling edge detection.		7-14	P6.0 - P7.3
K0 - K3	I	Vector interrupt input K0 - K3: falling edge detection		35-32	P0.0 - P0.3

Table 1-1. Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Circuit Type	Pin Num.	Share Pin
BUZ	I/O	2,4,8 kHz or 16kHz frequency output for buzzer signal.	-	23	P2.0
CLO		Clock output	-	24	P2.1
X_{in}, X_{out}	-	Crystal, ceramic or RC oscillator pins for main system clock.	-	18, 17	-
XT_{in}, XT_{out}	-	Crystal oscillator pins for sub-system clock.	-	20, 21	-
TCL0	I/O	External clock input for Timer/Counter 0	-	29	P4.0
TCLO0	I/O	Timer/Counter 0 clock output	-	30	P4.1
RESET	I	Reset input (active low).	B	22	-
V_{DD}	-	Power supply.	-	15	-
V_{SS}	-	Ground.	-	16	-
TEST	I	Test input: it must be connected to V_{SS}	-	19	-

PIN CIRCUIT DIAGRAMS

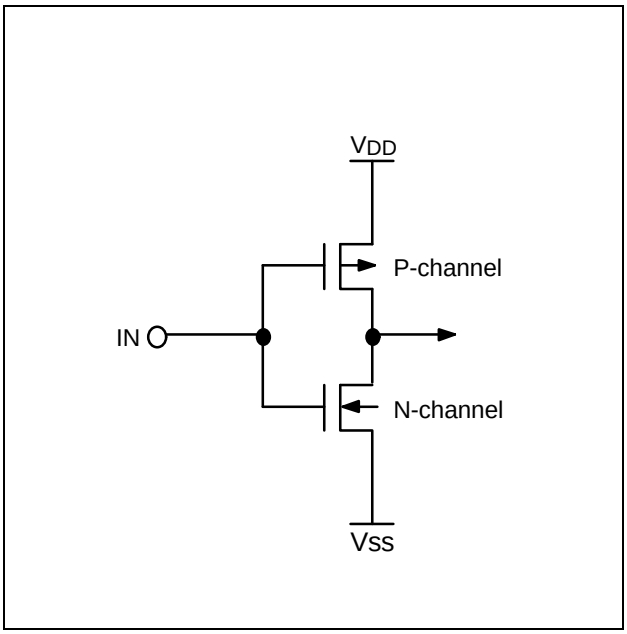


Figure 1-3. Pin Circuit Type A

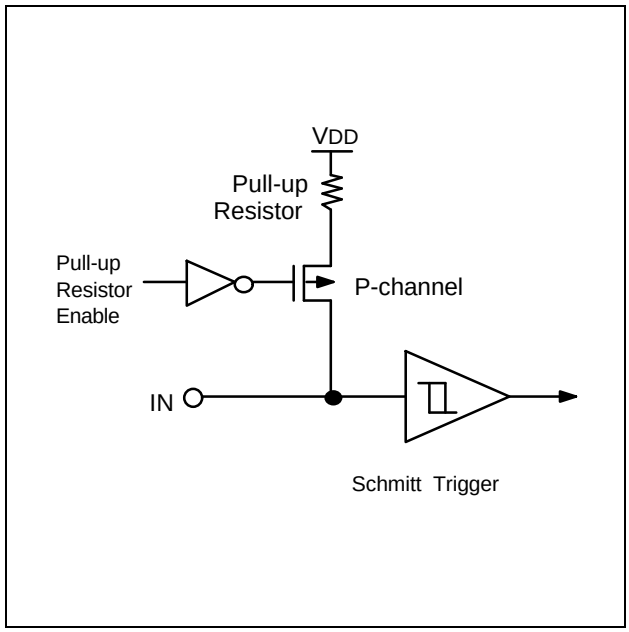


Figure 1-5. Pin Circuit Type A-3

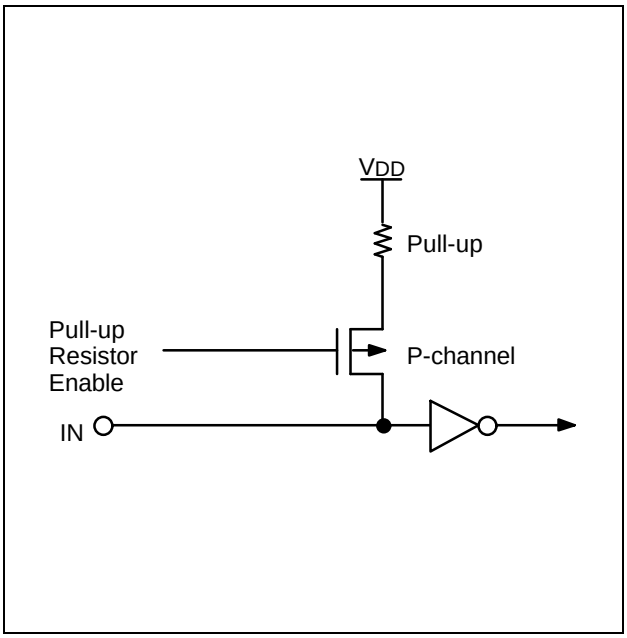


Figure 1-4. Pin Circuit Type A-1

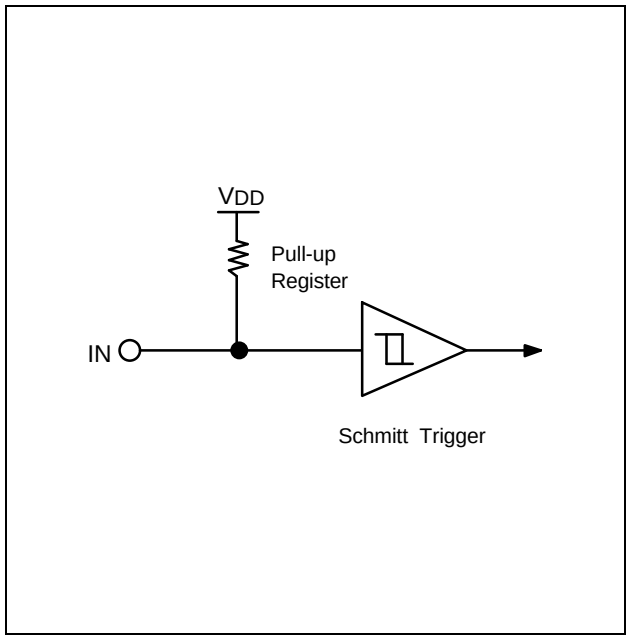


Figure 1-6. Pin Circuit Type B

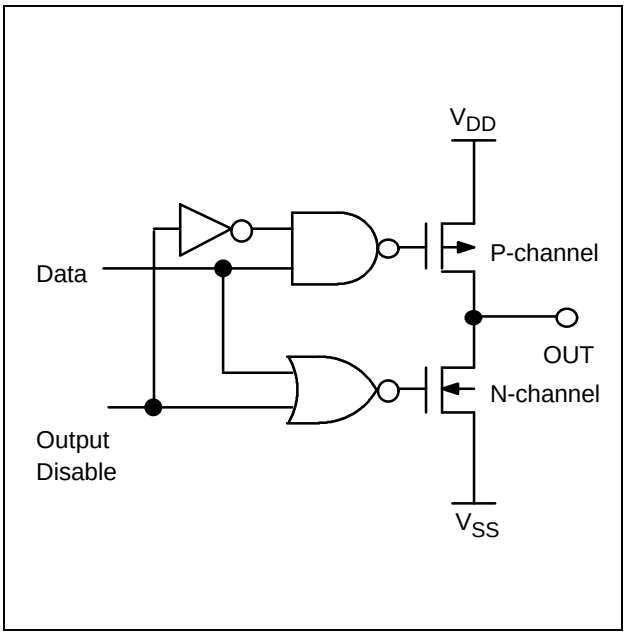


Figure 1-7. Pin Circuit Type C

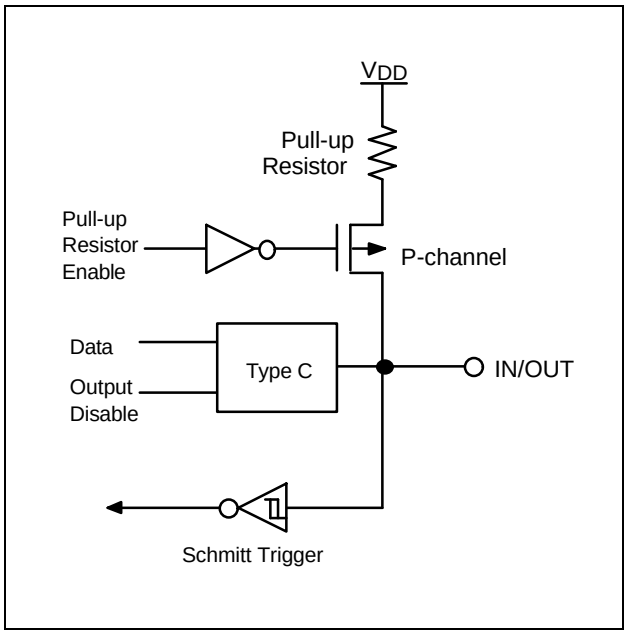


Figure 1-9. Pin Circuit Type D-1

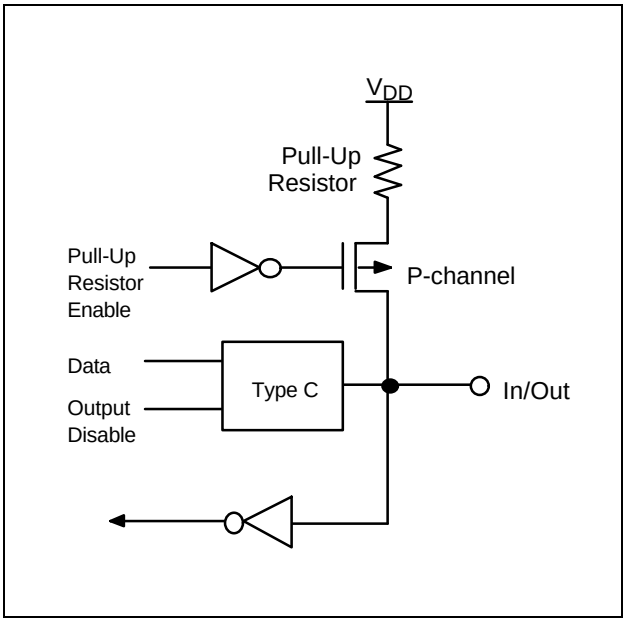


Figure 1-8. Pin Circuit Type D

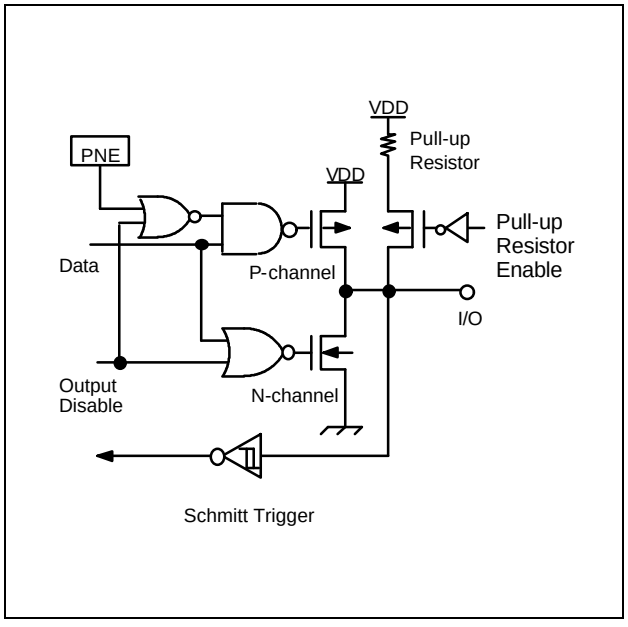


Figure 1-10. Pin Circuit Type E

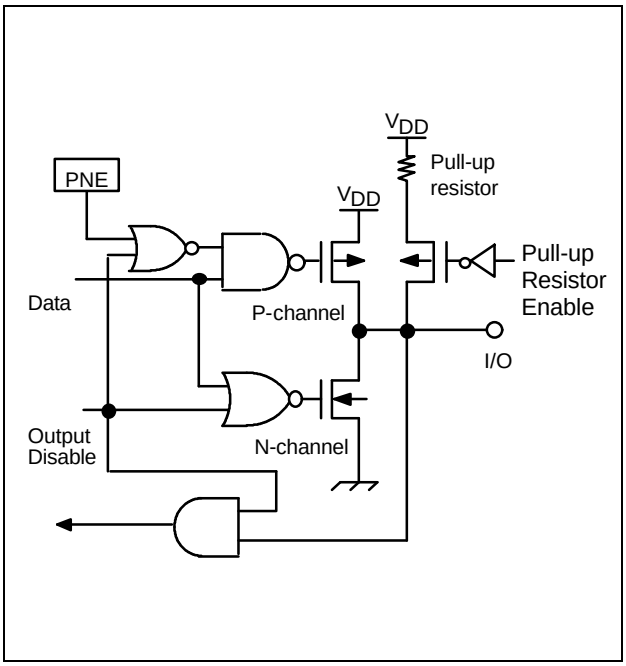


Figure 1-11. Pin Circuit Type E-1

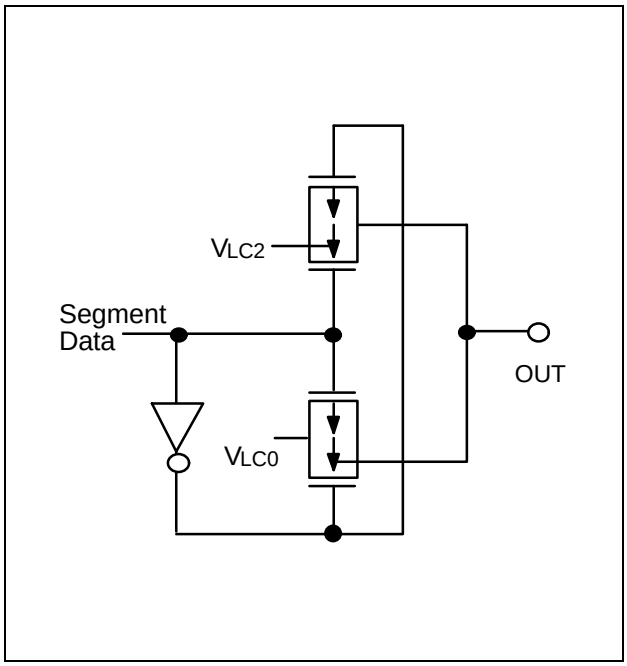


Figure 1-13. Pin Circuit Type H-10

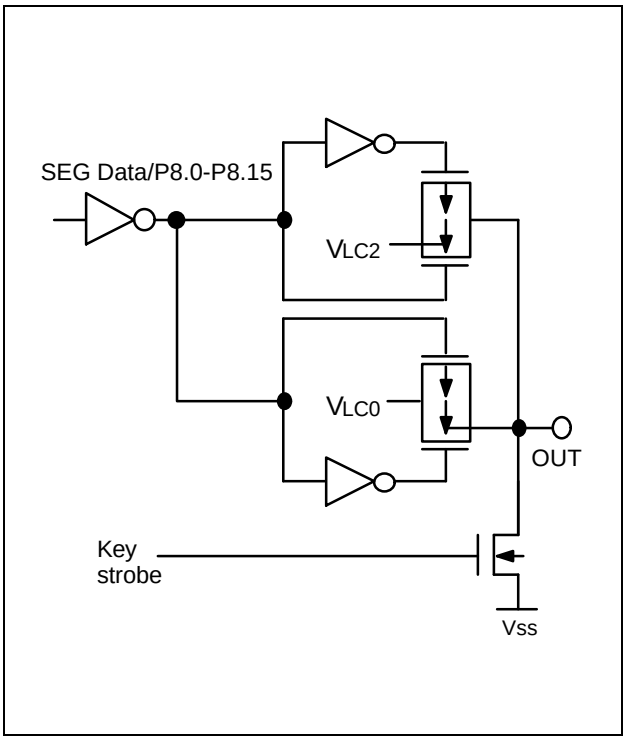


Figure 1-12. Pin Circuit Type H-9

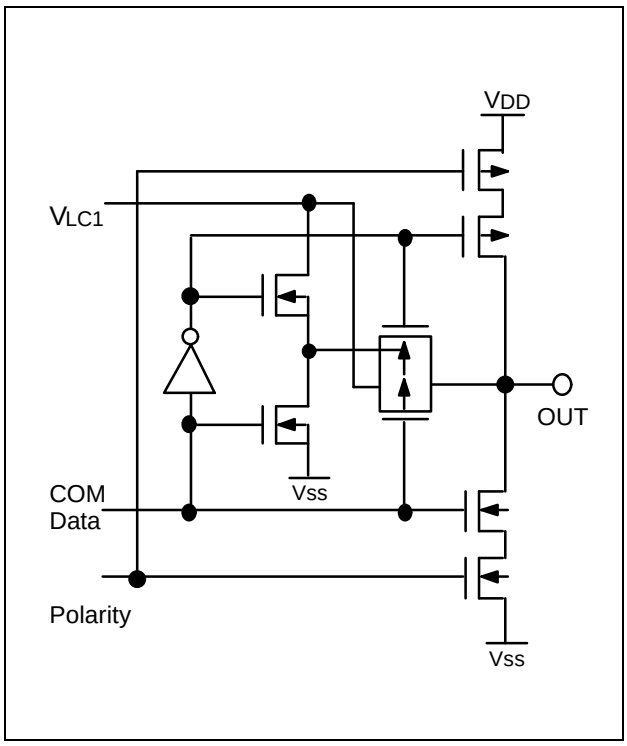


Figure 1-14. Pin Circuit Type H-11

13 ELECTRICAL DATA

OVERVIEW

In this section, information on S3C72E8/P72E8 electrical characteristics is presented as tables and graphics. The information is arranged in the following order:

STANDARD ELECTRICAL CHARACTERISTICS

— Absolute maximum ratings
— D.C electrical characteristics
— Main-system clock oscillator characteristics
— Sub-system clock oscillator characteristics
— I/O capacitance
— A.C electrical characteristics
— Operating voltage range

MISCELLANEOUS TIMING WAVEFORMS

— A.C timing measurement point
— Clock timing measurement at X_{in}
— Clock timing measurement at XT_{in}
— TCL0 timing
— Input timing for RESET
— Input timing for external interrupts

STOP MODE CHARACTERISTICS AND TIMING WAVEFORMS

— RAM data retention supply voltage in stop mode
— Stop mode release timing when initiated by RESET
— Stop mode release timing when initiated by an interrupt request

Table 13-1. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions		Rating	Units
Supply Voltage	V_{DD}	–		– 0.3 to + 6.5	V
Input Voltage	V_I	Ports 0, 1, 2, 4, 5, 6, 7		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_O	–		– 0.3 to V_{DD} + 0.3	V
High Level Output current	I_{OH}	One pin		– 15	mA
		All output pins		– 30	mA
Low Level Output Current	I_{OL}	One pin	Peak value	30	mA
			RMS value (note)	15	mA
		All pins	Peak value	100	mA
			RMS value (note)	60	mA
Operating Temperature	T_A	–		– 40 to + 85	°C
Storage Temperature	T_{STG}	–		– 65 to + 150	°C

NOTE : RMS value = Peak Value × $\sqrt{\text{Duty}}$.

Table 13-2. D.C Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input High Voltage	VIH1	Pins except below	0.7 V_{DD}	–	V_{DD}	V
	VIH2	Port0, 1, 6, 7, P4.0, RESET	0.8 V_{DD}	–	V_{DD}	
	VIH3	X_{IN}, X_{OUT} and XT_{IN}	V_{DD} – 0.1	–	V_{DD}	
Input Low Voltage	VIL1	All input pins except below	–	–	0.3 V_{DD}	
	VIL2	Port0, 1, 6, 7, P4.0, RESET		–	0.2 V_{DD}	
	VIL3	X_{IN},X_{OUT} and XT_{IN}		–	0.1	
Output High Voltage	VOH1	V_{DD} = 4.5 V to 5.5 V Port2, 4, 5, 6, 7 I_{OH} = – 1mA	V_{DD} – 1.0	–	–	

Table 13-2. D.C Characteristics(continued)

(T_A = – 40 °C to + 85C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Output Low Voltage	V_{OL1}	V_{DD} = 4.5 V to 5.5 V Port2, 4, 5, 6, 7 I_{OL}= 15mA		–	–	2	
		V_{DD} = 1.8 V to 5.5 V I_{OL}=1.6mA		–	–	0.4	
Input High Leakage Current	I_{LIH1}	Vin = V_{DD} All input pins except below		–	–	3	µA
	I_{LIH2}	Vin = V_{DD} X_{IN}, X_{OUT}, XT_{IN}				20	
Input Low Leakage Current	I_{LIL1}	V_{IN} = 0 V All input pins except X_{IN}, X_{OUT}, XT_{IN} and RESET		–	–	– 3	
	I_{LIL2}	V_{IN} = 0 V X_{IN}, X_{OUT}, XT_{IN}		–	–	– 20	
Output High Leakage Current	I_{LOH1}	V_O = V_{DD} Port2, 4, 5, 6, 7		–	–	3	
Output Low Leakage Current	I_{LOL1}	V_O = 0 V Port2, 4, 5, 6, 7		–	–	– 3	
Pull-up Resistor	RL1	V_{DD} = 5 V, V_{IN} = 0 V All pins except RESET		25	50	100	KΩ
		V_{DD} = 3 V		50	100	200	
	RL2	V_{DD} = 5 V, V_{IN} = 0 V RESET		100	250	400	
		V_{DD} = 3 V		200	500	800	
Medium Output Voltage(1)	V_{OM1}	COM0-COM8		VM1 – 0.2	VM1	VM1 + 0.2	V
	V_{OM2}	COM0-COM8		VM2 – 0.2	VM2	VM2 + 0.2	
	V_{OM3}	SEG0-CSEG59		VM3 – 0.2	VM3	VM3 + 0.2	
	V_{OM4}	SEG0-CSEG59		VM4 – 0.2	VM4	VM4 + 0.2	
High Output Impedance	ROH1	V_O = V_{DD}–0.5V	SEG0-SEG59	–	–	90	KΩ
	ROH2		COM0-COM8	–	–	25	
Low Output Resistor	ROL1	VO = 0.5V	SEG0-SEG59	–	–	90	kΩ
	ROL2		SEG0-SEG15 (key strobe)	–	–	2	
	ROL3		COM0-COM8	–	–	25	

Table 13-2. D.C Characteristics (continued)

(T_A = – 40 °C to + 85C, V_{DD} = 1.8 V to 5.5 V)

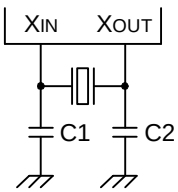
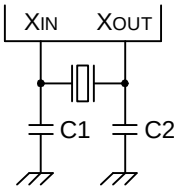
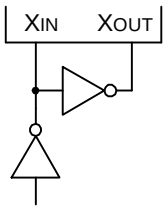
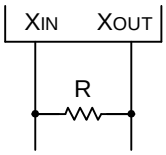
Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Supply Current (2) (3)	IDD1	Run mode : V_{DD} = 5 V ± 10%	6MHz	–	5.1	8	mA
		Crystal oscillator C1 = C2 = 22pF	4.19MHz		3.8	6	
		V_{DD} = 3 V ± 10%	6MHz		2.5	4	
			4.19MHz		1.8	3	
	IDD2	Idle mode : V_{DD} = 5 V ± 10%	6MHz		1.3	2.5	
		Crystal oscillator C1 = C2 = 22pF	4.19MHz		1.1	1.8	
		V_{DD} = 3 V ± 10%	6MHz		0.5	1.5	
			4.19MHz		0.4	1.0	
	IDD3	Run mode: V_{DD} = 3 V ± 10% 32kHz crystal oscillator		–	30	45	µA
	IDD4	Idle mode: V_{DD} = 3 V ± 10% 32kHz crystal oscillator	LCD ON (4)	–	17	30	
		V_{DD} = 3 V ± 10% 32kHz crystal oscillator	LCD OFF		6	15	
	IDD5	Stop mode; V_{DD} = 5 V ± 10%, XT_{IN} = 0V		–	2.4	5	
		Stop mode; V_{DD} = 3 V ± 10%, XT_{IN} = 0V			0.6	3	

NOTES:

1. VM1=2.75/3.75 V_{DD}, VM2=1/3.75 V_{DD}, VM3=2/3.75 V_{DD}, VM4=1.75/3.75 V_{DD}
2. Supply current does not include current drawn through internal pull-down resistor and LCD driving resistors.
3. For D.C. electrical voltages, PCON register must be set to 0011B.
4. The mode of I_{DD4} (LCD ON) is normal.

Table 13-3. Main System Clock Oscillator Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency(fx) (1)	–	0.4	–	6.0	MHz
		Stabilization time (2)	After V_{DD} reaches the minimum level of its variable range	–	–	4	ms
Crystal Oscillator		Oscillation frequency(fx) (1)	–	0.4	–	6	MHz
		Stabilization time (2)	V_{DD} = 4.5 V to 5.5 V	–	–	10	ms
			V_{DD} = 1.8 V to 5.5 V	–	–	60	
External Clock		X_{in} input frequency(fx) (1)	–	0.4	–	6	MHz
		X_{in} input high and low level width (t_{XH}, t_{XL})	–	83.3	–	1250	ns
RC Oscillator		Frequency	V_{DD} = 5 V	–	2	–	MHz
			V_{DD} = 3 V	–	1	–	

NOTES:

1. Oscillation frequency and input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillator stabilization after a power-on or release of STOP mode.

Table 13-4. Recommended Oscillator Constants

(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

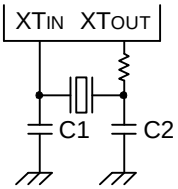
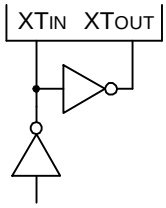
Manufacturer	Series Number (1)	Frequency Range	Load Cap (pF)		Oscillator Voltage Range (V)		Remarks
			C1	C2	MIN	MAX	
TDK	FCR ðÿM5	3.58 MHz–6.0 MHz	33	33	2.0	5.5	Leaded Type
	FCR ðÿMC5	3.58 MHz–6.0 MHz	(2)	(2)	2.0	5.5	On-chip C Leaded Type
	CCR ðÿMC3	3.58 MHz–6.0 MHz	(3)	(3)	2.0	5.5	On-chip C SMD Type

NOTES:

1. Please specify normal oscillator frequency.
2. On-chip C: 30pF built in.
3. On-chip C: 38pF built in.

Table 13-5. Subsystem Clock Oscillator Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Crystal Oscillator		Oscillation frequency (1)	–	32	32.768	35	kHz
		Stabilization time (2)	V_{DD} = 4.5 V to 5.5 V	–	1.0	2	ms
			V_{DD} = 1.8 V to 5.5 V	–	–	10	
External Clock		XT_{in} input frequency (1)	–	32	–	100	kHz
		XT_{in} input high and low level width (t_{XTH}, t_{XTL})	–	5	–	15	µs

NOTES:
1. Oscillation frequency and input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on or release of STOP mode.

Table 13-6. Input/Output Capacitance

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	f = 1 MHz; Unmeasured pins are returned to V_{SS}	–	–	15	pF
Output Capacitance	C_{OUT}		–	–	15	pF
I/O Capacitance	C_{IO}		–	–	15	pF

Table 13-7. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction Cycle Time (NOTE)	t_{CY}	V_{DD} = 2.7 V to 5.5 V	0.67	–	64	µs
		V_{DD} = 1.8 V to 5.5 V	1.33			
		With sub-system clock (fxt)	114	122	1952	
TCL0 Input Frequency	f_{TI}	V_{DD} = 2.7 V to 5.5 V	0	–	1.5	MHz
		V_{DD} = 1.8 V to 5.5 V			1	kHz
TCL0 Input High, Low Width	t_{TIH} t_{TIL}	V_{DD} = 2.7 V to 5.5 V	0.48	–	–	µs
		V_{DD} = 1.8 V to 5.5 V	1.8			
External Interrupt Input High, Low Width	t_{INTH}, t_{INTL}	INT0, INT1, KS0 - KS7	10	–	–	µs
		KS0 - KS3	10			
RESET Low Level Width	t_{RSL}	–	10	–	–	µs

NOTE: Unless otherwise specified, the values of instruction cycle time condition assume a main-system clock (fx) source.

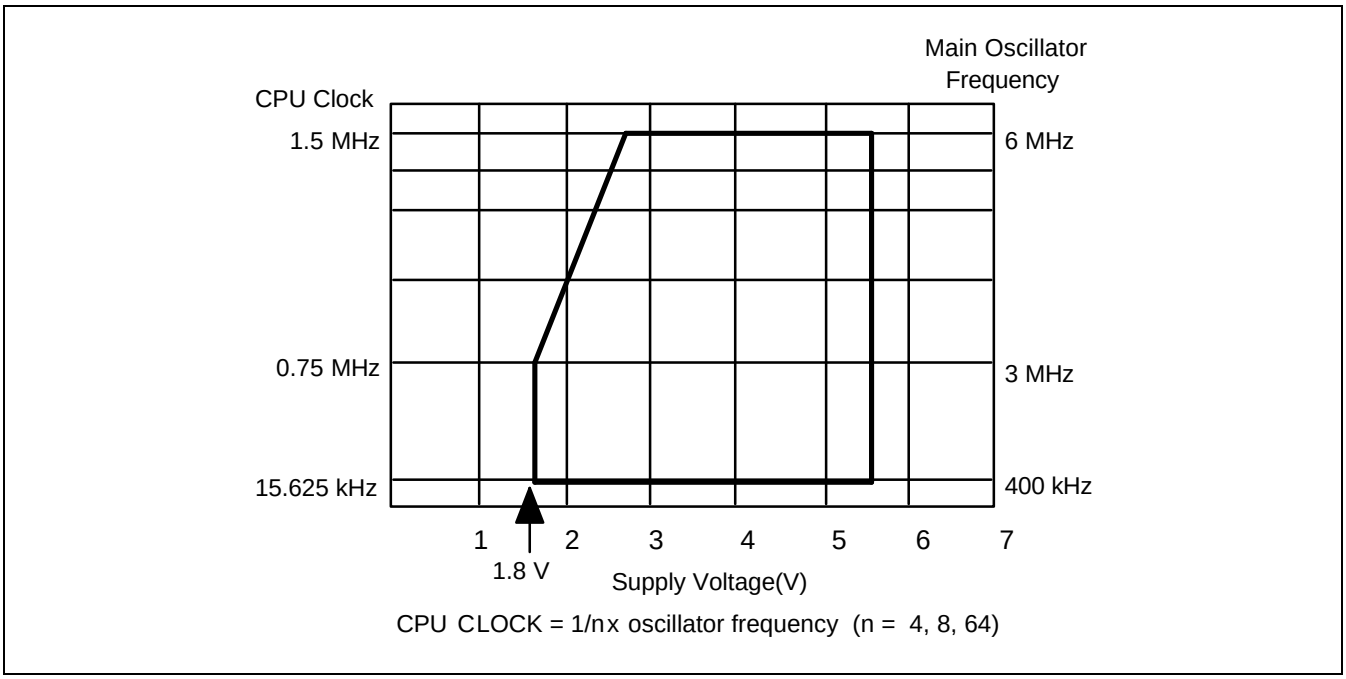


Figure 13-1. Standard Operating Voltage Range

Table 13-8. RAM Data Retention Supply Voltage in Stop Mode

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	–	1.8	–	5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8 V	–	0.1	10	µA
Release signal set time	t_{SREL}	–	0	–	–	µs
Oscillator stabilization wait time (1)	t_{WAIT}	Released by RESET	–	2^{17} / fx	–	ms
		Released by interrupt	–	(2)	–	

NOTES:
1. During oscillator stabilization time, all CPU operations are stopped to avoid unstable operation upon oscillation start.
2. The basic timer mode register (BMOD) interval timer delays execution of CPU instructions during the wait time.

TIMING WAVEFORMS

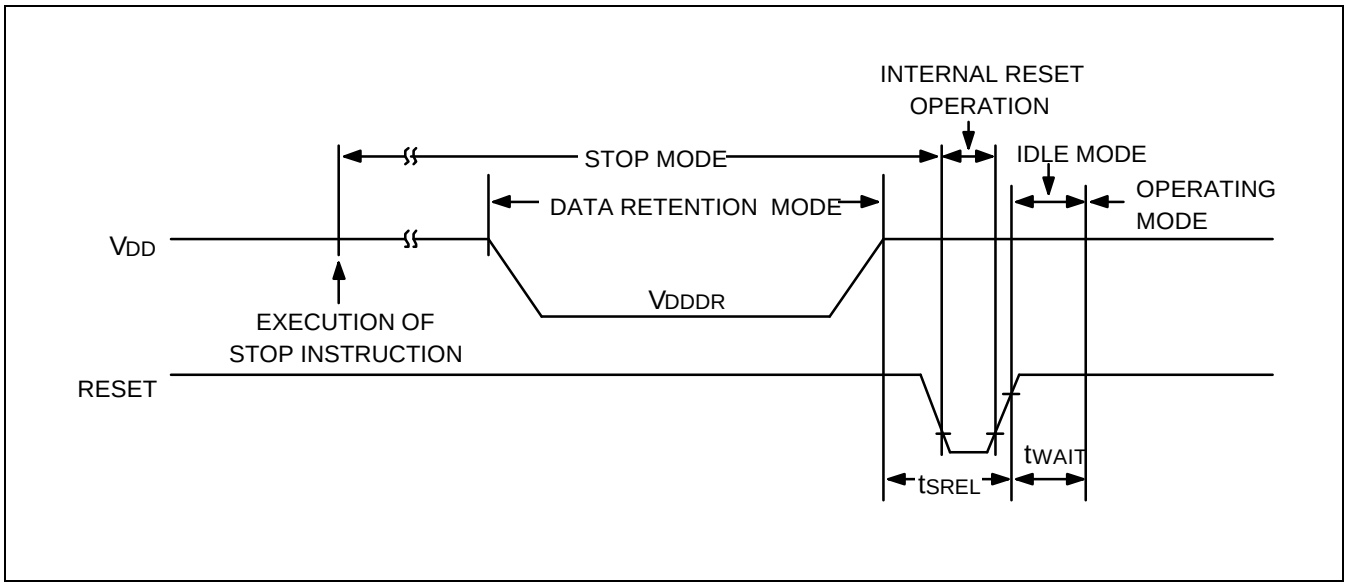


Figure 13-2. Stop Mode Release Timing When Initiated By RESET

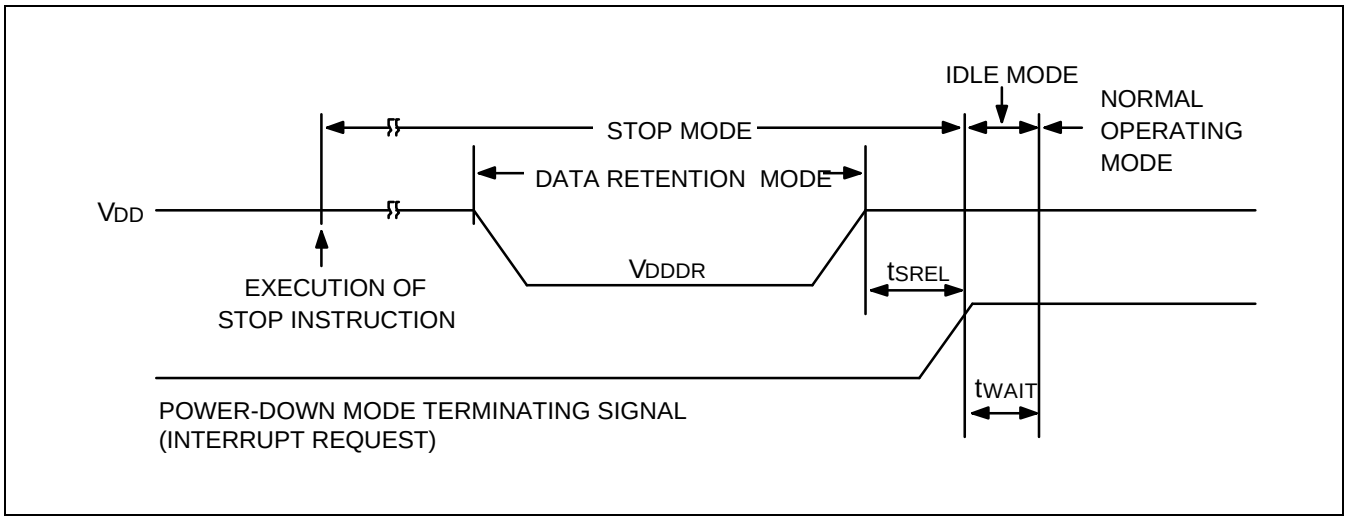


Figure 13-3. Stop Mode Release Timing When Initiated By Interrupt Request

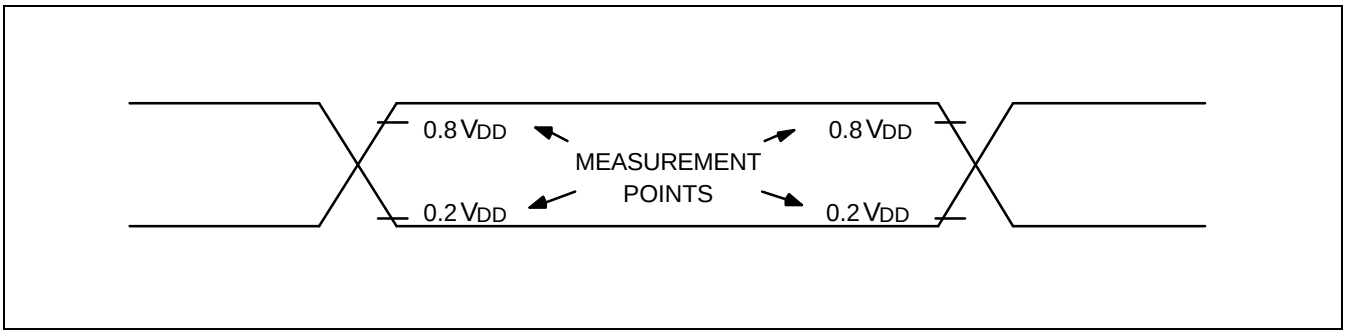


Figure 13-4. A.C. Timing Measurement Points (Except for X_{in} and XT_{in})

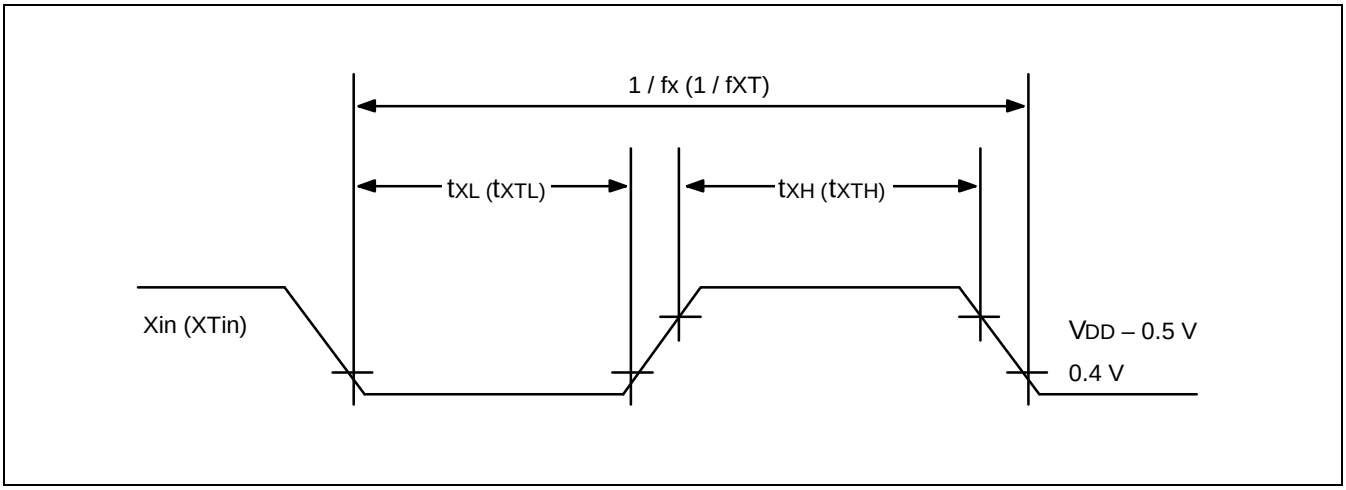


Figure 13-5. Clock Timing Measurement at X_{in} and XT_{in}

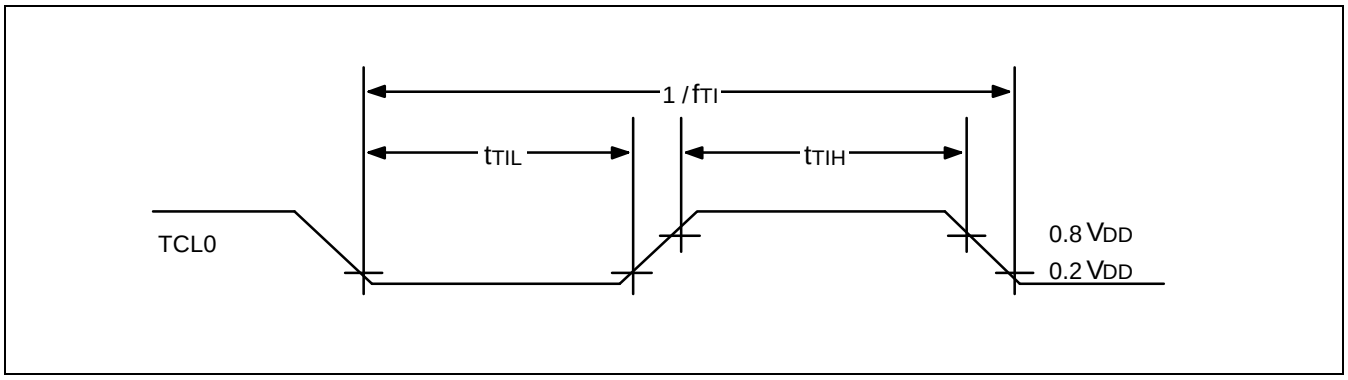


Figure 13-6. TCL0 Timing

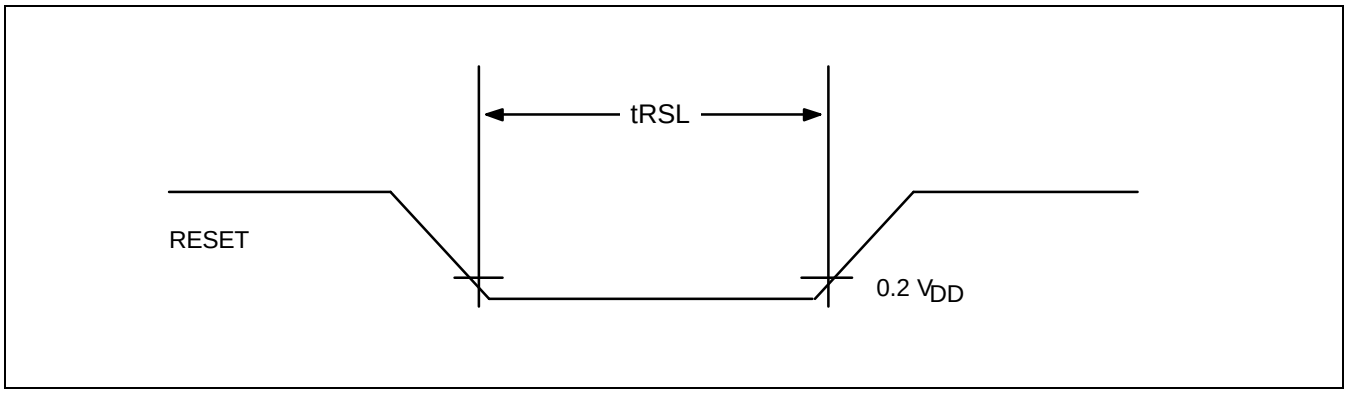


Figure 13-7. Input Timing for RESET Signal

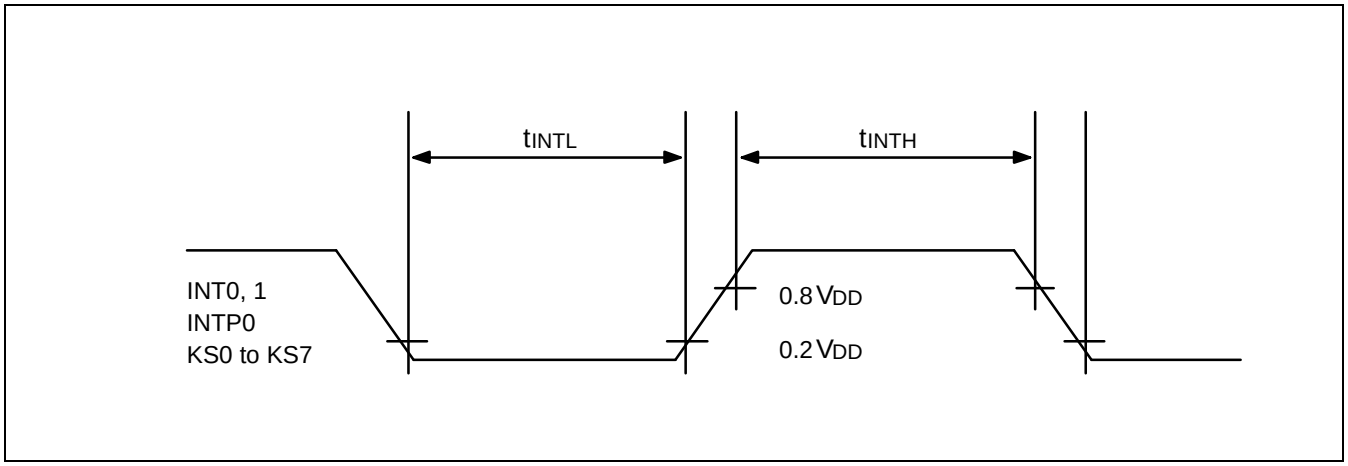


Figure 13-8. Input Timing for External Interrupts and Quasi-Interrupts

14 MECHANICAL DATA

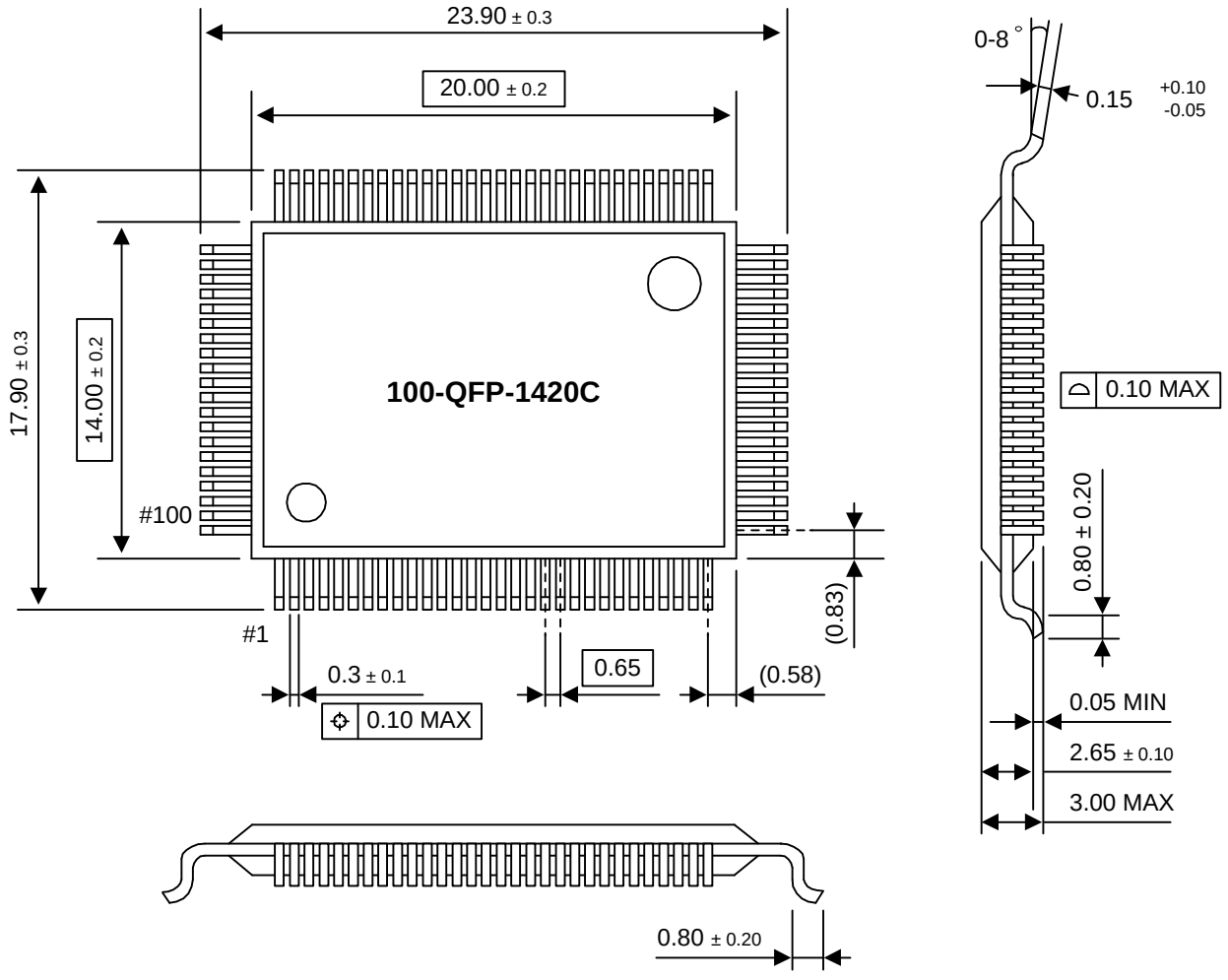
OVERVIEW

This section contains the following information about the device package:

— Package dimensions in millimeters

— Pad diagram

— Pad/pin coordinate data table



NOTE: Dimensions are in millimeters.

Figure 14-1. 100-QFP-1420 Package Dimensions

15 S3P72E8 OTP

OVERVIEW

The S3P72E8 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3C72E8 microcontroller. It has an on-chip OTP ROM instead of masked ROM. The EPROM is accessed by serial data format.

The S3P72E8 is fully compatible with the S3C72E8, both in function and in pin configuration. Because of its simple programming requirements, the S3P72E8 is ideal for use as an evaluation chip for the S3C72E8.

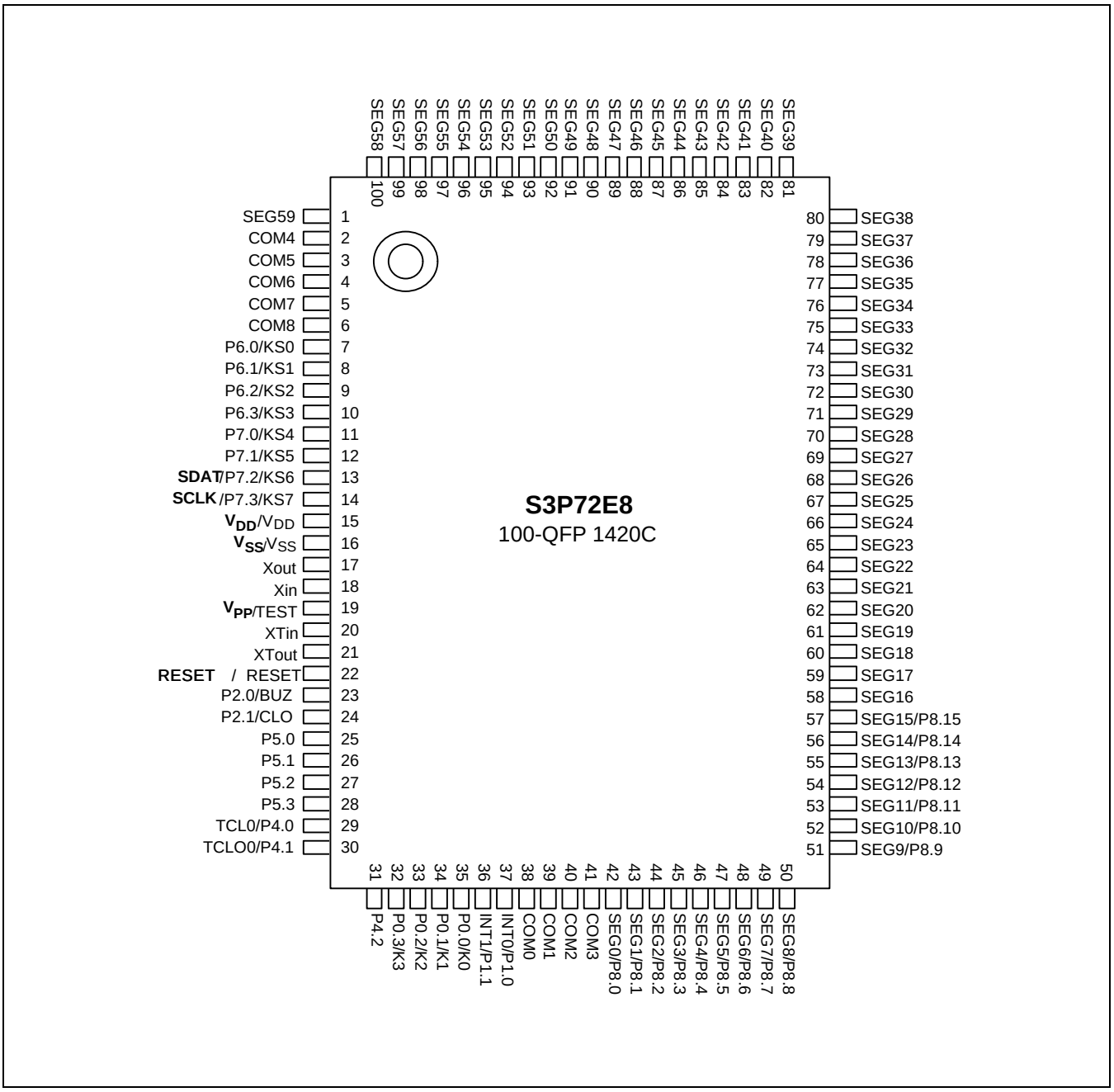


Figure 15-1. S3P72E8 Pin Assignments (100-QFP Package)

Table 15-1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip	During Programming			
Pin Name	Pin Name	Pin No.	I/O	Function
P3.1	SDAT	13	I/O	Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input / push-pull output port.
P3.0	SCLK	14	I/O	Serial clock pin. Input only pin.
TEST	V_{PP}(TEST)	19	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. (Option)
RESET	RESET	22	I	Chip initialization
V_{DD} / V_{SS}	V_{DD} / V_{SS}	15/16	I	Logic power supply pin. VDD should be tied to +5 V during programming.

Table 15-2. Comparison of S3P72E8 and S3C72E8 Features

Characteristic	S3P72E8	S3C72E8
Program Memory	8 Kbyte EPROM	8 Kbyte mask ROM
Operating Voltage (V_{DD})	1.8 V to 5.5 V	1.8 V to 5.5V
OTP Programming Mode	V_{DD} = 5 V, V_{PP}(TEST)=12.5V	
Pin Configuration	100 QFP	100 QFP
EPROM Programmability	User Program 1 time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP}(TEST) pin of the S3P72E8, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 15-3 below.

Table 15-3. Operating Mode Selection Criteria

V_{DD}	Vpp (TEST)	REG/ MEM	Address (A15-A0)	R/W	Mode
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.

Table 15-4. D.C Characteristics

(T_A = –40 °C to +85C, VDD = 1.8 V to 5.5V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Supply Current [2][3]	I_{DD1}	Run mode : V_{DD}=5V±10%	6MHz	–	5.1	8	mA
		Crystal oscillator C1=C2=22pF	4.19MHz		3.8	6	
		V_{DD}=3V±10%	6MHz		2.5	4	
			4.19MHz		1.8	3	
	I_{DD2}	Idle mode : V_{DD}=5V±10%	6MHz		1.3	2.5	
		Crystal oscillator C1=C2=22pF	4.19MHz		1.1	1.8	
		V_{DD}=3V±10%	6MHz		0.5	1.5	
			4.19MHz		0.4	1.0	
	I_{DD3}	Run mode : V_{DD}=3V±10% 32kHz crystal oscillator		–	30	45	µA
	I_{DD4}	Idle mode : V_{DD}=3V±10% 32kHz crystal oscillator	LCD ON[4]	–	17	30	
		V_{DD}=3V±10% 32kHz crystal oscillator	LCD OFF		6	15	
	I_{DD5}	Stop mode; V_{DD}=5V±10%		–	2.4	5	
		Stop mode; V_{DD}=3V±10%			0.6	3	

NOTES:

1. VM1=2.75/3.75 VDD, VM2=1/3.75 VDD, VM3=2/3.75 VDD, VM4=1.75/3.75 VDD
2. Supply current does not include current drawn through internal pull-down resistor and LCD driving resistors.
3. For D.C. electrical voltages, PCON register must be set to 0011B.
5. The mode of I_{DD4} (LCD ON) is normal.

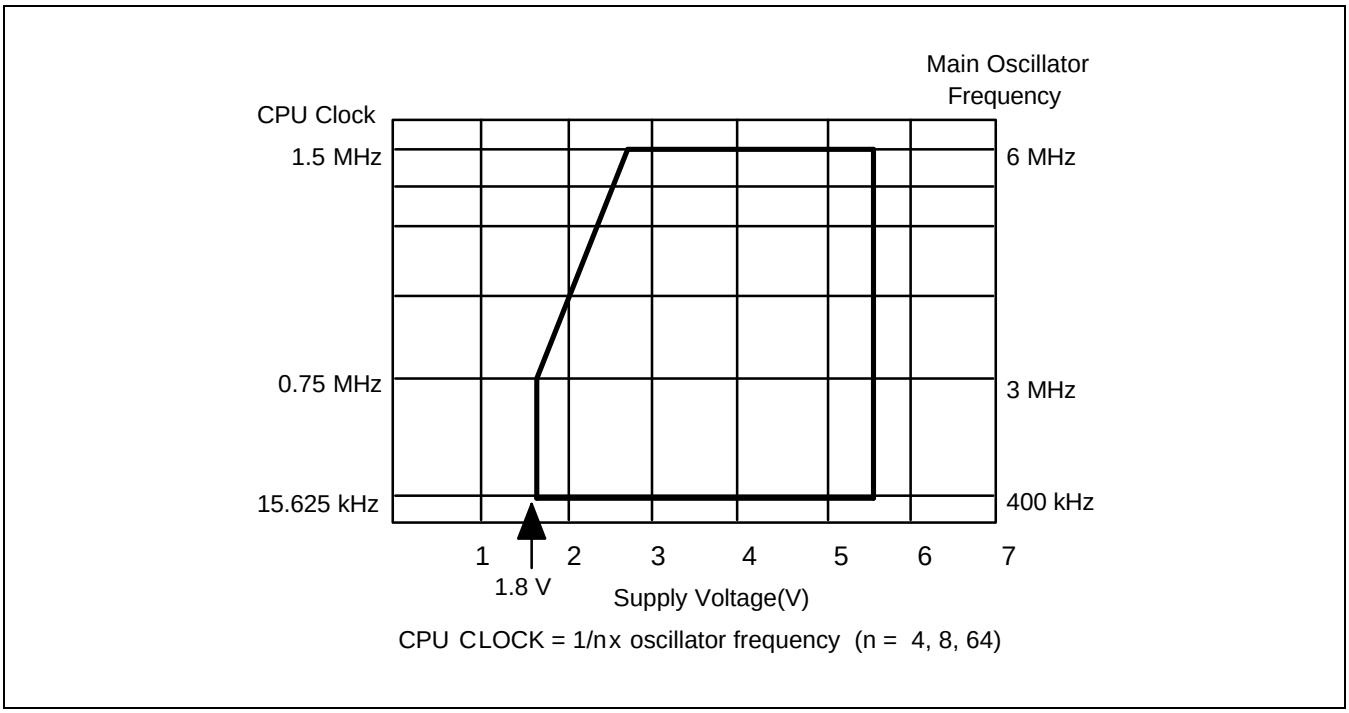


Figure 15-2. Standard Operating Voltage Range