L6208

FULLY INTEGRATED STEPPER MOTOR DRIVER

PRELIMINARY DATA

- OPERATING SUPPLY VOLTAGE FROM 8 TO 52V
- 5A PEAK CURRENT (2.8A DC)
- $R_{DS(ON)}$ 0.3Ω TYP. VALUE @ T_j = 25 °C
- BUILT-IN DECODING LOGIC
- BUILT-IN CONSTANT OFF-TIME PWM CURRENT CONTROL
- FAST/SLOW DECAY MODE SELECTION
- HIGH SIDE OVER CURRENT PROTECTION 5.6A TYP.
- CROSS CONDUCTION PROTECTION
- THERMAL SHUTDOWN
- OPERATING FREQUENCY UP TO 100KHz
- INTRINSIC FAST FREE WHEELING DIODES
- UVLO: UNDER VOLTAGE LOCKOUT

PowerDIP24 (20+2+2)	PowerSO36	SO24 (20+2+2)

ORDERING NUMBERS:

L6208N	L6208PD	L6208D

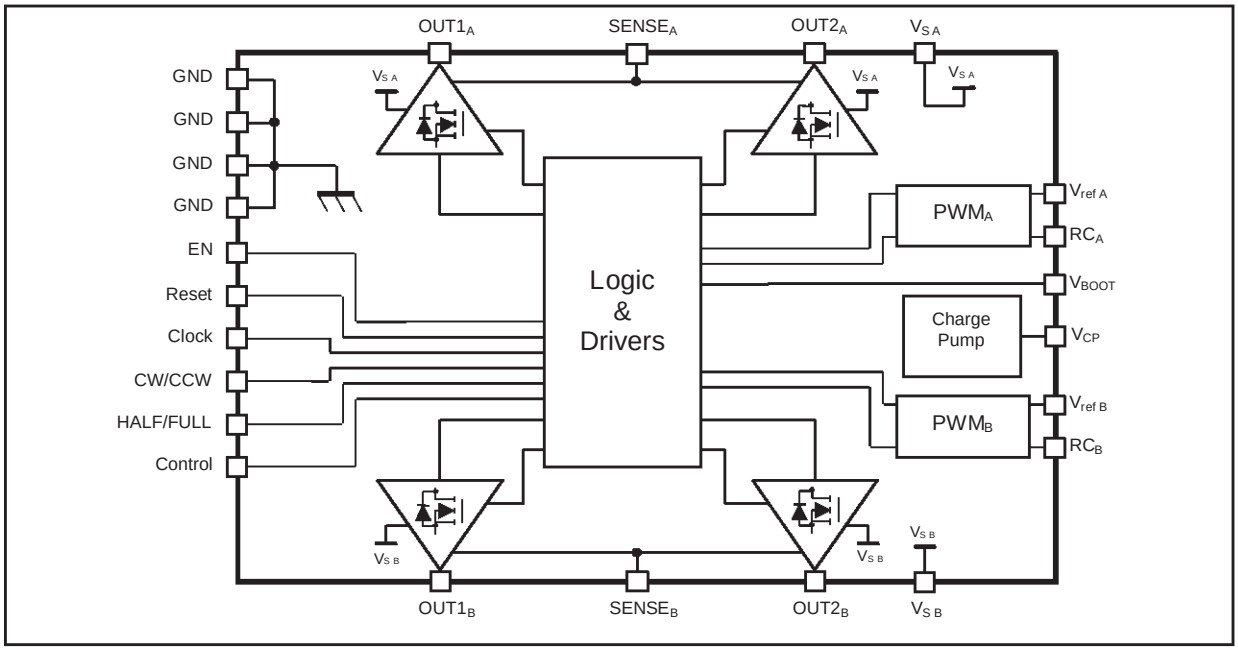
DESCRIPTION

The L6208 is a fully integrated stepper motor driver manufactured with multipower BCD technology, which combines isolated DMOS power transistors with CMOS and bipolar circuits on the same chip.

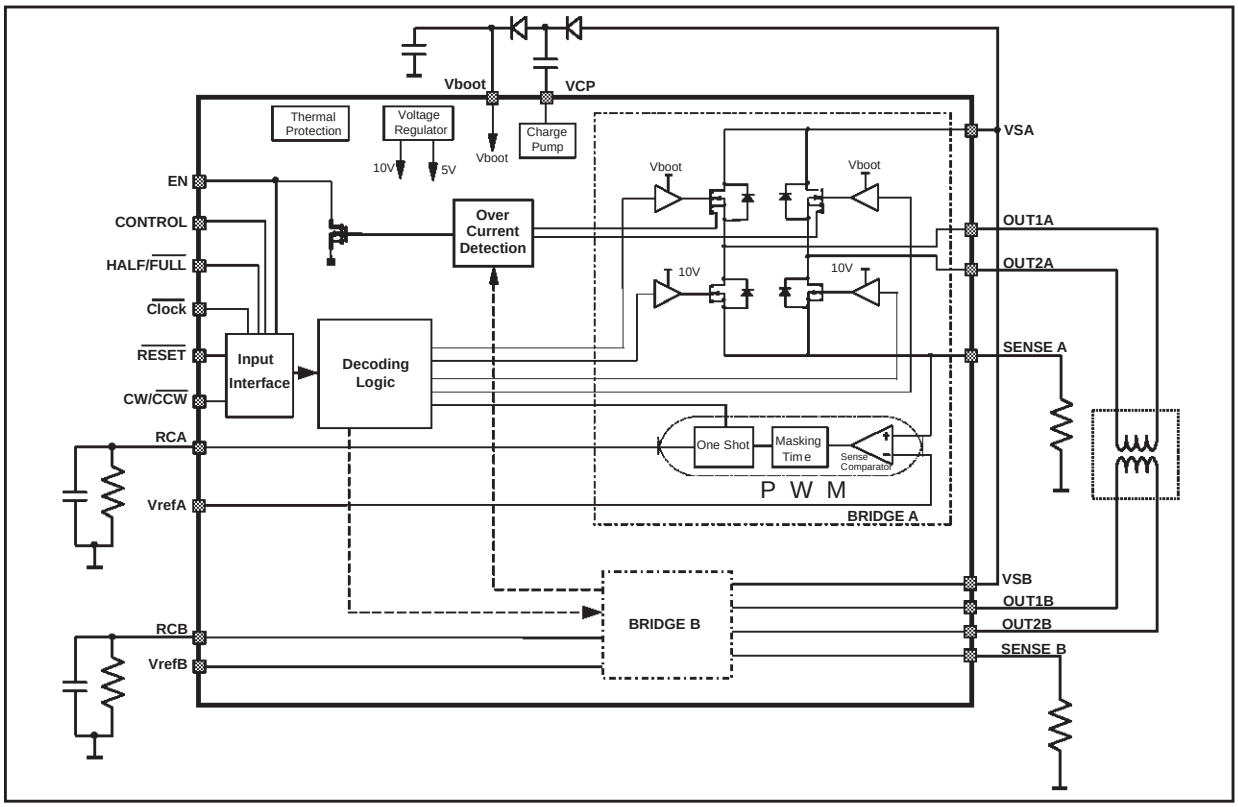
The logic inputs are CMOS/TTL and µP compatible. The device also includes all the circuitry needed to drive a stepper motor, that is the constant off time PWM control that performs the chopping current control and the state machine that generates the stepping sequence. Other features are the protection of the high side switches against unsafe over current conditions and the thermal shutdown.

The L6208 is assembled in PowerDIP24(20+2+2), PowerSO36 and SO24(20+2+2) packages.

BLOCK DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



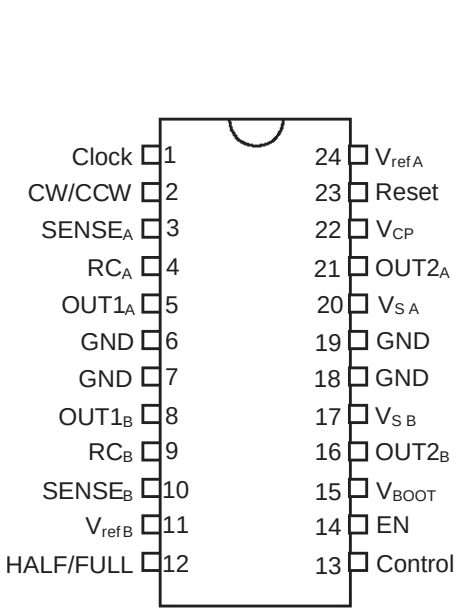
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test conditions	Value	Unit
V_S	Supply Voltage		60	V
V_{IN},V_{EN}	Input and Enable Voltage Range		-0.3 to +7	V
V_{refA}, V_{refB}	Voltage Range at V_{ref} pins		-0.3 to +7	V
$V_{RCA,RCB}$	Voltage Range at RC_A and RC_B pins		-0.3 to +7	V
V_{SENSE}	DC Sensing Voltage Range		-1 to +4	V
V_{BOOT}	Bootstrap Peak Voltage		V_S + 10	V
$I_{S(peak)}$	Pulsed Supply Current (for each V_S pin), internally limited by the overcurrent protection.	t_{PULSE} < 1ms	7.1	A
I_S	DCvSupply Current (for each V_S pin)		2.8	A
V_{OD}	Differential Voltage Between $V_{S\,A}$, $OUT1_A$, $OUT2_A$, $SENSE_A$ and $V_{S\,B}$, $OUT1_B$, $OUT2_B$, $SENSE_B$		60	V
T_{stg}, T_{OP}	Storage and Operating Temperature Range		-40 to 150	°C

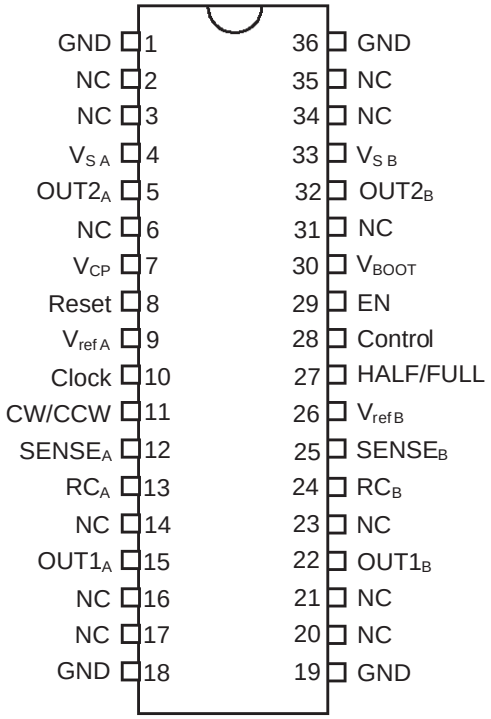
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		MIN	MAX	Unit
V_S	Supply Voltages		12	52	V
V_{OD}	Differential Voltage Between $V_{S\,A}$, $OUT1_A$, $OUT2_A$, $SENSE_A$ and $V_{S\,B}$, $OUT1_B$, $OUT2_B$, $SENSE_B$			52	V
V_{SENSE}	Sensing voltage (pulsed tw<t_{rr}) (DC)		-6 -1	6 1	V V
V_{ref}	V_{ref} Operating Voltage		-0.1	5	
I_{OUT}	DC Output Current			2.8	V
T_j	Operating Junction Temperature		-25	+125	°C
f_c	Commutation Frequency			100	kHz

PIN CONNECTIONS (Top View)



PDIP24/SO24



PowerSO36

PIN DESCRIPTION

Name	PowerSO36	PDIP24/ SO24	Function
$V_{S\,A}$	4	20	Supply voltage of the bridge A.
$V_{S\,B}$	33	17	Supply voltage of the bridge B. Must be connected to $V_{S\,A}$.
$OUT1_A$ $OUT2_A$	15 5	5 21	Bridge A outputs.
$OUT1_B$ $OUT2_B$	22 32	8 16	Bridge B outputs.
$SENSE_A$	12	3	Sense resistor for the bridge A.
$SENSE_B$	25	10	Sense resistor for the bridge B.
GND	1, 18, 19, 36	6, 7, 18, 19	Common ground terminals. In Powerdip and SO packages, these pins are also used for heat dissipation toward the PCB.
EN	29	14	Chip Enable. A Low logic level applied to this pin switches Off all the power DMOSs.
HALF/FULL	27	12	Logic input. When high, HALF STEP operation is selected; a Low logic level selects FULL STEP operation. ONE-PHASE-ON FULL STEP MODE (*wave mode*) is obtained by selecting FULL when the state machine is at an *even* numbered state. TWO-PHASE-ON FULL STEP MODE (*normal mode*) is obtained by selecting FULL when the state machine is at an *odd* numbered state.
Reset	8	23	Logic input. A Low logic level restores the *home* state (state 1) on the state machine.
Clock	10	1	Logic input. Step Clock. The step occurs on the rising edge of this signal.
CW/CCW	11	2	Logic input. Logic High sets clockwise direction. Logic Low sets counterclockwise direction.
Control	28	13	Logic input. Selects chopping style. FAST DECAY is selected with logic Low. A logic High selects SLOW DECAY.
$V_{ref\,A}$	9	24	A voltage applied to these pins sets the reference voltage of the sense comparators, determining the output current in PWM current control.
$V_{ref\,B}$	26	11	
V_{CP}	7	22	Bootstrap oscillator. Oscillator output for the external charge pump.
V_{BOOT}	30	15	Supply voltage to overdrive the upper DMOSs.
RC_A	13	4	A parallel RC network connected to these pins sets the OFF time of the low-side power DMOS of the correspondent bridge. The pulse generator is a monostable triggered by the output of the sense comparator of the bridge (t_{OFF} = 0.69 RC).
RC_B	24	9	

THERMAL DATA

Symbol	Description	PDIP24	SO24	PowerSO36	Unit
$R_{th\text{-}j\text{-}pins}$	MaximumThermal Resistance Junction-Pins	18	14	-	°C/W
$R_{th\text{-}j\text{-}case}$	Maximum Thermal Resistance Junction-Case	-	-	1	°C/W
$R_{th\text{-}j\text{-}amb1}$	MaximumThermal Resistance Junction-Ambient (1)	42	50	35	°C/W
$R_{th\text{-}j\text{-}amb2}$	Maximum Thermal Resistance Junction-Ambient (2)	58	77	62	°C/W

<(1)>Mounted on a multiplayer PCB with a dissipating copper surface on the bottom side of 2 x 12mm x 25mm (with a thickness of at least 35 µm).
<(2)>It's the same condition of the point above, without any heatsinking surface on the board.

ELECTRICAL CHARACTERISTICS

(T_{amb} = 25 °C, V_S = 48V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_S	Supply Voltage		8		52	V
I_S	Quiescent Supply Current	All Bridges OFF		5.5	10	mA
T_j	Thermal Shutdown Temperature		150			°C
Output DMOS Transistors						
I_{DSS}	Leakage Current	V_S = 52V			1	mA
$R_{DS(ON)}$	High-side Switch ON Resistance	T_j = 25 °C		0.34	0.4	Ω
		T_j =125 °C		0.53	0.59	Ω
	Low-side Switch ON Resistance	T_j = 25 °C		0.28	0.34	Ω
		T_j =125 °C		0.47	0.53	Ω
Source Drain Diodes						
V_{SD}	Forward ON Voltage	I_{SD} = 2.8A, EN = LOW		1.2	1.4	V
t_{rr}	Reverse Recovery Time	I_f = 2.8A		300		ns
t_{fr}	Forward Recovery Time			200		ns
Switching Rates						
$t_{D(on)}$	Output to out Turn ON Delay Time (3)	I_{LOAD}=2.8A	110	250	400	ns
t_{ON}	Output Rise Time (3)	I_{LOAD}=2.8A	20	105	300	ns
$t_{D(OFF)}$	Enable to out Turn OFF Delay Time (3)	I_{LOAD}=2.8A	240	580	760	ns
t_{OFF}	Output Fall Time (3)	I_{LOAD}=2.8A	20	78	300	ns
t_{DCLK}	Clock to output delay time (3)	I_{LOAD}=2.8A		2		µs

ELECTRICAL CHARACTERISTICS (continued)
(T_{amb} = 25 °C, V_S = 48V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{dt}	Dead Time Protection			1		µs
t_{blank}	Internal Blanking Time on SENSE pins			1	1.5	µs
f_{CP}	Charge pump frequency			0.75	1	MHz
UVLO comp						
$V_{th(ON)}$	Turn ON threshold		6.6	7	7.4	µs
$V_{th(OFF)}$	Turn OFF threshold		5.6	6	6.4	µs
Logic Input						
V_{INL}	Low level logic input voltage		-0.3		0.8	V
V_{INH}	High level logic input voltage		2		7	V
I_{INH}	High level logic input current	$V_{IN, EN}$ = 5 V			70	µA
I_{INL}	Low level logic input current	$V_{IN, EN}$ = GND			-10	µA
t_{CLK}	Minimum clock time (4)	see Fig. 2		0.1	1	µs
t_S	Minimum set up time (4)				1	µs
t_H	Minimum hold time (4)				1	µs
t_R	Minimum reset time (4)				1	µs
t_{RCLK}	Minimum reset to clock delay (4)				1	µs
Over Current Protection						
$I_{S\ OVER}$	Input supply over current protection threshold	Tj = 25 °C	4	5.6	7.1	A
V_{DIAG}	Open drain low level output voltage	I = 4 mA			0.4	V
Comparator and Monostable						
$I_{RCA, RCB}$	Source current at RC pins	V_{RC}=2.5 V	3	5		mA
V_{ref}	Input common mode comparator voltage range		-0.1		5	V
V_{th}	Comparator threshold voltage on SENSE pins	$V_{ref\ A, B}$ = 0.5 V	V_{ref} - 5mV		V_{ref} + 5mV	
t_{prop}	Turn OFF propagation delay (5)	$V_{ref\ A, B}$ = 0.5 V	0.1	0.2	0.3	µs
t_{OFF}	PWMRecirculation time	20 kΩ < R < 100 kΩ 0.1 nF < C < 100 nF	0.67RC	0.69RC	0.71RC	s
I_{bias}	Input bias current at V_{ref} pins			0.2		µA

<(3)>Resistive load used. See Fig. 1.
<(4)>See Fig. 2.
<(5)>Defined as the time between the voltage at the input of the current sense reaching the V_{ref} threshold and the lower DMOS switch beginning to turn off. The voltage at SENSE pin is increased instantaneously from V_{ref} -10 mV to V_{ref} +10 mV.

Figure 1. Switching Rates Definition

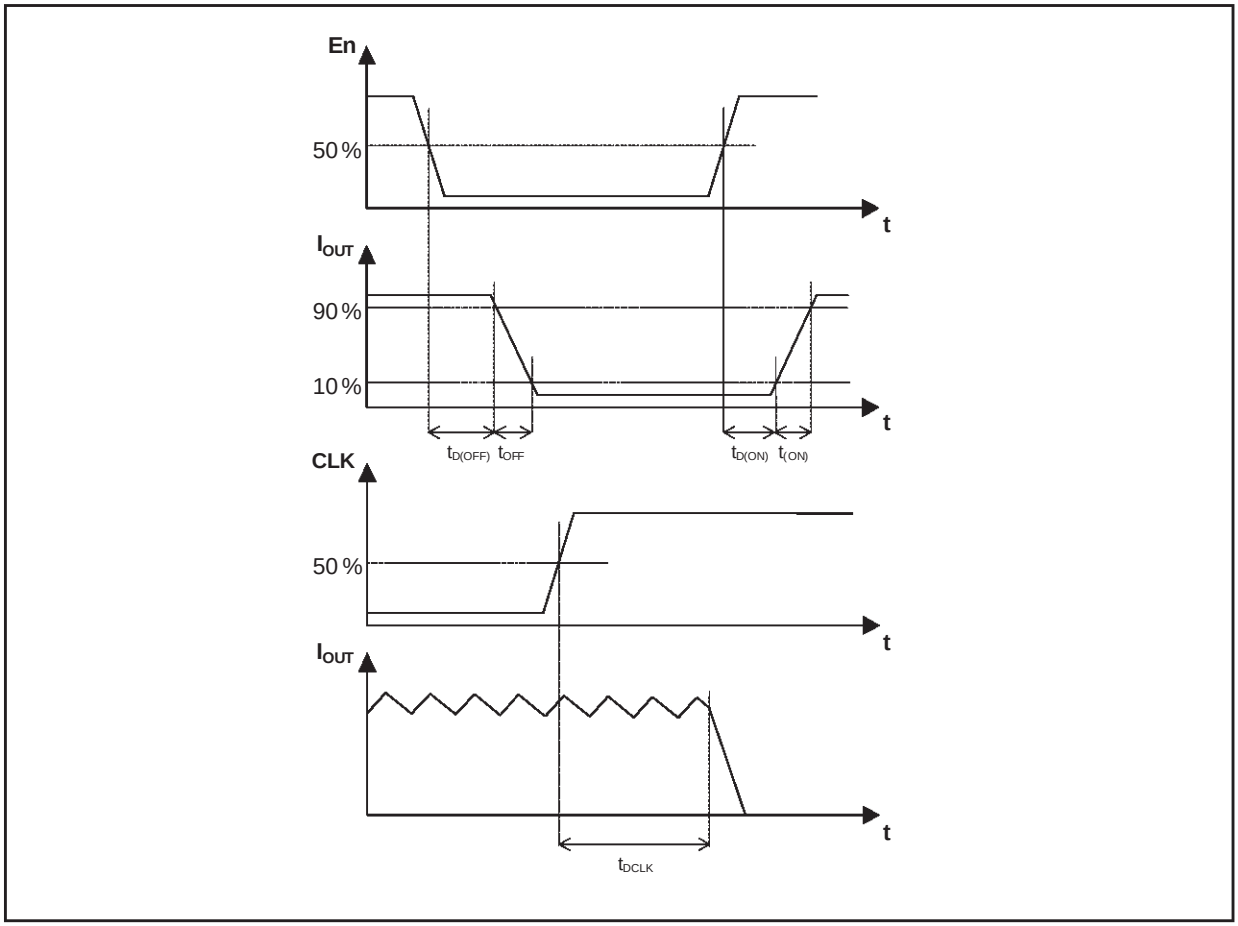


Figure 2. Minimum Timing Definition

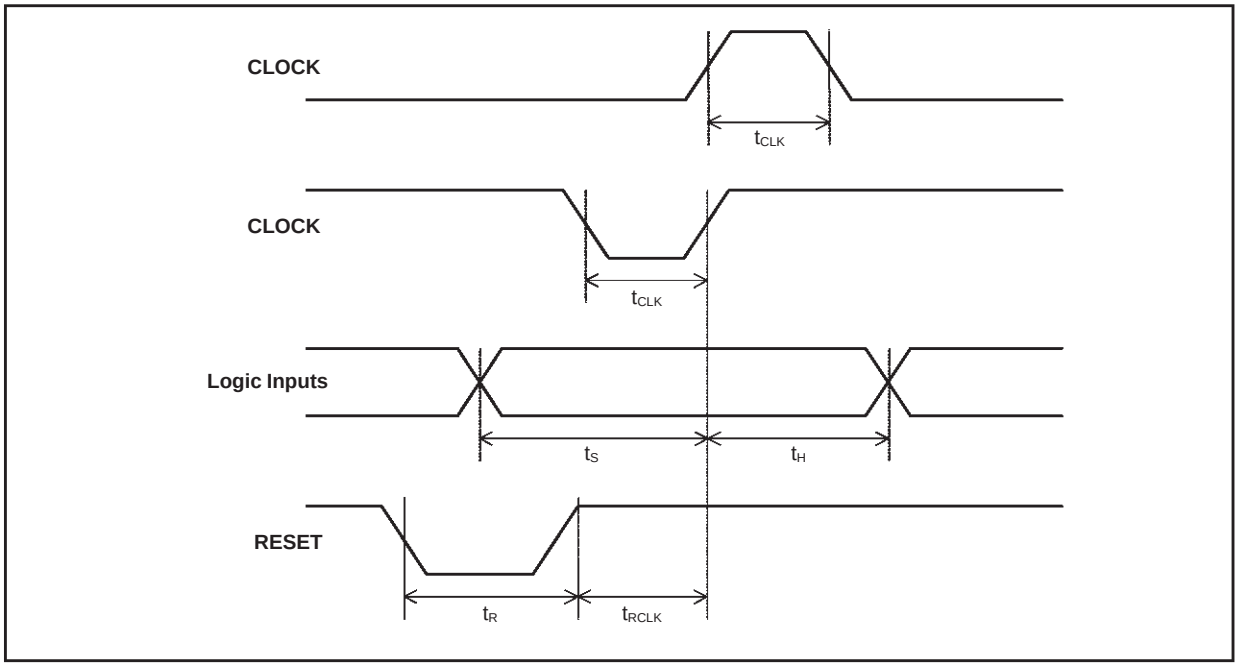


Figure 3. Typical Quiescent Current vs. Supply Voltage

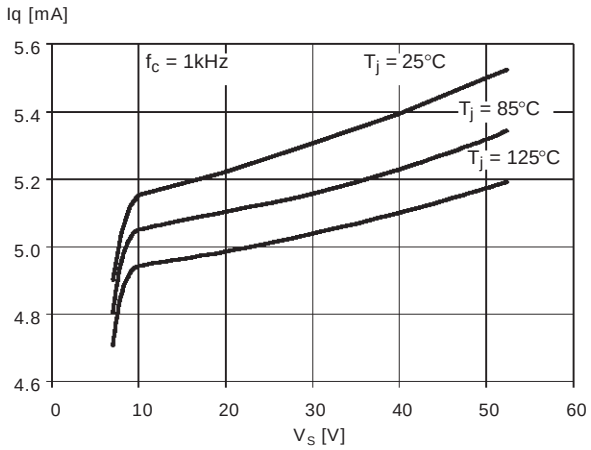


Figure 4. Normalized Typical Quiescent Current vs. Switching Frequency

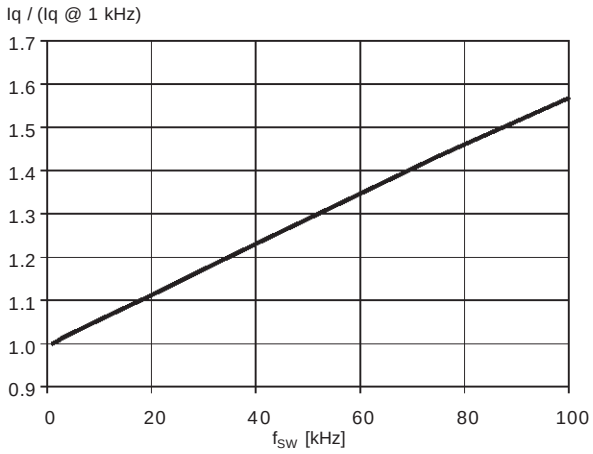


Figure 5. Typical Low-Side $R_{DS(ON)}$ vs. Supply Voltage

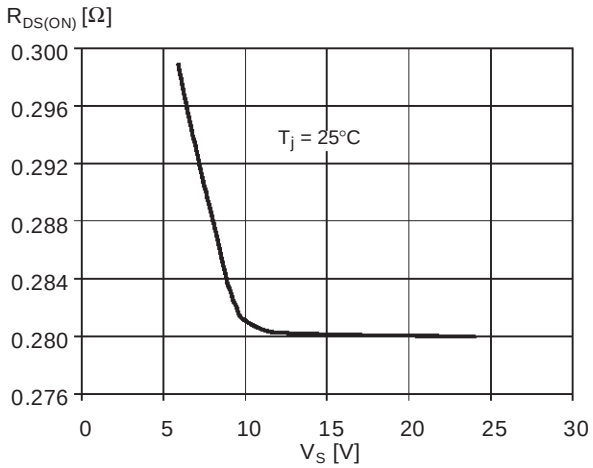


Figure 6. Typical High-Side RDS(ON) vs. Supply Voltage

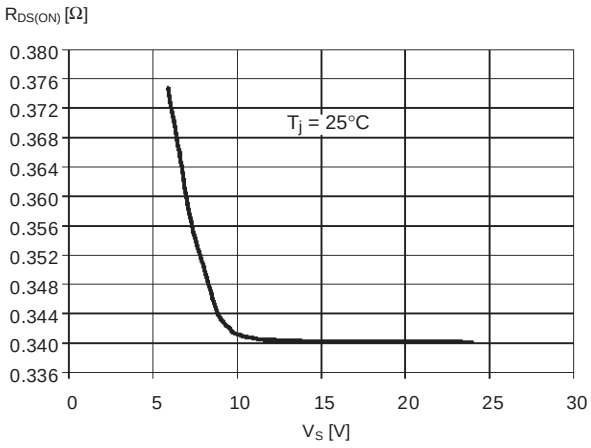


Figure 7. Normalized $R_{DS(ON)}$ vs.Junction Temperature (typical value)

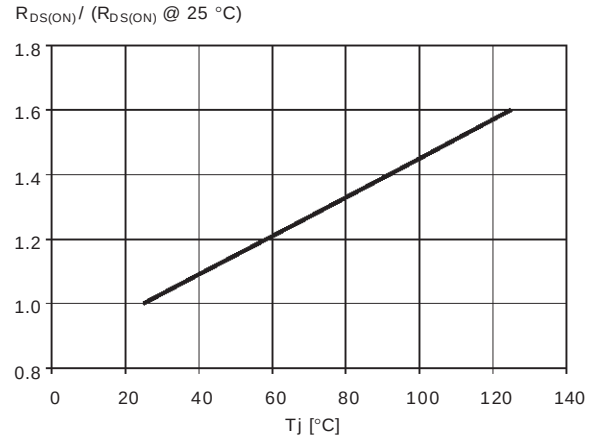
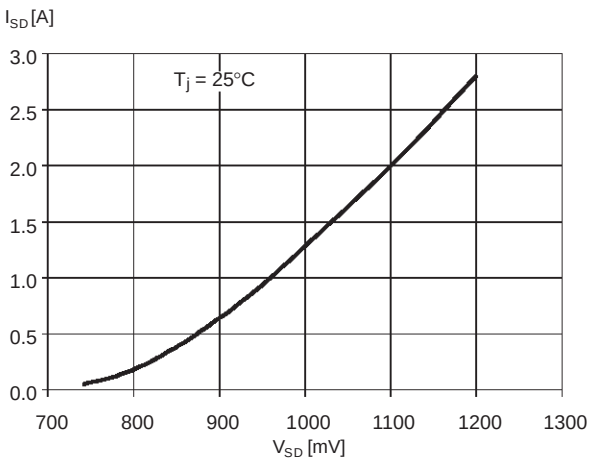


Figure 8. Typical Drain-Source Diode Forward ON Characteristic



CIRCUIT DESCRIPTION

The L6208 is a fully integrated bipolar stepper motor driver with two full bridge having power DMOS with a typical RDSON of 0.3Ω each. All the circuitry to implement the phase generation (decoding logic) is integrated, as well as a constant T_{off} PWM control for the current, separately for any of the two winding of the driven motor.

The decoding logic generates three different sequences, selected by the HALF/FULL input. These are normal (two phases), wave drive (one phase energized) and half-step (alternately one phase/two phases energized).

The decoding logic generates three different sequences, selected by the HALF/FULL input. These are normal (two phases energized), wave drive (one phase energized) and half-step (alternately one phase/two phases energized).

The constant T_{off} PWM current control consists in a sense comparator and a monostable.

When the current in each phase of the motor reaches the value set by the correspondent V_{ref} voltage (V_{ref} / R_{SENSE}), it will be forced to decrease for a constant Toff time, set by the RC network applied to the RC_A and RC_B pins. If the Control pin is at a High logic level, during the off-time the voltage applied to the motor phase will be approx. 0 V, turning on the high-side MOSFETs of the bridge (slow decay recirculation); if control is Low, instead, the voltage applied to the phase will be reversed, turning off the low side MOSFET that was on and turning on the opposite low-side (fast decay recirculation).

Figure 9.

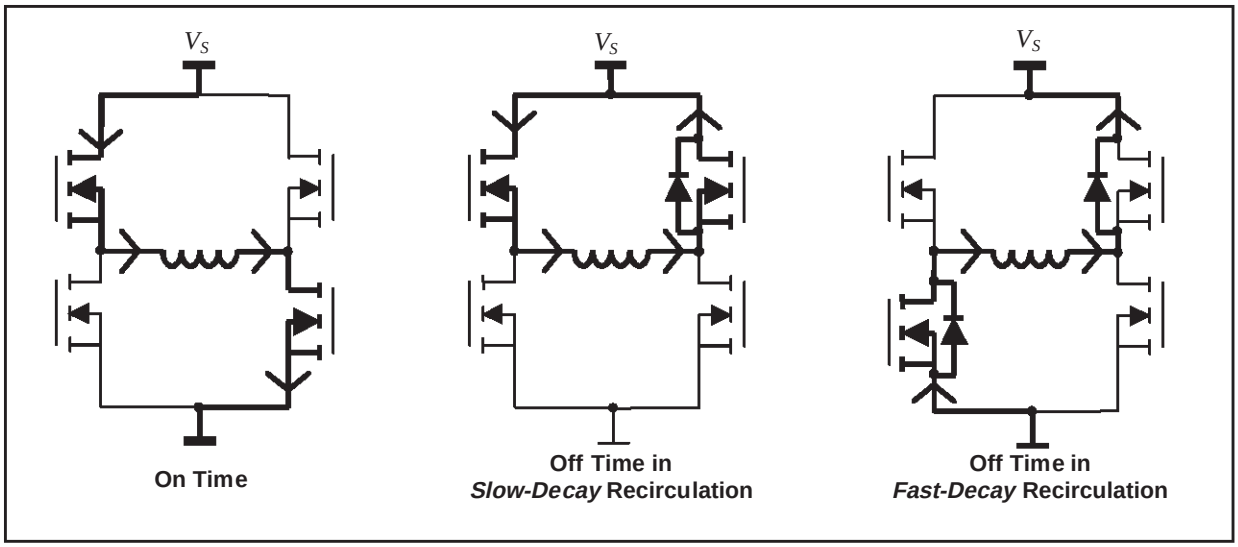
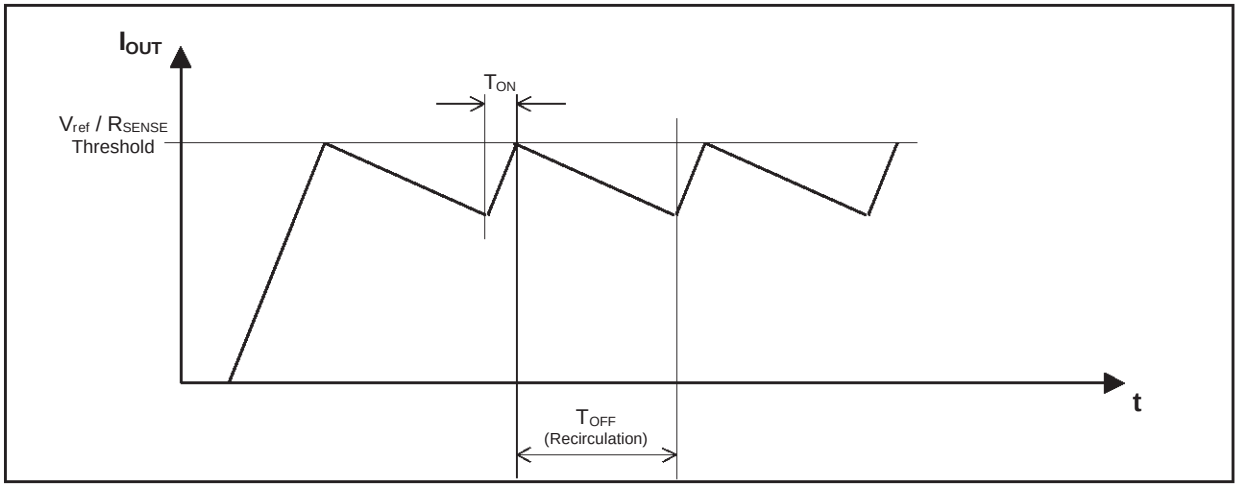


Figure 10. PWM Chopping Current Control

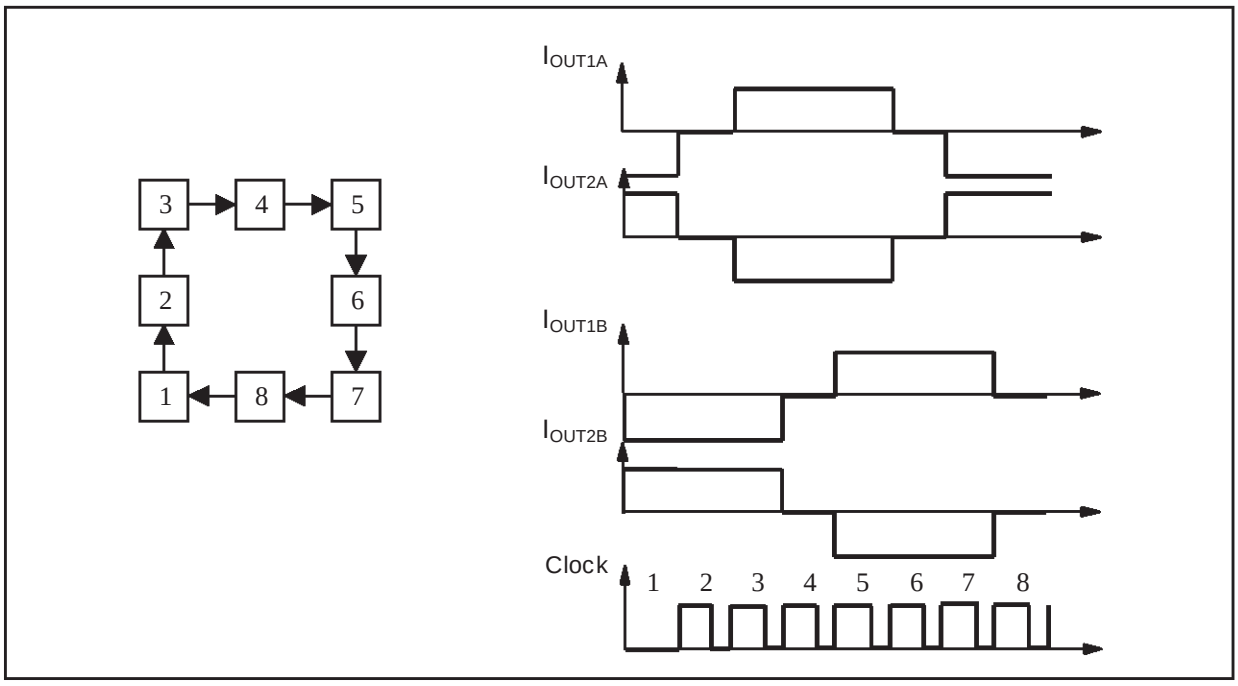


A non-dissipative current sensing on the high side power DMOSs, an internal reference and an internal open drain, with a pull down capability of 4mA (typical value), that goes LOW under fault conditions, ensure a protection against short circuit to GND or between two phases of each of the two full bridges. The trip point of this protection is internally set at 5.6 A (typ. value). By using an external R-C on the EN pins, the off time before recover normal operation conditions after a fault can be easily programmed, by means of the accurate threshold of the logic inputs. Note that protection against short to the supply rail is typically provided by the PWM current control circuitry.
These features make the L6208 a complete bipolar stepper motor driver that outperforms the components currently available on the market

MOTOR DRIVING PHASE SEQUENCE
The decoding logic integrated in the L6208 generates the sequences for normal drive, wave drive and half step modes. The state machine sequences and the output currents (neglecting, for simplicity, the PWM control) are shown below, in the case of clockwise rotation. For counterclockwise rotation the sequences are simply reversed. The state machine advances on the rising edge of the Clock signal, and a Low logic level on the Reset input restores the logic to state 1.

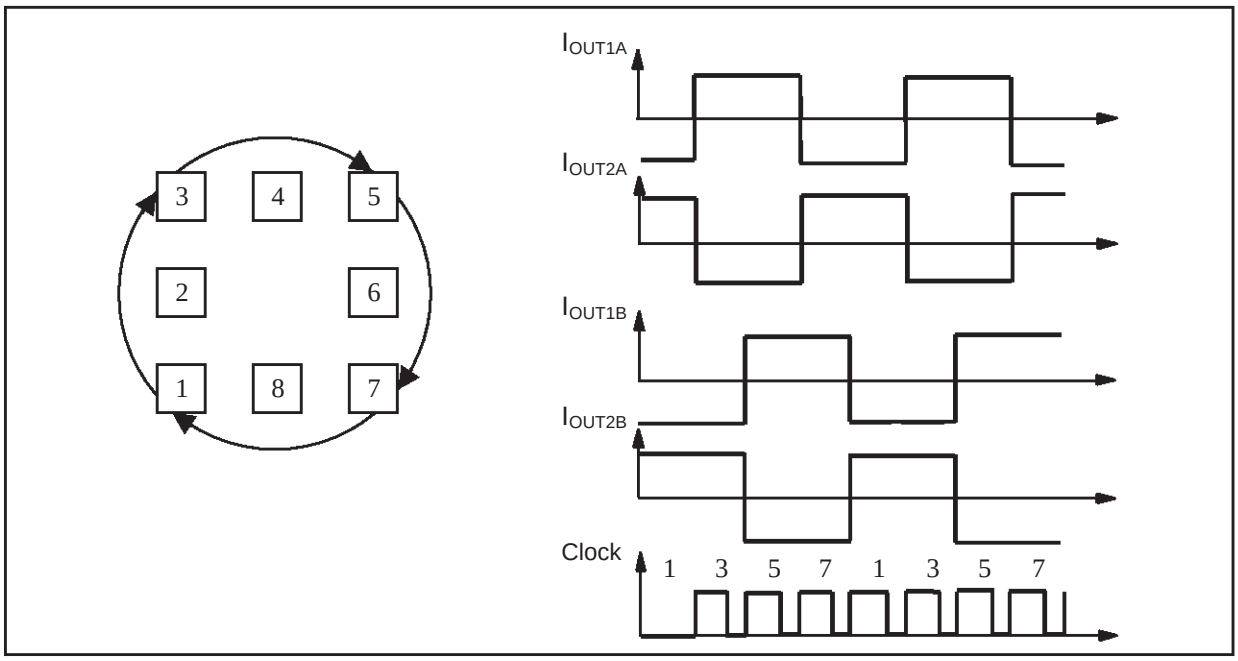
HALF STEP MODE
Half step mode is selected by a high logic level on the HALF/FULL pin.

Figure 11.



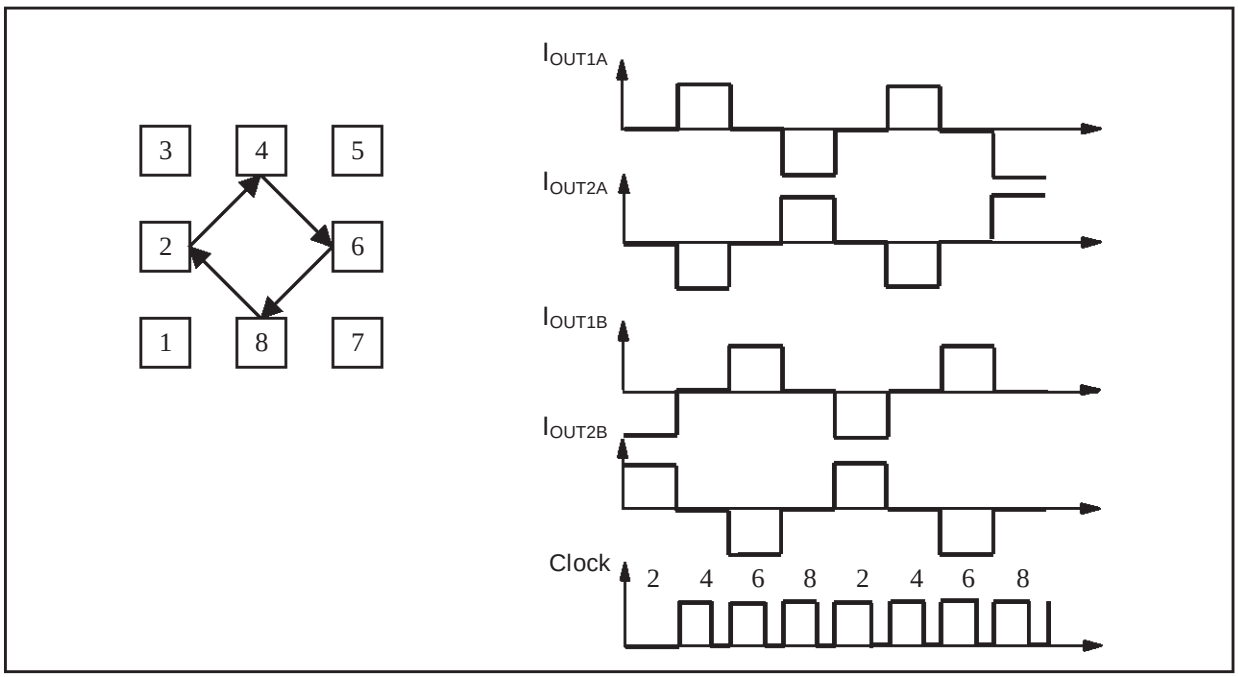
NORMAL DRIVE MODE (Full-step two-phase-on)
Normal drive mode is selected by a Low level on the HALF/FULL input when the state machine is at an odd numbered state.

Figure 12.



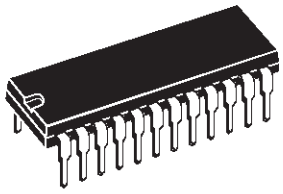
WAVE DRIVE MODE (Full-step one-phase-on)
Wave drive mode is selected by a Low level on the HALF/FULL input when the state machine is at an even numbered state.

Figure 13.

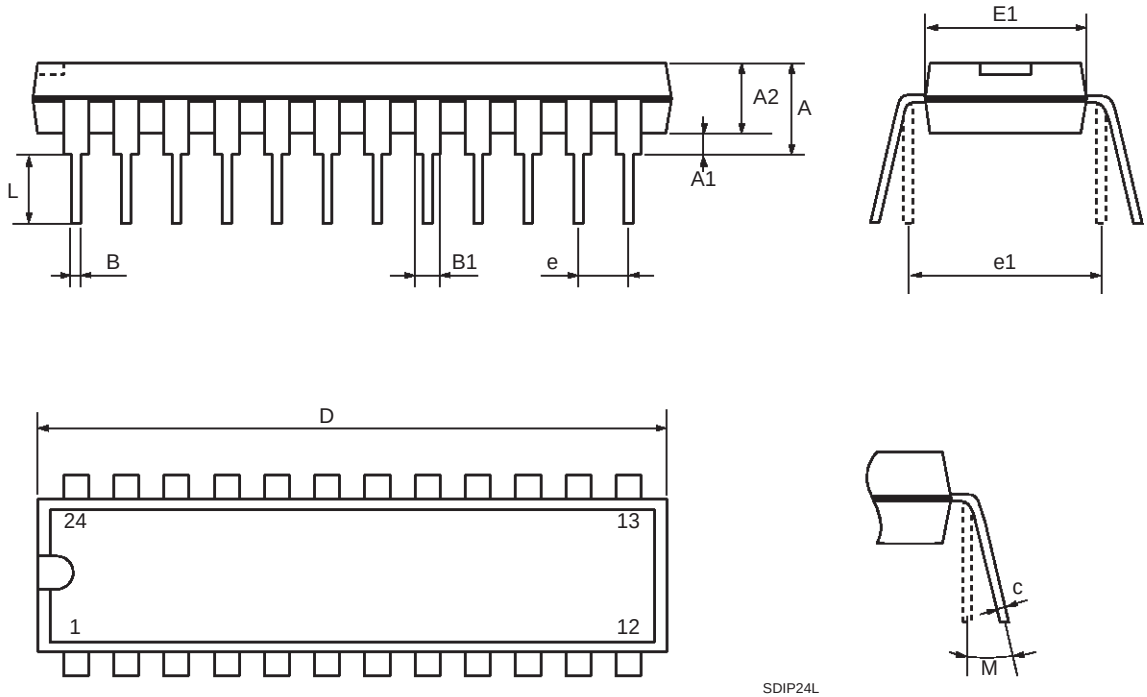


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.320			0.170
A1	0.380			0.015		
A2		3.300			0.130	
B	0.410	0.460	0.510	0.016	0.018	0.020
B1	1.400	1.520	1.650	0.055	0.060	0.065
c	0.200	0.250	0.300	0.008	0.010	0.012
D	31.62	31.75	31.88	1.245	1.250	1.255
E	7.620		8.260	0.300		0.325
e		2.54			0.100	
E1	6.350	6.600	6.860	0.250	0.260	0.270
e1		7.620			0.300	
L	3.180		3.430	0.125		0.135
M	0° min, 15° max.					

OUTLINE AND MECHANICAL DATA

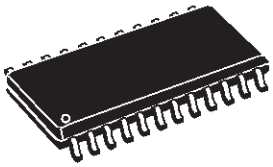


Powerdip 24

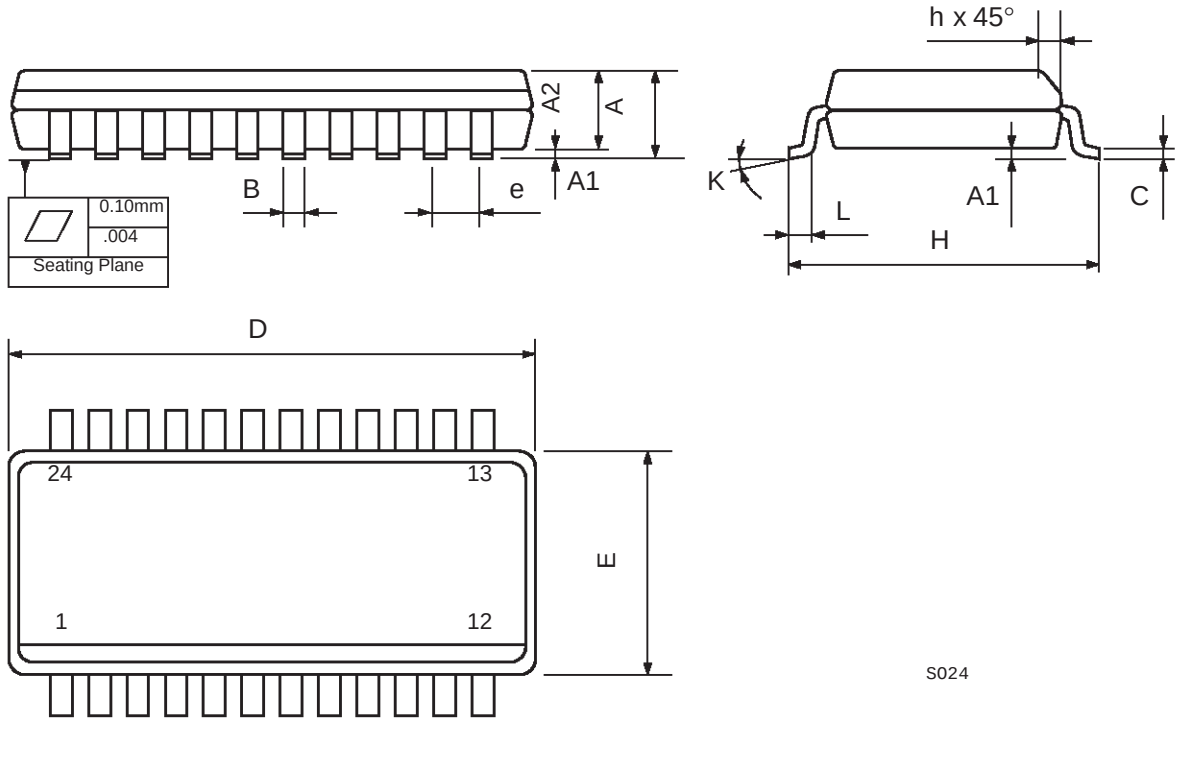


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
A2			2.55			0.100
B	0.33		0.51	0.013		0.0200
C	0.23		0.32	0.009		0.013
D	15.20		15.60	0.598		0.614
E	7.40		7.60	0.291		0.299
e		1.27			0,050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
k	0° (min.), 8° (max.)					
L	0.40		1.27	0.016		0.050

OUTLINE AND MECHANICAL DATA



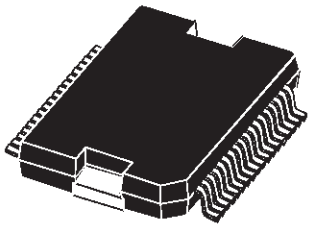
SO24



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.60			0.141
a1	0.10		0.30	0.004		0.012
a2			3.30			0.130
a3	0		0.10	0		0.004
b	0.22		0.38	0.008		0.015
c	0.23		0.32	0.009		0.012
D (1)	15.80		16.00	0.622		0.630
D1	9.40		9.80	0.370		0.385
E	13.90		14.50	0.547		0.570
e		0.65			0.0256	
e3		11.05			0.435	
E1 (1)	10.90		11.10	0.429		0.437
E2			2.90			0.114
E3	5.80		6.20	0.228		0.244
E4	2.90		3.20	0.114		0.126
G	0		0.10	0		0.004
H	15.50		15.90	0.610		0.626
h			1.10			0.043
L	0.80		1.10	0.031		0.043
N	10°(max.)					
S	8 °(max.)					

(1): "D" and "E1" do not include mold flash or protrusions
- Mold flash or protrusions shall not exceed 0.15mm (0.006 inch)
- Critical dimensions are "a3", "E" and "G".

OUTLINE AND MECHANICAL DATA



PowerSO36