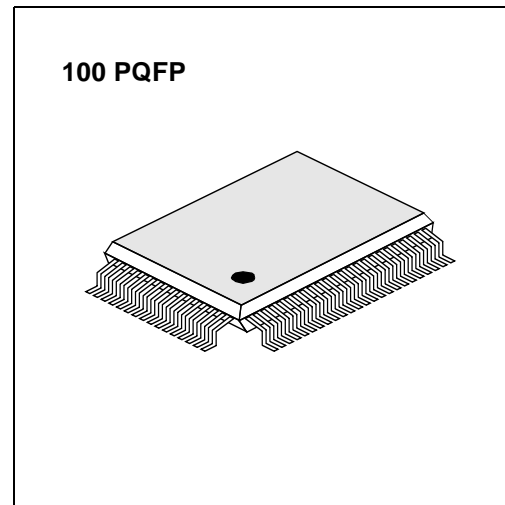


MULTISTANDARD VIDEO DECODER/SCALER

The KS0127B converts analog NTSC, PAL or SECAM video in composite, S-video, or component format to digitized component video. Output data can be selected for CCIR 601 or square pixel sample rates in either YCbCr or RGB formats. The digital video can be scaled down in both the horizontal and vertical directions. The KS0127B also decodes Intercast, Teletext, Closed Caption, and WSS data with a built-in bit data slicer. Digitized CVBS data can be output directly during VBI for external processing.

FEATURES

- Accepts NTSC-M/N/4.43, PAL-M/N/B/G/H/I/D/K/L and SECAM formats with auto detection
- 6 analog inputs: 3 S-video, 6 composite, or 1 3-wire YCbCr component video
- 2-line luma and chroma comb filters including adaptive luma comb for NTSC
- Programmable luma bandwidth, contrast, brightness, and edge enhancement
- Programmable chroma bandwidth, hue, and saturation
- High quality horizontal and vertical down scaler
- Intericast, Teletext and Closed Caption decoding with built-in bit slicer
- Direct output of digitized CVBS during VBI for Intericast application
- Analog square pixel or CCIR 601 sample rates
- Output in 4:4:4, 4:2:2, or 4:1:1 YCbCr component, or 24-bit or 16-bit RGB formats with dithering
- YCbCr 4:2:2 output can be 8 or 16 bits wide with embedded timing reference code support for 8-bit mode
- Simultaneous scaled and non-scaled digital output ports outputs for 8-bit mode.
- Direct access to scaler via bi-directional digital port.
- Programmable Gamma correction table
- Programmable timing signals
- Industry standard IIC interface



ORDERING INFORMATION

| Device | Package | Temperature Range |
|---------|----------|-------------------|
| KS0127B | 100 PQFP | -20°~+70°C |

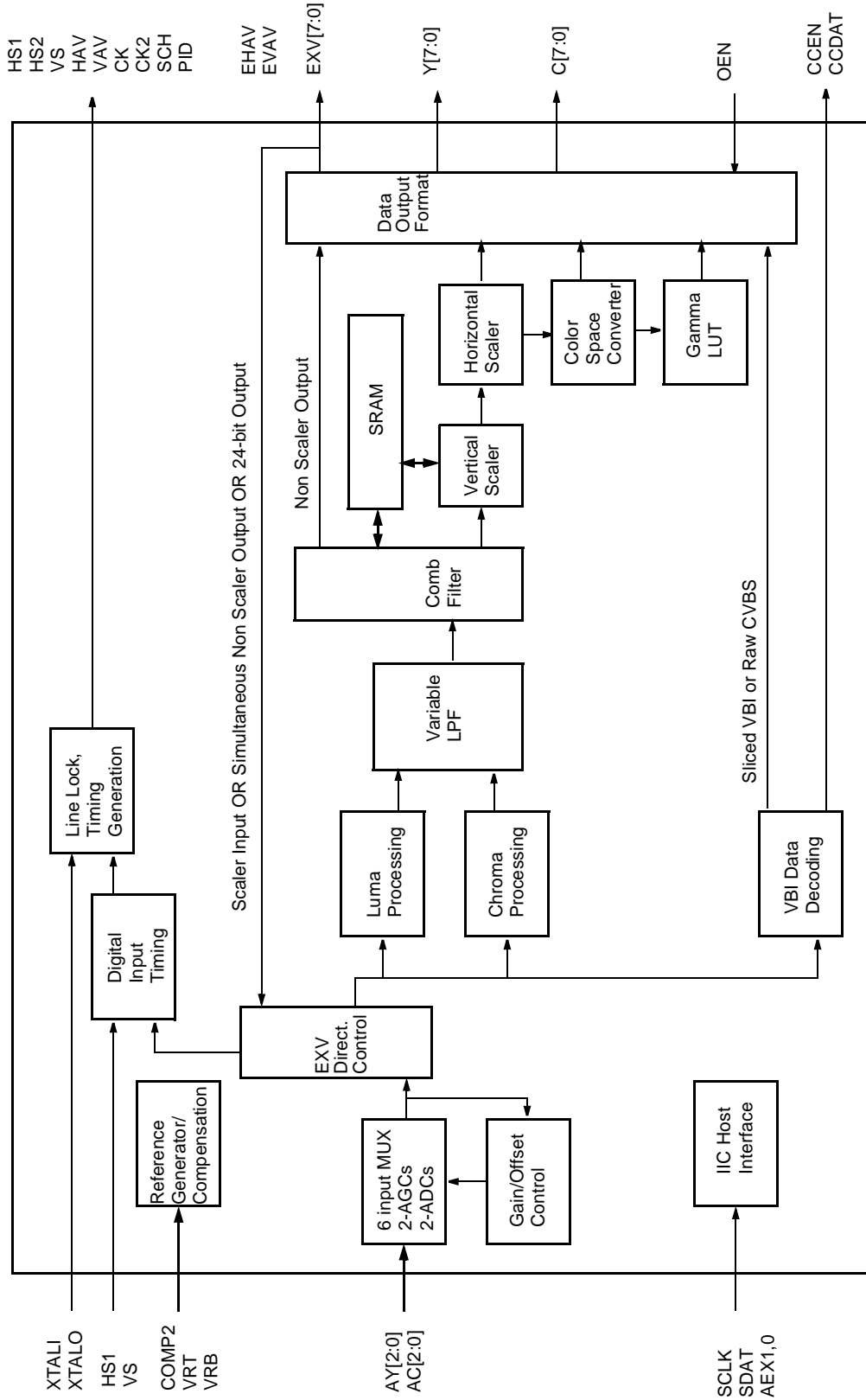
APPLICATIONS

- Multimedia
- Digital Video
- Video Capture/Editing

RELATED PRODUCTS

- KS0119Q2 NTSC VIDEO ENCODER
- KS0123 MULTISTANDARD VIDEO ENCODER
- KS0125 MULTISTANDARD VIDEO ENCODER
- KS0122 MULTISTANDARD VIDEO DECODER
- KS0127 MULTISTANDARD VIDEO DECODER

BLOCK DIAGRAM



PIN DESCRIPTION

| Pin Name | Pin # | Type | Description |
|-------------------------|-------|------|---|
| INPUT | | | |
| AY0 | 84 | I | 1 of 6 analog CVBS or 1 of 3 S-video Y inputs. |
| AY1 | 86 | I | 1 of 6 analog CVBS or 1 of 3 S-video Y inputs. |
| AY2 | 88 | I | 1 of 6 analog CVBS input or 1 of 3 S-video Y inputs or Y input for 3 wire component input |
| AC0 | 90 | I | 1 of 6 analog CVBS or 1 of 3 S-video C inputs. |
| AC1 | 92 | I | 1 of 6 analog CVBS or 1 of 3 S-video C inputs or Cb input for 3 wire component input |
| AC2 | 94 | I | 1 of 6 analog CVBS or 1 of 3 S-video C inputs or Cr input for 3 wire component input |
| XTALI | 8 | I | Pin 1 for an external crystal or TTL clock input. |
| XTALO | 7 | O | Pin 2 for an external crystal. |
| $\overline{\text{RST}}$ | 10 | I | Chip reset. Active low signal. |

OUTPUT (All output pins can be selectively three-stated)

| | | | |
|--------------------------------|----------------------|-----|--|
| Y0 - Y7, C0 - C7 | 45-48,53-56,33-39,44 | O | Digital video outputs. |
| EXV0 - EXV7 | 16,27,28,61-63,68,71 | I/O | Expanded digital video I/O port. Can be configured as an additional 8-bit output port (no scaling), or additional outputs of the main digital output stream for 24 bit output modes, as an 8-bit input for direct digital access of the down scaler. |
| HS1 | 26 | I/O | Programmable horizontal timing signal. One pulse every video line. When the EXV port is configured as an input, this pin can be programmed as an input. |
| HS2($\overline{\text{IIC}}$) | 76 | I/O | Programmable horizontal timing signal. One pulse every video line. At power up, this pin needs a 10 k Ω pull-down resistor to configure the chip to operate in IIC mode. |
| VS | 23 | I/O | Programmable vertical timing signal. When the EXV port is configured as an input, this pin can be programmed as an input. |
| HAV | 25 | O | Programmable horizontal active video flag. |
| VAV(OENC0) | 3 | I/O | Programmable vertical active video flag. During reset, the pin is an input and the logic state of this pin is latched into the OENC [0] register bit. Use a 10 k Ω resistor for pull-up or pull-down. |
| EHAV | 5 | O | Valid pixel data flag. Polarity is programmable. Active when output video data is valid. |

PIN DESCRIPTION (Continued)

| Pin Name | Pin # | Type | Description |
|-------------|-------|------|--|
| EVAV(OENC1) | 4 | I/O | Valid line flag. Polarity is programmable. Active when output video line is valid. During reset, the pin is an input and the logic state of this pin is latched into the OENC[1] register bit. Use a 10 k Ω resistor for pull-up or pull-down. |
| ODD | 22 | O | Odd field flag. Polarity is programmable. Active for fields 1 and 3. |
| PID | 17 | O | PAL ID flag. High for phase alternating line. |
| OEN | 15 | I | Digital video data, timing and clock output 3-state control. |
| CK | 18 | I/O | Pixel clock. In normal decoding mode, this is an output. When the EXV port is used as an input, this can be programmed as an input pixel clock. |
| CK2 | 21 | O | Pixel output clock (rate is one half of CK) aligned to HAV signal. |
| CCDAT | 73 | O | Sliced VBI data output. Data can be from Closed Caption, Teletext, Intercast, or WSS type encoded data. |
| CCEN | 74 | O | When high, this pin indicates that valid VBI data is being clocked out at the CCDAT pin or at the digital video output. |

MULTI-PURPOSE I/O PORTS AND TEST ENABLE

| | | | |
|------------|----|-----|--|
| PORTA | 58 | I/O | Multi-purpose I/O port. |
| SCH(PORTB) | 24 | I/O | Multi-purpose I/O port. |
| TESTEN | 57 | I | When tied to VDD, the chip is put into the test mode. For normal use, this pin should be connected to VSS. |
| TEST | 96 | I | When tied to VDD, the chip is put into the test mode. For normal use, this pin should be connected to VSS. |

REFERENCE AND COMPENSATION

| | | | |
|-------|----|-----|---|
| VRT | 77 | I/O | ADC VRT compensation (requires an external 0.1 μ F capacitor connected to VSS). |
| VRB | 78 | I/O | ADC VRB compensation (requires an external 0.1 μ F capacitor connected to VSS). |
| COMP2 | 97 | I/O | Internal 1.3 V reference (requires an external 0.1 μ F capacitor connected to VSS). |

HOST INTERFACE

| | | | |
|-------------|---------|-----|---|
| SCLK | 75 | I | Serial clock for IIC host interface. |
| SDAT | 72 | I/O | Serial data for IIC host interface. |
| AEX0 - AEX1 | 69 - 70 | I | Device ID selection for IIC host interface. |

PIN DESCRIPTION (Continued)

| Pin Name | Pin # | Type | Description |
|----------|-------|------|-------------|
|----------|-------|------|-------------|

POWER AND GROUND

| | | | |
|-------|---------------------------------------|-------|---|
| VDD | 20,59 | PWR | Digital power supply for output buffers. The voltage can be +5V or 3.3V depending on interface requirement. |
| VDD3 | 11,12,42,43,66,67 | +3.3V | Digital power supply for internal logic. |
| VDDA | 85,89,93,98 | +5V | Analog power supply for ADC, AGC and reference circuits. |
| VDDA1 | 9 | +5V | Analog power supply for clock generation circuitry. |
| VSS | 6,13,14,19,40,41,60,64,65,83,87,91,95 | GND | Common ground. |

NC

| | | | |
|-----|------------------------------|---|--|
| NCP | 1,2,29-32,49-52,79-82,99,100 | - | These pins are directly connected to the die substrate. If electrical connect is desired (not required) only connection to VSS is allowed. |
|-----|------------------------------|---|--|

PIN CROSS REFERENCE: NUMERICAL ORDER BY PIN NUMBER

| Pin # | Pin Name | Pin # | Pin Name | Pin # | Pin Name | Pin # | Pin Name |
|-------|-------------|-------|----------|-------|----------|-------|----------|
| 1 | NCP | 26 | HS1 | 51 | NCP | 76 | HS2(IIC) |
| 2 | NCP | 27 | EXV1 | 52 | NCP | 77 | VRT |
| 3 | VAV(OENC0) | 28 | EXV2 | 53 | Y4 | 78 | VRB |
| 4 | EVAV(OENC1) | 29 | NCP | 54 | Y5 | 79 | NCP |
| 5 | EHAV | 30 | NCP | 55 | Y6 | 80 | NCP |
| 6 | VSS | 31 | NCP | 56 | Y7 | 81 | NCP |
| 7 | XTALO | 32 | NCP | 57 | TESTEN | 82 | NCP |
| 8 | XTALI | 33 | C0 | 58 | PORTA | 83 | VSS |
| 9 | VDDA1 | 34 | C1 | 59 | VDD | 84 | AY0 |
| 10 | RST | 35 | C2 | 60 | VSS | 85 | VDDA |
| 11 | VDD3 | 36 | C3 | 61 | EXV3 | 86 | AY1 |
| 12 | VDD3 | 37 | C4 | 62 | EXV4 | 87 | VSS |
| 13 | VSS | 38 | C5 | 63 | EXV5 | 88 | AY2 |
| 14 | VSS | 39 | C6 | 64 | VSS | 89 | VDDA |
| 15 | OEN | 40 | VSS | 65 | VSS | 90 | AC0 |
| 16 | EXV0 | 41 | VSS | 66 | VDD3 | 91 | VSS |
| 17 | PID | 42 | VDD3 | 67 | VDD3 | 92 | AC1 |
| 18 | CK | 43 | VDD3 | 68 | EXV6 | 93 | VDDA |
| 19 | VSS | 44 | C7 | 69 | AEX0 | 94 | AC2 |
| 20 | VDD | 45 | Y0 | 70 | AEX1 | 95 | VSS |
| 21 | CK2 | 46 | Y1 | 71 | EXV7 | 96 | TEST |
| 22 | ODD | 47 | Y2 | 72 | SDAT | 97 | COMP2 |
| 23 | VS | 48 | Y3 | 73 | CCDAT | 98 | VDDA |
| 24 | SCH(PORTB) | 49 | NCP | 74 | CCEN | 99 | NCP |
| 25 | HAV | 50 | NCP | 75 | SCLK | 100 | NCP |

1. FUNCTIONAL DESCRIPTION

1.1. VIDEO INPUT

The KS0127B supports complete video decoding of many analog video standards. In addition, the chip can support direct 8-bit YCbCr input for high quality video scaling and other processing.

1.1.1. Analog Video Input

Figure 1 shows the detailed block diagram of the analog front end. Up to six composite video sources, three S-video sources, one 3-wire YCbCr component video source, or any combination can be selected. The allowed inputs are selected using the **INSEL[3:0]** bits in the **CMDB** register. Table 1 lists all possible input selections. The front end has two paths each containing an analog gain control, a clamping control, and an 8-bit ADC. Composite video input uses only the luma path. S-video and analog component YCbCr inputs utilize both the luma and chroma paths. The ADC digital data is used to calculate the correct gain and clamp values. The data is feedback to the analog clamping and gain control. This architecture eliminates any offset and gain mismatch in the analog front end.

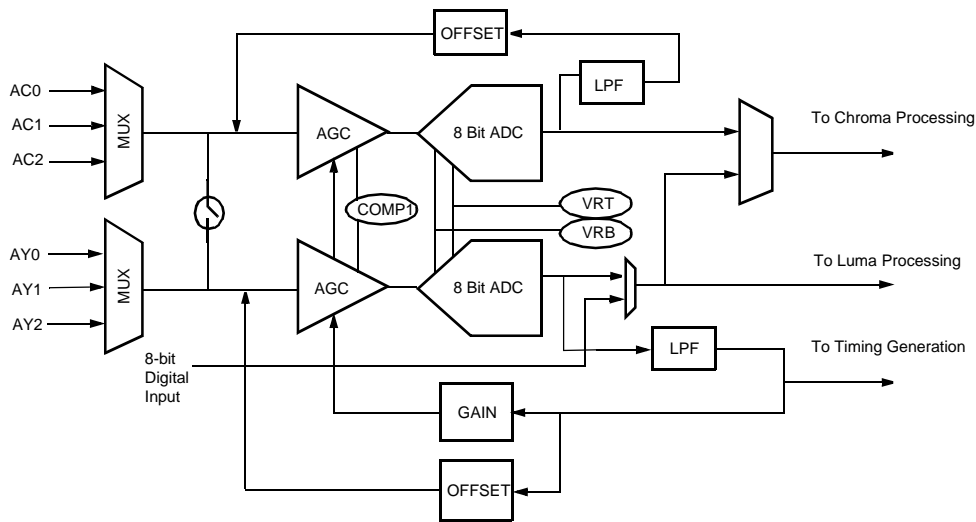


Figure 1. Analog Front End

The analog inputs must be AC coupled through an external 0.1 μF capacitor clamp. Due to the high sampling rate of the ADCs inside the KS0127B, most video sources will not require a low-pass filter for alias reduction. For those video sources with harmonics above 13 MHz, a simple single order pole at 6 MHz will provide sufficient high frequency signal reduction. This can be implemented with a 400 pF capacitor in parallel with the 75 Ω load.

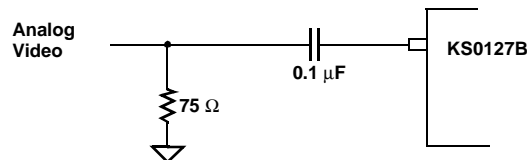


Figure 2. Typical Analog Video Input

Table 1: Analog Video Input selections

| INSEL[3:0](hex) | Selected Input(s) | Video Type |
|-----------------|--------------------------|-----------------------|
| 0 | AY0 | Composite |
| 1 | AY1 | Composite |
| 2 | AY2 | Composite |
| 4 | AC0 | Composite |
| 5 | AC1 | Composite |
| 6 | AC2 | Composite |
| 8 | AY0, AC0 | S-Video |
| 9 | AY1, AC1 | S-Video |
| A | AY2, AC2 | S-Video |
| F | AY2(Y), AC1(Cb), AC2(Cr) | YCbCr component video |

1.1.2. Digital AGC Control

The AGC normally references to the ADC code difference between sync tip and back porch. Two sets of sync tip-back porch ADC values are available for different AGC gain requirements: if **AGCGN** = 0, the sync tip locks to code 2, and the back porch locks to code 70; when **AGCGN** = 1, the sync tip locks to 16, and the back porch locks to code 70. Video signal with abnormal sync tip or very bright saturated colors may cause the ADC to limit the maximum value. This situation can be corrected by enabling the **AGCOVF** bit in the **CMDB** register to force the gain tracking loop to reduce AGC when maximum limiting conditions occur. The AGC may also be programmed to freeze the AGC at the current value by setting the **AGCFRZ** bit in the **CMDB** register. Once the AGC is frozen, the gain can be manually adjusted with the **AGC** register. The tracking time constant for the AGC can be controlled with the **AGC_LPG[1:0]** bits in the **TRACKB** register. In addition, the AGC tracking time constant can be configured as 2X faster during acquisition via the **AGC_LKG**.

1.1.3. Digital Video Input

The high quality digital video down scaler in the KS0127B can be directly accessed via the EXV bi-directional port. The KS0127B accepts CCIR 656 compliant 8-bit YCbCr digital video input with embedded or external timing. Video timing may also be generated by the KS0127B. Data path for 8-bit YCbCr input is shown in Figure 3. Selection of analog video input or digital CCIR 656 data is with the **INPSL[1:0]** register bits. The KS0127B can operate in master or slave timing mode when the chip is programmed for digital video input.

1.1.4. Pixel Clock and Timing Mode Selection for Digital Video Input

Pixel clock and synchronization timing can be individually selected to either come from an external generator or be generated internally. In addition, if synchronization is provided by an external source, the KS0127B supports embedded syncs as defined in CCIR 656, or TTL HS and VS inputs. Selection of pixel clock is via **CKDIR** bit in

CMDD register. Timing selection is through either SYNDIR or EAV bit.

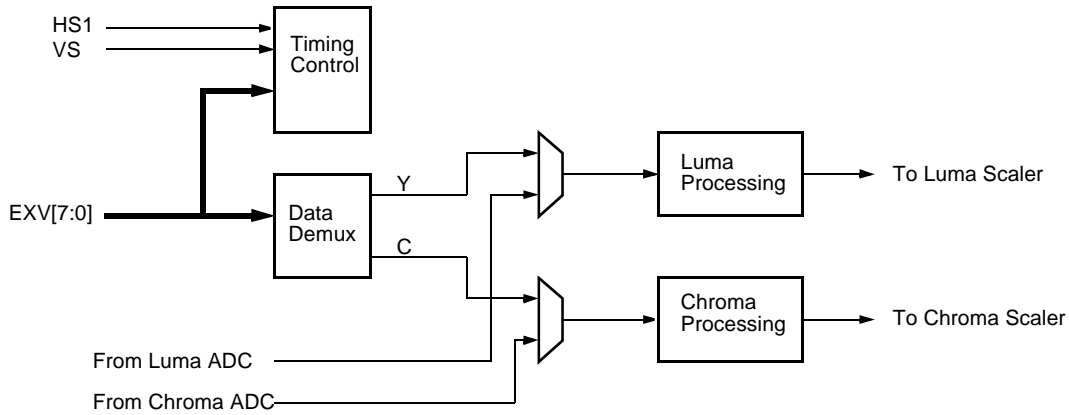


Figure 3. 8-bit YCbCr Input Data Path

By using an external pixel clock, the reference clock input at XTALI is no longer required. Additional register bits have to be programmed for different selections of pixel clock and timing, which are detailed in Table 2. The following register/bit-settings are required for digital video input:

- INSEL[3:0] = 8, 9, A, or F.
- TSTCGN = 1.
- DMCTL[1:0] = 2 or 3.
- UGAIN = 238.
- BRT = 34.
- SAT = 229.
- RGBH = UNIT = PED = 1.

Table 2: Digital Video Input Pixel Clock and Timing Selection

| Pixel Clock | TTL Timing | Embedded Timing | Additional Register Programming | | | | | | |
|-------------|------------|-----------------|---------------------------------|----------------------|-------------------|------|---|--------|--|
| | | | CKDIR ^{*1} | SYNDIR ^{*2} | EAV ^{*3} | VMEN | TSTGPH | TSTGEN | TSTGFR |
| 0 | 0 | 0 | 1 | 0 | 1 | 3 | 0 if input data is at square pixel rate. 1 if input is at CCIR 601 rate. | 1 | 0 if input is 50 Hz video. 1 if input is 60 Hz video. |
| 0 | 0 | 1 | 0 | 1 | 1 | 3 | | 1 | |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | | 1 | |
| 1 | 0 | 0 | 1 | 0 | 1 | 3 | | 1 | |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | | 1 | |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | | 1 | |

*1: CKDIR = 0 - CK is output and is internally generated. CKDIR = 1 - CK is input from an external source.

*2: SYNDIR = 0 - HS1 and VS are output. SYNDIR = 1 - HS1 and VS are inputs from external sources.

*3: EAV = 0 - chip will not sync to embedded timing. EAV = 1 - chip will sync to embedded timing.

Note: the combination X11 for CKDIR, SYNDIR, EAV is not valid.

When in digital input mode, all programmable timing registers (such as HAVB, HAVE, HS2B etc.) are still functional. If HS1 and VS are programmed as inputs, the associated output timing controls such as HS1B,E will have no effect. An example of horizontal timing for digital input is shown in Figure 4.

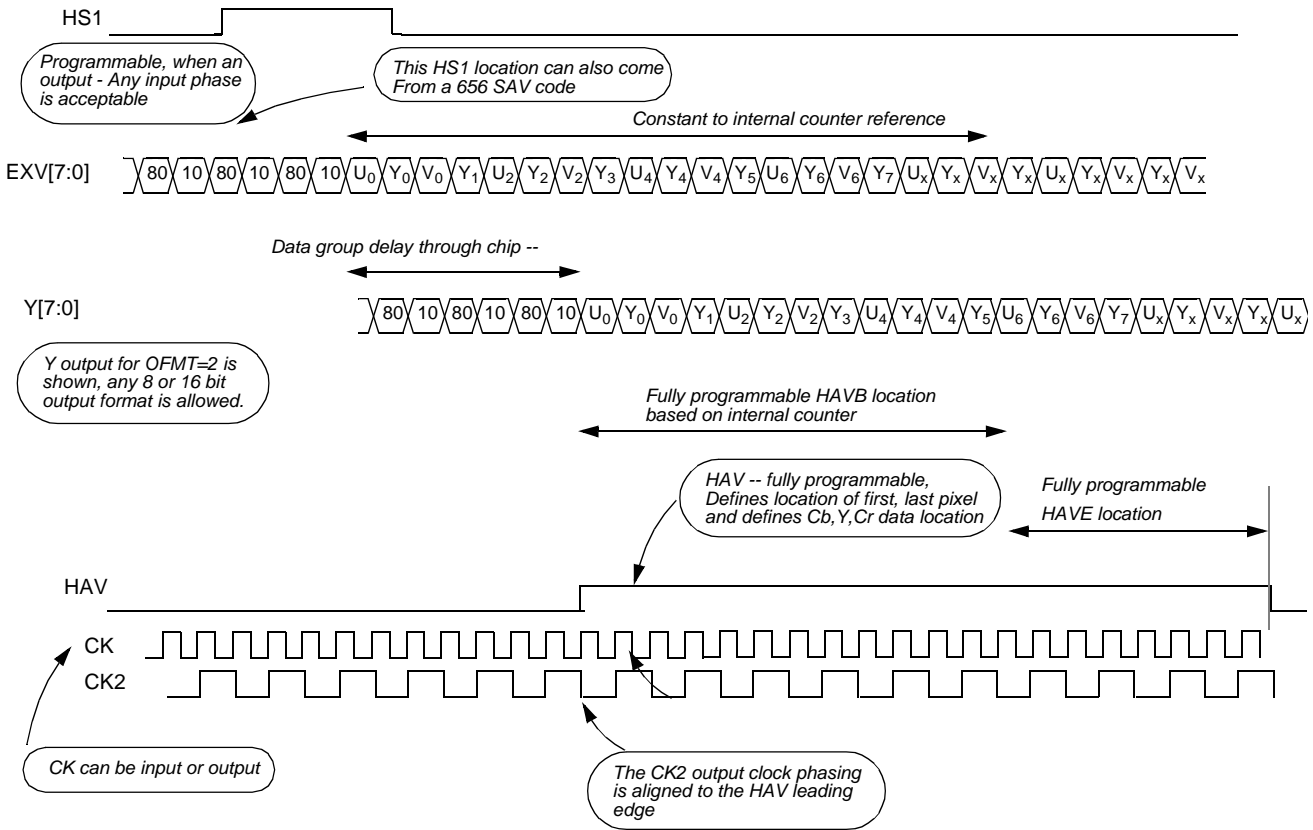


Figure 4. Horizontal Timing for EXV Port as Digital Input

1.1.5. Additional Information for Analog Component Video Input

For the KS0127B to correctly set the V component phase in analog component video input mode, PID (pin 17) and PORTA (pin 58) need to be connected together. PORTA has to be configured as input (**DIRA** = 0) and connected to the internal CBG signal (**DATAA**[2:0] = 3).

It is also recommended that external clamp circuit be used for Cb and Cr inputs (before the coupling caps) and the internal chroma clamp be disabled (**COFFENB** = 1) due to slight Cb/Cr leakage.

1.2. VIDEO TRACKING AND TIMING GENERATION

When the KS0127B is configured for analog video input, the chip tracks the video input and generates a sampling clock that is line locked to the input video. The KS0127B requires an external reference clock for video tracking. This reference can be supplied via a crystal using the on chip crystal interface or any TTL compatible source. These configurations are shown in Figure 5

1.2.1. Clock Input Timing Reference

The KS0127B can use either a 24.576 MHz or a 26.8 MHz reference. However, it is recommended that the 24.576 MHz reference be used for CCIR 601 operation, and the 26.8 MHz reference be used for square pixel or dual mode operation. Other specifications for the crystal are:

- Fundamental or third overtone
- Load capacitance of ~20 pF
- Series resistance of 40 Ω or less
- Frequency deviation of 50 ppm or less over operating temperature range

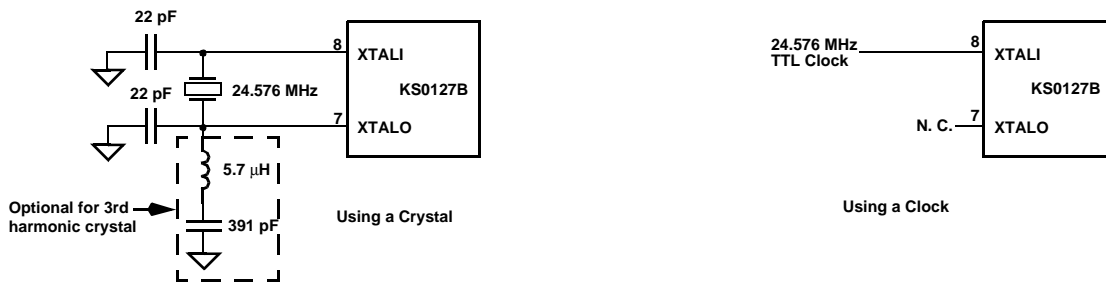


Figure 5. Standard Clock Configurations

1.2.2. The Sampling Clock

The sampling clock is generated by multiplying the line rate by N. This ensures that samples are aligned horizontally, vertically and in time. The required N factor for the KS0127B is based upon the field rate (60 Hz or 50 Hz) and the desired sampling rates (CCIR 601 or square pixel). Field rate can be automatically detected and can be monitored with the **FFRDET** bit in the **STAT** register. Manual control of the field rate can be controlled with the **MNFMT** and **IFMT** bits. The **PIXSEL** bit in register **CMDA** selects CCIR 601 or square pixel. Table 3 shows the constants for the various combinations of input formats and output pixel rates.

Table 3: Timing for Different Pixel Rates

| | CCIR 601 Data Rates | | Square Pixel Data Rates | | Units |
|--------------------|---------------------|--------------------|-------------------------|--------------------|--------|
| | M | N,B,G,H,I,D,K,K1,L | M | N,B,G,H,I,D,K,K1,L | |
| Field Rate | 60 | 50 | 60 | 50 | Hz |
| Pixels/Line (N) | 858 | 864 | 780 | 944 | Pixels |
| Active Pixels/Line | 720 | 720 | 640 | 768 | Pixels |
| Active Lines/Frame | 480 | 580 | 480 | 580 | Lines |
| Pixel Rate | 13.5 | 13.5 | 12.27 | 14.75 | MHz |
| ADC Sampling Rate | 27 | 27 | 24.54 | 29.5 | MHz |

The time constants for the pixel clock tracking loop can be adjusted with the **HFSEL**[1:0] bits.

In addition to providing the pixel clock, the KS0127B also outputs various timing signals to indicate the beginning of a line, a field, and for field and frame identification. All the timing and clock pins may be optionally put into high impedance state. Three-state of these pins are software controlled and initial state of these pins at power up is controlled via two configuration pins: 3 and 4.

The KS0127B can generate all the video timing without video input. This enables the KS0127B to be used as a video timing generator for a system that contains both the KS0127B for live video input and a MPEG decoder which requires a video timing generator.

1.2.3. Horizontal Timing

The KS0127B creates many internal timing signals aligned to the horizontal sync tip (mid-way of the falling edge of horizontal sync, typically ADC code 36). These include locations of color burst (CBG, CBGW) used in chrominance processing, back porch (BPG), and sync tip timing signals (SLICE, FS_PULSE) used for AGC and clamp functions. SLICE is low whenever the input is below half way level of horizontal sync (typically ADC code 36). FS_PULSE is a single clock pulse coincide with the start of SLICE. One of these internal signals can be made available at the PORTA or PORTB pin at any time.

The chip outputs two horizontal synchronization signals: HS1 and HS2. The start and stop locations for these signals are fully programmable. Offset programmed to **HSxB**, **HSxE**, and **HSxBE0** are added to the default edge locations as shown in Table 4. Note that there are different modulo numbers for different input video standards and output pixel rates.

Table 4: Horizontal Timing Signal Edge Locations (in # of CK)

| Description | Signal | 60 Hz | | 50 Hz | |
|---------------------------------------|--------|---------------------------|-------------------------------|---------------------------|-------------------------------|
| | | CCIR 601 (modulo 1716) | Square Pixel (modulo 1560) | CCIR 601 (modulo 1728) | Square Pixel (modulo 1888) |
| Chip delay | | 120 | 120 | 120 | 120 |
| Sync gate (1-CK pulse) | SYG | 72 | 72 | 72 | 72 |
| Back porch gate | BPG | [147 222] | [129 204] | [154 234] | [168 254] |
| Color burst gate (1-CK pulse) | CBG | 222 | 204 | 234 | 254 |
| Wide color burst gate | CBGW | [159 254] | [147 233] | [173 254] | [186 277] |
| Two pulses per line (1-CK each pulse) | FH2 | 42, 900 | 42, 822 | 42, 906 | 42, 986 |
| Default one pulse per line | HS1 | [65 238] | [45 220] | [69 250] | [65 270] |
| Default one pulse per line | HS2 | [65 238] | [45 220] | [69 250] | [65 270] |
| Default horizontal cropping | HAV | [351 75] | [334 58] | [379 91] | [415 59] |

An additional signal, HAV, is provided for horizontal video cropping. This signal has programmable polarity, start and stop locations. Two 11-bit registers, **HAVB** and **HAVE**, are used to define the first and last pixel locations of the horizontal portion of the cropped video. Numbers programmed into these registers are used as offset to the default locations as shown in Table 4. Note that even though **HAVB** and **HAVE** have 1-CK resolution, the difference between them should be maintained at multiple of 4 CKs for correct output.

Table 4 shows the default edge locations relative to the midway of the falling edge of the analog horizontal sync. Note the numbers shown are in multiple of CK clocks. Figure 6 shows the approximate locations for the horizontal timing signals. Horizontal timing signals used for scaling will be described in Section 1.6.1.

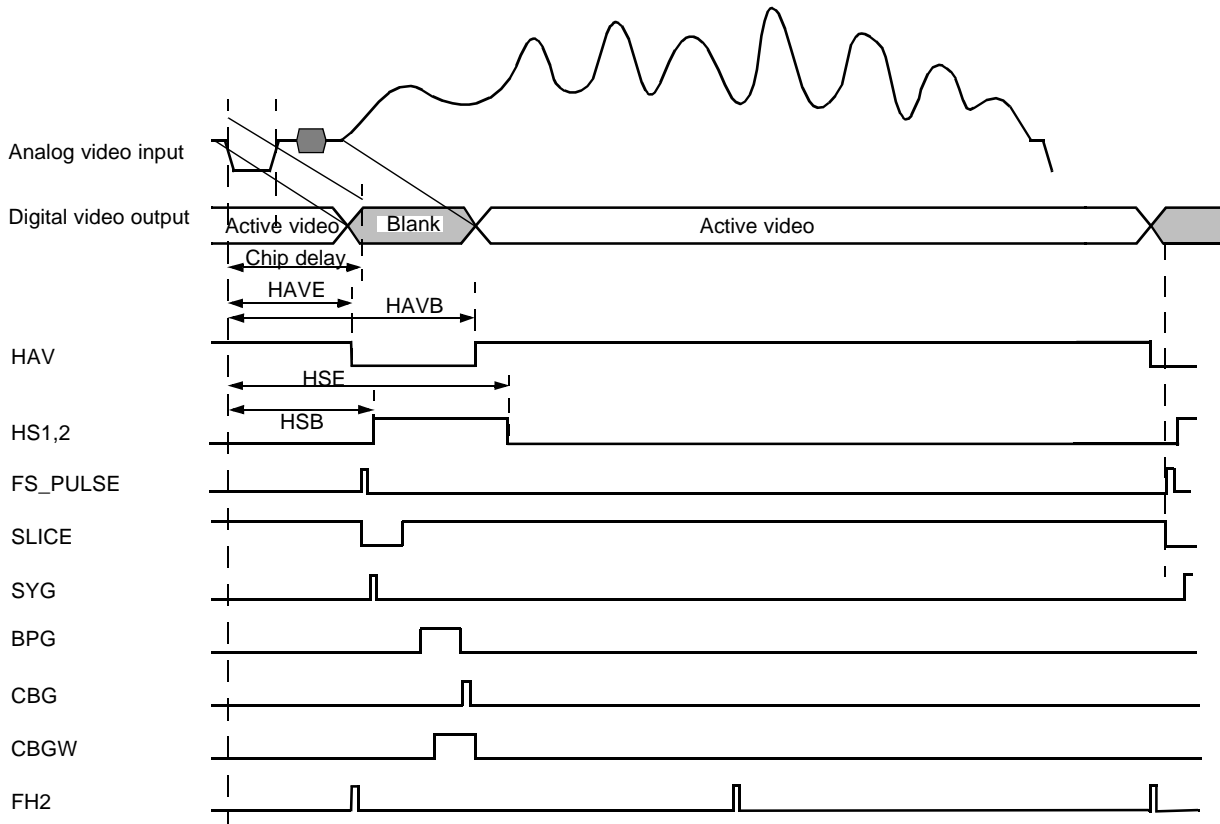


Figure 6. Approximate Locations for the Horizontal Timing Signals

1.2.4. Vertical Timing

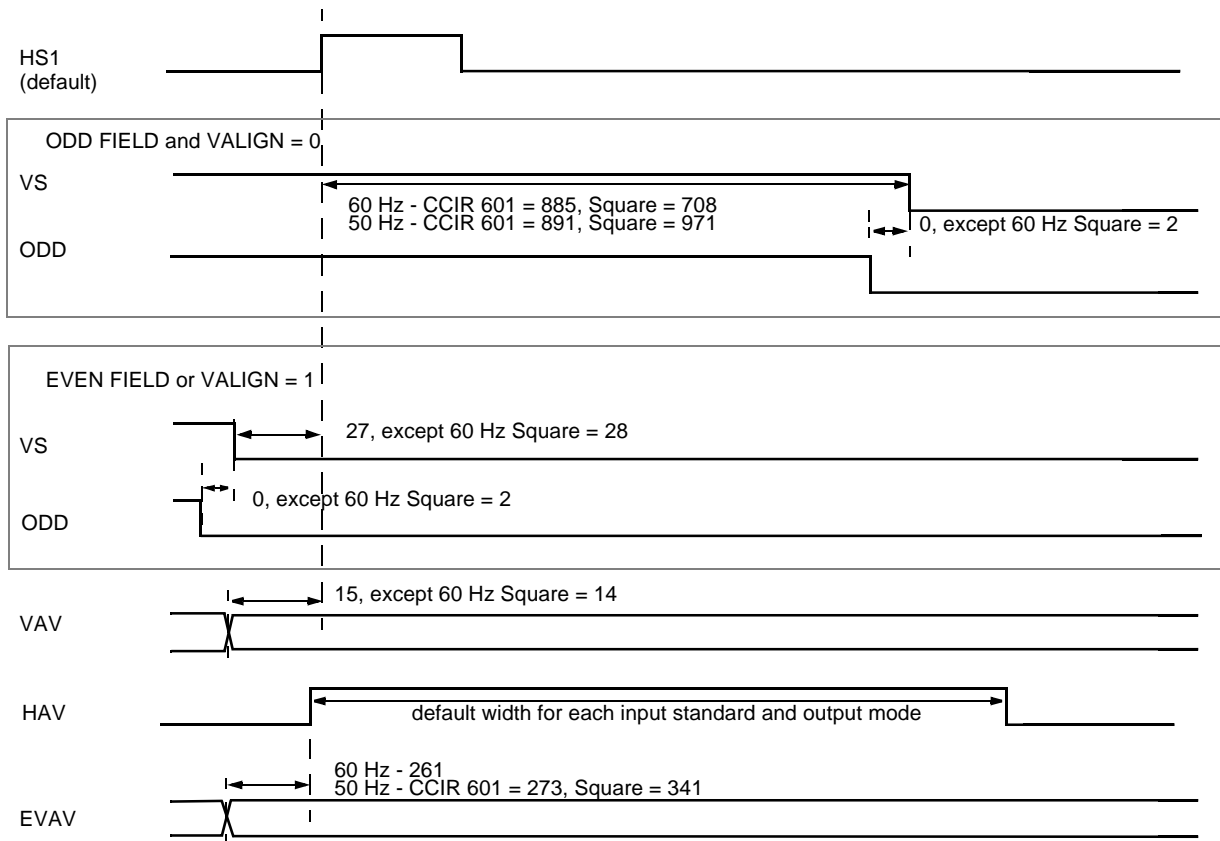
The vertical timing signals include VS, VAV, ODD, SCH, and PID.

The VS is used for identifying the first line of video in the vertical position. The VS leading edge can be programmed to either track the incoming video's serration pulses or to be aligned to the beginning of the video line or half way, as shown in Figure 36 and Figure 37. If **VALIGN** = 0, the VS leading edge is based on the output of an internal low pass filter, and its location is dependent on the noise conditions of the video input. The trailing edge of VS is locked to either the beginning of the video line or half way. The half way location relative to the beginning of the video line changes depending on current input standard and output format. If **VALIGN** = 1, the leading edge of the VS is aligned to the beginning of the video line or half way. The trailing edge is always aligned to the beginning of the video line. The **VSE** bit in the **CMDA** register can be programmed to shorten the VS falling edge by one horizontal line.

The VAV signal is used for vertical cropping. The start and stop lines for VAV are programmable through the **VAVB** and **VAVE** registers, respectively.

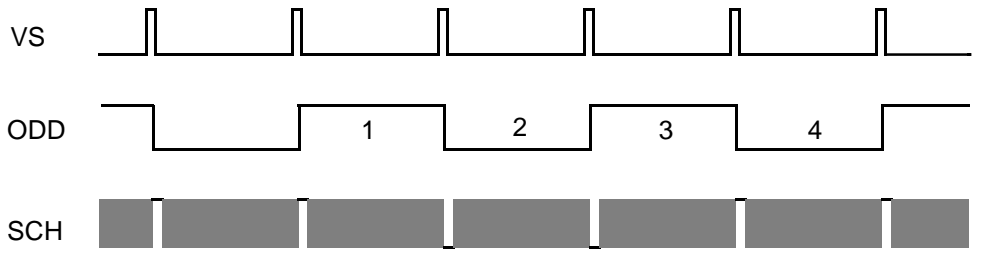
The ODD signal signifies the current field number. When ODD is active, the current field is 1 or 3 (or 5 or 7 if in PAL mode). The leading and trailing edges of ODD can be aligned to either the leading edge of VS (**VALIGN** = 1) or the trailing edge of VS (**VALIGN** = 0). The signal may be used in conjunction with SCH and PID to exactly identify the

current field. To distinguish between fields 1, 2 verse fields 3, 4 (or fields 1, 2, 3, 4 verse fields 5, 6, 7, 8 for PAL) the phase of the color burst relative to the sync tip must be measured. That information is provided by the SCH pin. The KS0127B provides the output of a comparator that measures whether the current color burst phase relative to the falling edge of the sync is greater or less than a predetermined constant. This constant is controlled with **SCHCMP[3:0]**. The polarity of the SCH output pin depends on the current **SCHCMP[3:0]** value. The SCH signal changes every video line. The SCH for line 260 is held for the entire vertical blanking period. By using the SCH signal for the same line from each field, proper field identification can be determined. Figure 8 shows field identification values for **SCHCMP[3:0]=0**. It is important to note that the SCH value is only valid for video signals that have a constant sync tip to color burst relationship. This is not the case with consumer VCRs.



Note: Numbers shown are in CK. Active high polarities are used. Timing shown for VAV and EVAV are with qualifier off.

Figure 7. Short Term Vertical Timing



Truth Table

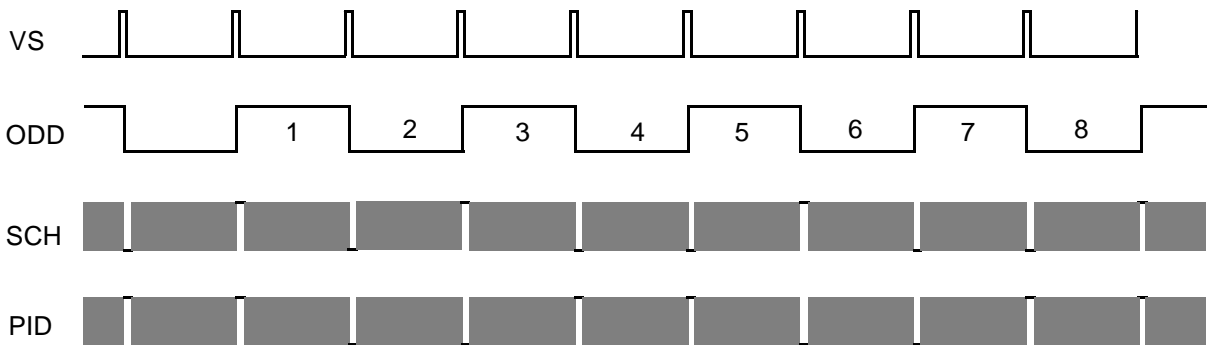
| | | | | |
|-------|---|---|---|---|
| FIELD | 1 | 2 | 3 | 4 |
| ODD | H | L | H | L |
| SCH | H | L | L | H |

Note:
ODD and SCH are measured at the trailing edge of VS.

Figure 8. NTSC Vertical Timing Signals

The PID pin is used to identify whether the current V-axis is inverted in PAL mode. This signal changes at the color burst. By noting this value at the same line of each field, a determination of whether a field is from {1-4} or {5-8} can be made. As with the SCH pin, the KS0127B is designed to hold the line 260 PID measurement for the entire vertical blank period. This allows easy sampling of the PID or current field identification.

The ODD, SCH and PID signals change at different times and more than once within the video fields. Proper data for field identification is determined by latching all three signals at the trailing edge of VS. Figure 9 shows the VS, ODD, SCH, and PID signals and their latched values for each of the 8 possible fields. Figure 10 is the line to line timing diagram for these signals in PAL mode.



Truth Table

| | | | | | | | | |
|-------|---|---|---|---|---|---|---|---|
| FIELD | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| ODD | H | L | H | L | H | L | H | L |
| SCH | H | L | H | L | L | H | L | L |
| PID | H | L | L | H | H | L | L | H |

Note:
ODD, SCH and PID are measured at the trailing edge of VS (VALIGN = 0).

Figure 9. PAL Vertical Timing Signals

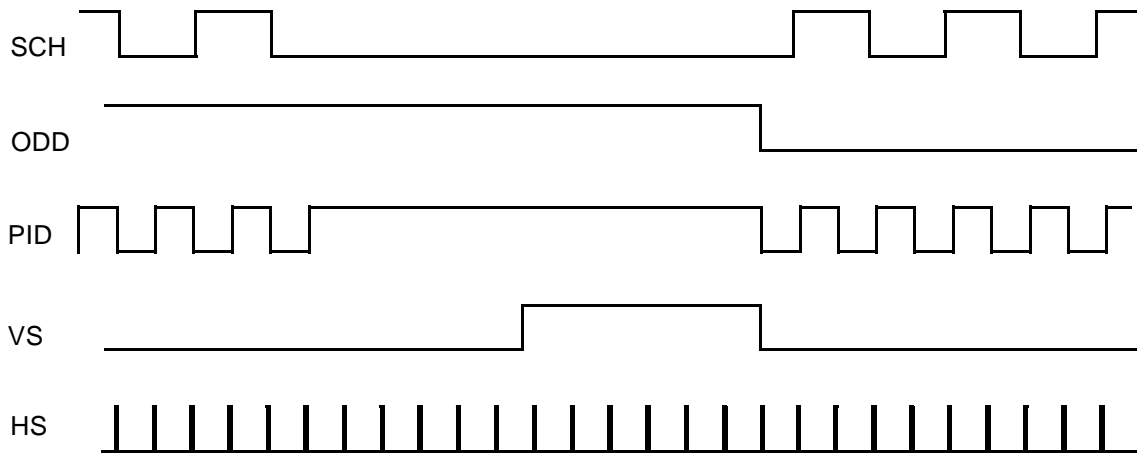


Figure 10. Line to Line VS, SCH and PID Timing (PAL input)

1.3. HORIZONTAL LUMA PROCESSING

A simplified block diagram for the luma path is shown in Figure 11.

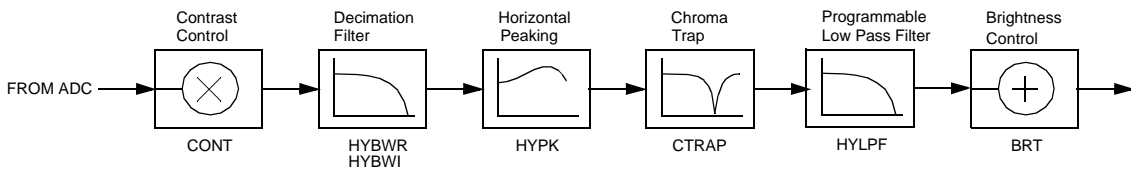


Figure 11. Horizontal Luma Processing Unit

1.3.1. Luminance DC Gain

The KS0127B can accommodate CCIR 624 M/N/H/G standards, which fall into categories of -40 or -43 sync tip and inclusion or exclusion of 7.5 setup. The KS0127B can produce correct CCIR 601 luminance output levels by controlling the gain and offset in the luminance path via **PED**. This register should be set for the appropriate input standard. The programmable **CONT** and **BRT** registers provide the user with additional flexibility to create non-standard luminance gain and offset values.

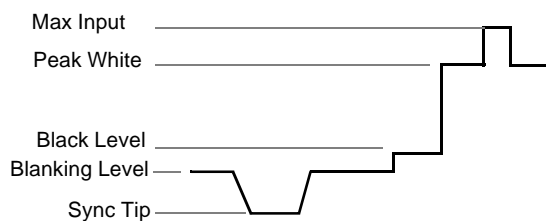


Figure 12. Luminance Signal

Luminance levels produced by the KS0127B for different broadcast standards (assuming **AGCGN=0**, **CONT=0** and **BRT=0**) are summarized in Table 5.

Table 5: Luminance Digital Level Code

| Signal | M/N PED=1 | | | M/N PED=0 | | | B/G/H PED=1 | | |
|----------------------------|----------------------|------------|--------|----------------------|------------|--------|---------------------|------------|--------|
| | Level (IRE) | ADC (CVBS) | Y[7:0] | Level (IRE) | ADC (CVBS) | Y[7:0] | Level (IRE) | ADC (CVBS) | Y[7:0] |
| Max Input | 109 | 255 | 255 | 109 | 255 | 255 | 117 | 255 | 255 |
| Peak White | 100 | 240 | 235 | 100 | 240 | 235 | 100 | 229 | 235 |
| Black | 7.5 | 83 | 16 | 0 | 70 | 16 | 0 | 70 | 16 |
| Blank | 0 | 70 | 1 | 0 | 70 | 16 | 0 | 70 | |
| Sync | -40 | 2 | 1 | -40 | 2 | 1 | -43 | 2 | |
| KS0127B Data Path Equation | $C_Y = 1.37CVBS-100$ | | | $C_Y = 1.288CVBS-74$ | | | $C_Y = 1.37CVBS-80$ | | |

When digital component output is desired in RGB mode, the **RGBH** register can be programmed to increase the 0-100% values from standard CCIR 601 levels to full range levels. The gain variations are shown in Table 6.

Table 6: RGB Output Range

| Signal | RGB normal gain (RGBH=0) | | RGB high gain (RGBH=1) | |
|------------|--------------------------|-------------|------------------------|-------------|
| | Cy | RGB (U,V=0) | Cy | RGB (U,V=0) |
| Peak White | 235 | 235 | 255 | 255 |
| Black | 16 | 16 | 0 | 0 |

For CCIR 601 digital video input (**INPSL[1:0]** = 1), register **UNIT** must be set to 1 to produce unit gain.

1.3.2. Horizontal Luma Frequency Shaping

The luma path contains many programmable filters for different purposes. The combination of these filters will give different frequency characteristics.

The over sampled video data from the ADC pass through a decimation filter. The decimation filter has user programmable bandwidth. Three registers are used to control the decimation filter characteristics and each is designed for certain purposes. The **HYBWI**, when set to "1", provides extra bandwidth for very high quality video source. The **HYBWR**, when set to "1", reduces the bandwidth so high frequency noise can be eliminated. The 3-bit register **HYLPF[2:0]** provides the necessary bandwidth reduction for horizontal scaling. When all three registers are programmed to '0', the decimation filter has the bandwidth of the normal video. The KS0127B provides the option of bypassing the decimation filter. This option should be used only when the input video is band limited and with low high frequency noise.

For composite video input, the notch filter can be enabled (**CTRAP** set to "1") to extract the luminance. The notch filter has different center frequencies for different input video format. User selectable peaking function is included for edge enhancement. The notch filter should be bypassed for S-video and component video input, or if luma comb filter is enabled.

The luminance filter characteristics have been designed to be very similar for all combinations of 60/50 Hz video and CCIR 601/square pixel sampling rates. Figure 13 and Figure 14 show the output characteristics of the luminance path with different filter combinations for the supported input standards and output pixel rates.

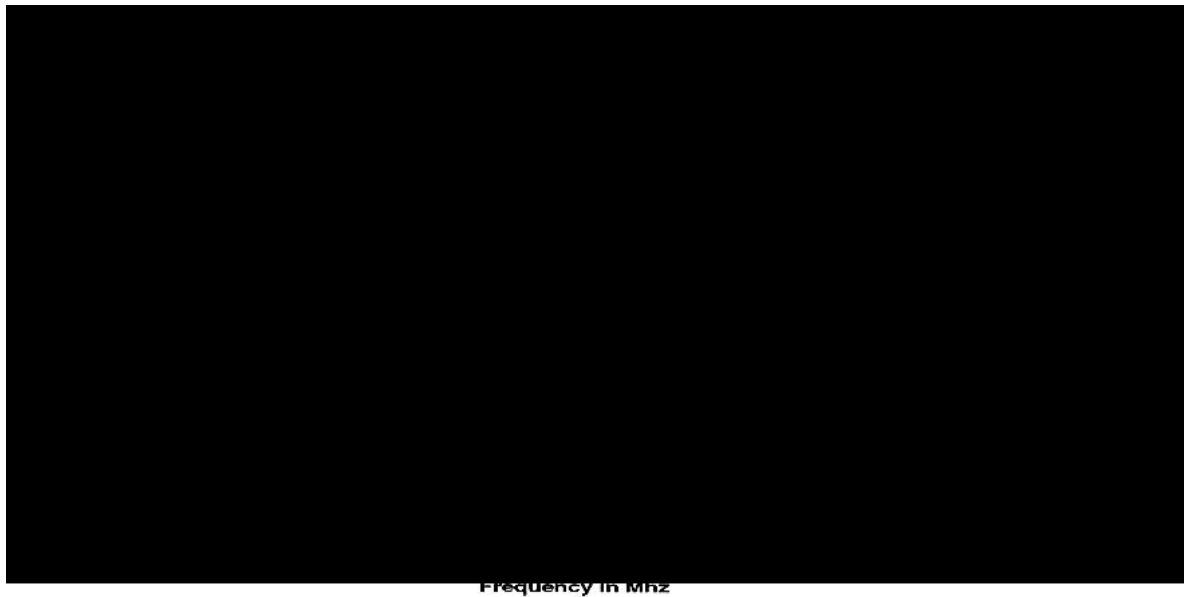


Figure 13. Medium to High Frequency Luma Filter Characteristics (CTRAP=0)

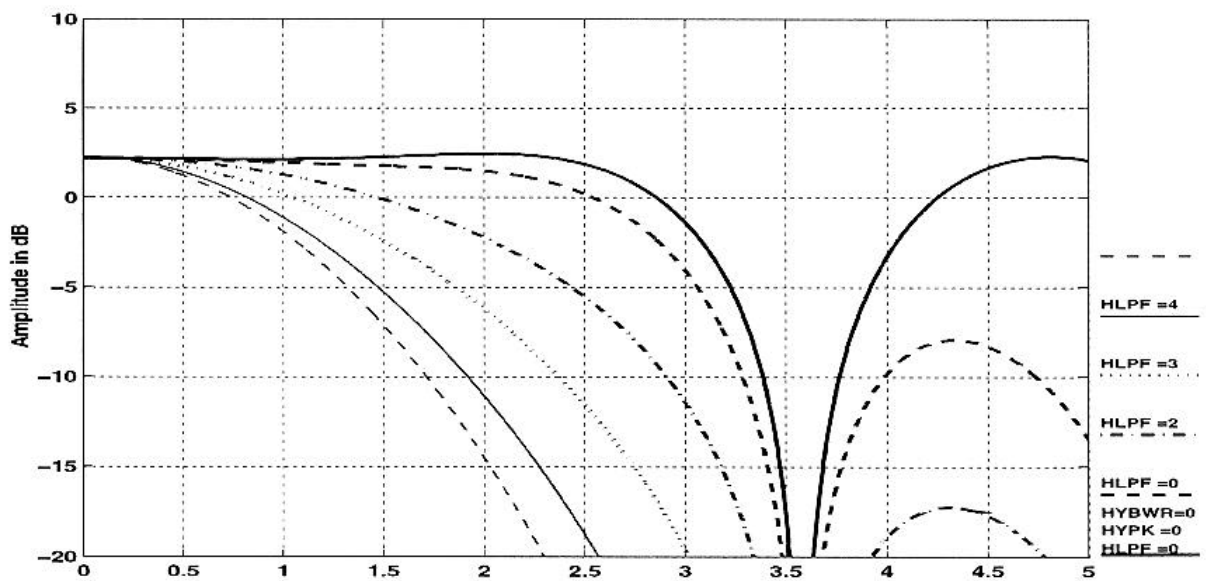


Figure 14. Medium to Low Frequency Luma Filter Characteristics (NTSC, CTRAP=1)

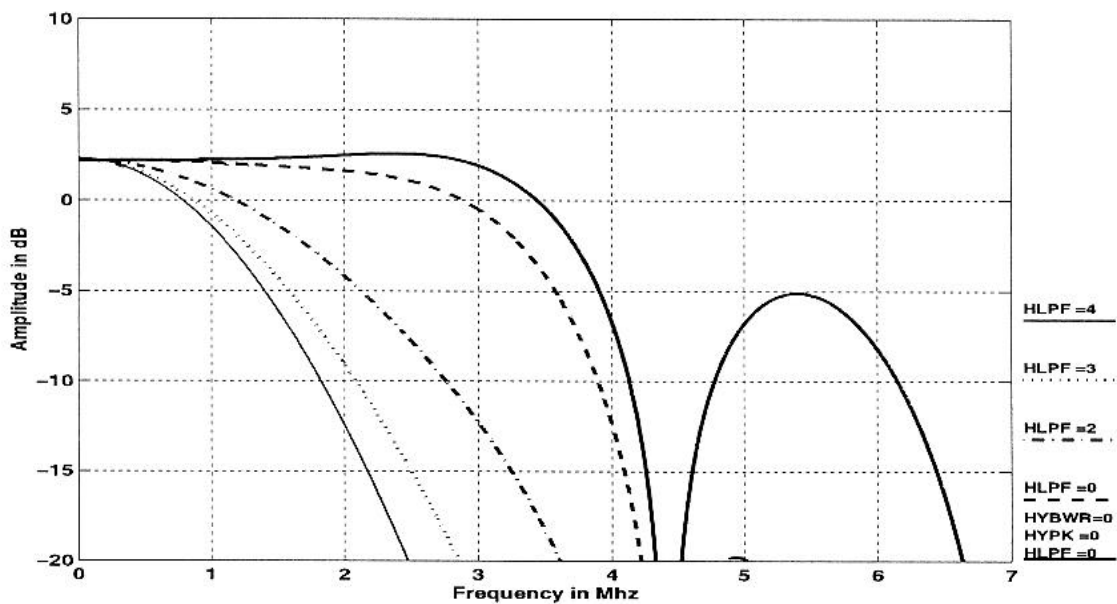


Figure 15. Medium to Low Frequency Luma Filter Characteristic (PAL, CTRAP=1)

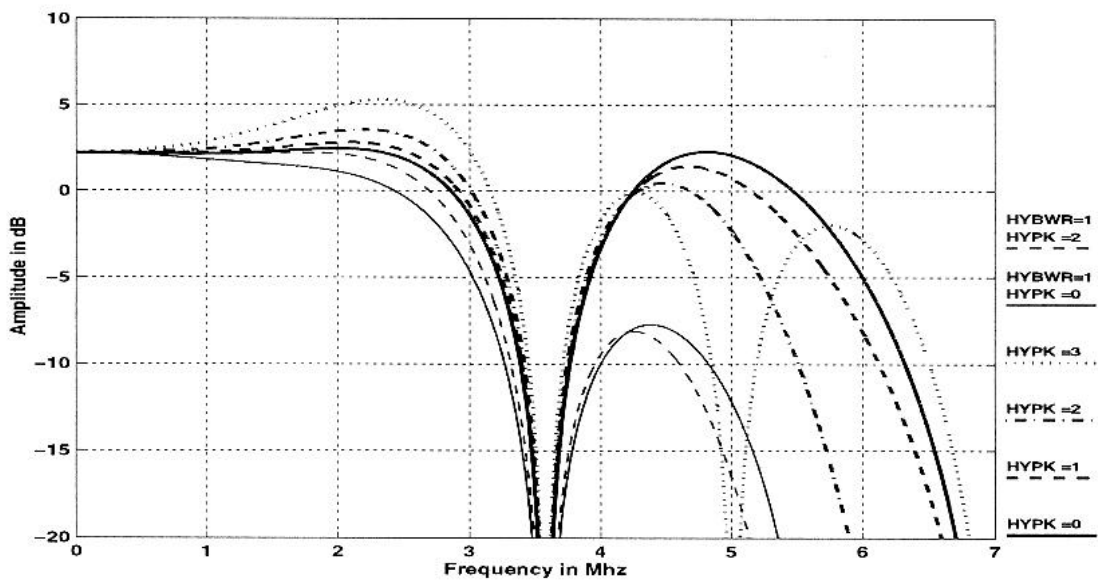


Figure 16. Luma Filter Characteristic with Peaking On (NTSC, CTRAP=1)

1.4. HORIZONTAL CHROMA PROCESSING

A simplified block diagram for the horizontal chroma processing unit is shown in Figure 17.

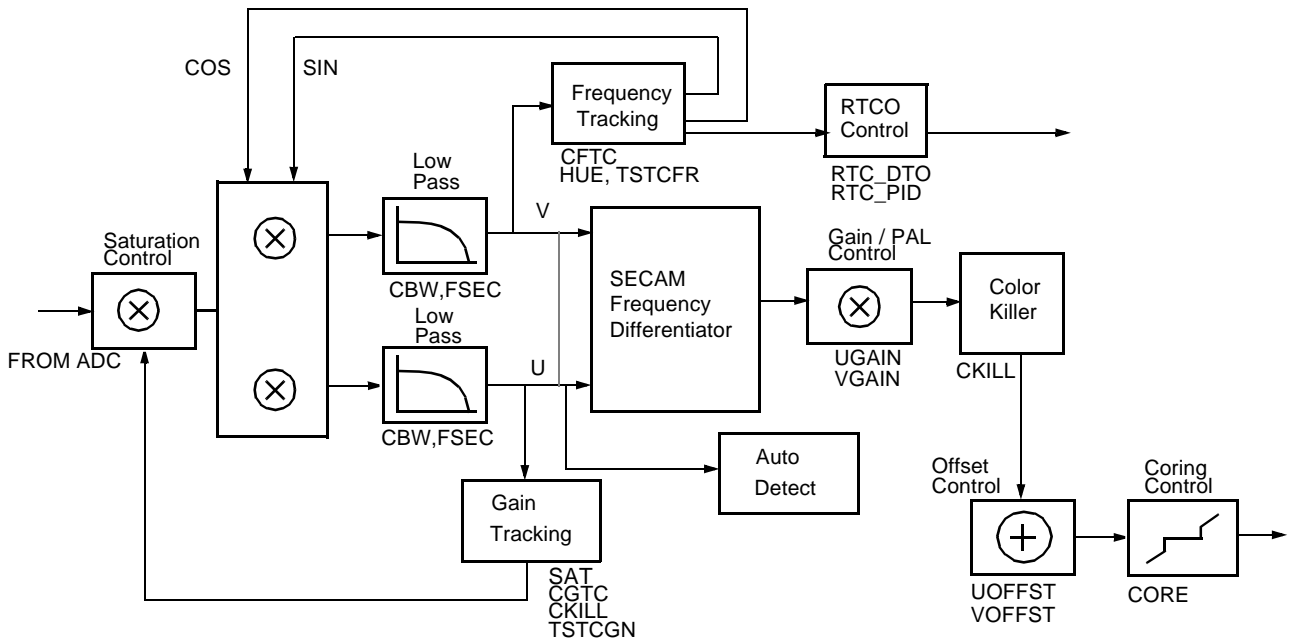


Figure 17. Horizontal Chroma Processing Unit

The KS0127B supports chroma input in NTSC, PAL, SECAM and component formats. The color standard is automatically detected and the various chroma processing blocks are enabled as required for the given chroma standard. Details of the various chroma processing blocks follow.

1.4.1. IF Compensation

For improved chroma demodulation when the input video is from a mis-tuned IF source, an IF compensation filter is included that has variable gain for the upper chroma side band. This is controlled by the **CIFCMP**[1:0] bits at location **CDEM**. The frequency response is shown in Figure 18. For convenience, all plots are normalized to the NTSC modulation frequency.

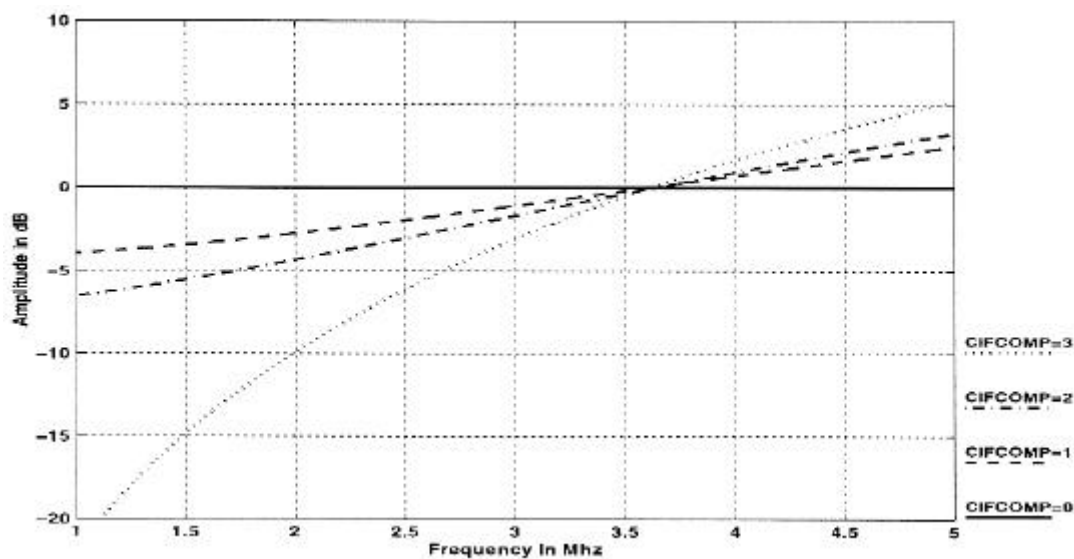


Figure 18. Chroma IF Compensation Frequency Response

1.4.2. Demodulation Gain

The demodulation gain block is controlled by feedback from the gain tracking block. For NTSC and PAL type inputs, the gain constant is derived from a programmable reference compared against the U component of the input video. This reference is controlled by the **SAT** register. The default value '0' is the correct gain (saturation for nominal output). For SECAM type input, the feedback is calculated such that proper frequency demodulation is obtained. When external calibration is desired, the gain feed back loop can be 'opened' by setting **TSTCGN**=1. The **SAT** then controls bits 8 through 1 of a 10 bit multiplier.

For standard auto tracking applications, it is recommended that the **SAT** register be used as an end user saturation control. This register is 2's complement.

1.4.3. Demodulation Low Pass Filter

The demodulation circuit also contains a programmable low pass filter and a coring function for noise reduction. The chroma low pass filter frequency response for the demodulation circuit for the various video standards are shown in Figure 19

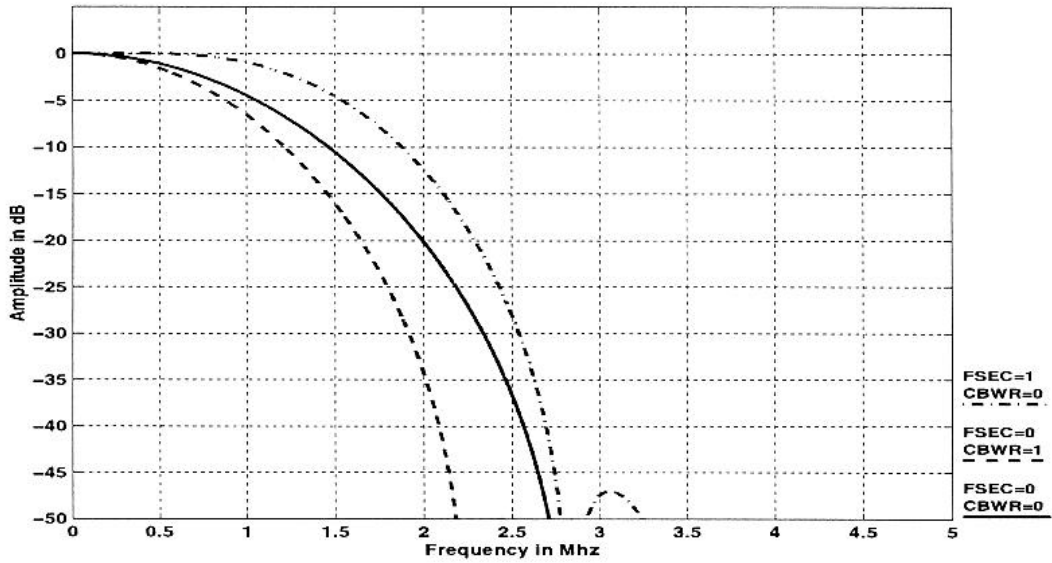


Figure 19. Chroma Low Pass Filter Frequency Response

1.4.4. SECAM Demodulation

SECAM processing includes a frequency differentiator, a Cloche and a de-emphasis filter. Frequency response for the filters are shown in Figure 20 and Figure 21.

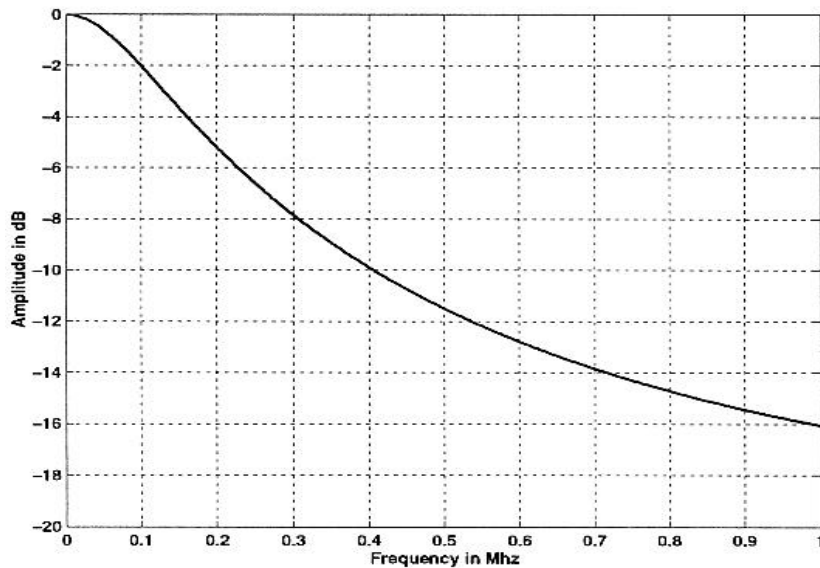


Figure 20. Cloche Filter Frequency Characteristic

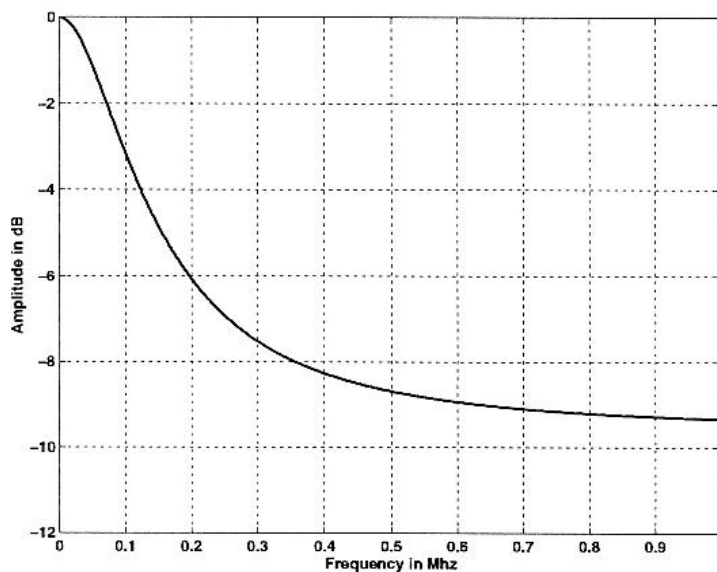


Figure 21. De-emphasis Filter Frequency Response

1.4.5. Additional Chroma Functions

KS0127B has many built in auto detection circuits. These allow KS0127B to track any type of video standard input automatically.

For analog component video input, the demodulation function is not enabled. The low pass filter provides a group delay for Cb and Cr alignment. This enables the two components to be sampled by one ADC.

An RTCO serial output is provided that encodes the current chroma and pixel frequency of the decoder. This information can be used by an Encoder running off of the decoder clock to produce proper color output. The horizontal position of the serial signal is controlled by the **HS2** location. The phasing of the DTO and the Encoder can be reset using the **RTC.DTO** bit. For PAL mode, the PID polarity can be controlled with the **RTC.PID** bit.

1.5. COMB FILTER

Comb filters provide superior Y/C separation for composite NTSC and PAL than simple chroma trap filter. The KS0127B contains on-chip separate 2-line stored luma and chroma comb filters. An internal signal COMB controls for what lines the comb function is enabled. This signal is available through the PORTB pin. Combing is part of the vertical processing which also includes vertical scaling, which is discussed in Section 1.6. A block diagram for the vertical processing section is shown in Figure 22.

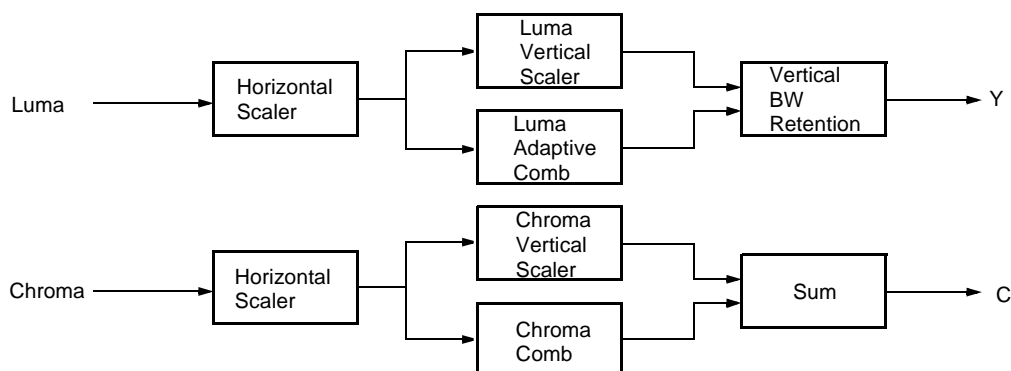


Figure 22. Vertical Processing

1.5.1. Luma Comb Filter

The luma comb filter reduces high frequency chroma leakage into the luminance path. The KS0127B uses 2-line stored luma data for combing. Filter coefficients for different video input standards are provided and can be selected automatically based on the video input. Filter coefficients may also be set manually.

An optional active comb is employed for NTSC video. Selection of luma comb coefficients is based on line-to-line chroma correlation.

Provision is made to disable luma comb for S-video, component, or digital video input. This is achieved by programming the luma comb control register **MNYCMB** to "1", and by choosing the value 3 or 4 for **YCMBCO[2:0]**. This will result either a 1-line or 2-line luma delay. Care must be exercised when disabling the luma comb so that luma line delay matches the chroma path line delay.

Special filtering is applied to ensure that high vertical bandwidth is retained for the luma path.

1.5.2. Chroma Comb Filter

The chroma comb filter provides further color separation from the composite video. Filter coefficients can be automatically selected based on the input video standard or manually set using **NMCCMB** and **CCMBCO[2:0]**.

1.6. SCALING

The KS0127B includes a high quality down scaler. The video images can be down scaled in both horizontal and vertical direction to an arbitrary size.

1.6.1. Horizontal Scaler

The horizontal scaler uses a 5-tap 32-phase interpolation filter for luma, and a 3-tap 8-phase interpolation filter for chroma. Scaled pixel data are stored in an on-chip FIFO so they can be sent out in a continuous stream.

Horizontal scaling ratio is programmed via the 15-bit register **HSCL**. The timing signal EHAV is used to indicate when scaled pixel data is available at the video output port. EHAV can be programmed so that it is active for every line regardless of vertical cropping and scaling. Or it can be programmed to be active only for valid video lines. For example, Figure 23 shows the timing for CIF output assuming HAV is programmed to be active for 720 pixels. The **HSCL** register is programmed with the value 4000 (hex). The trailing edge of EHAV is either aligned with the trailing edge of HAV if the total number of scaled pixels is even, or is one pixel clock earlier if the number is odd.

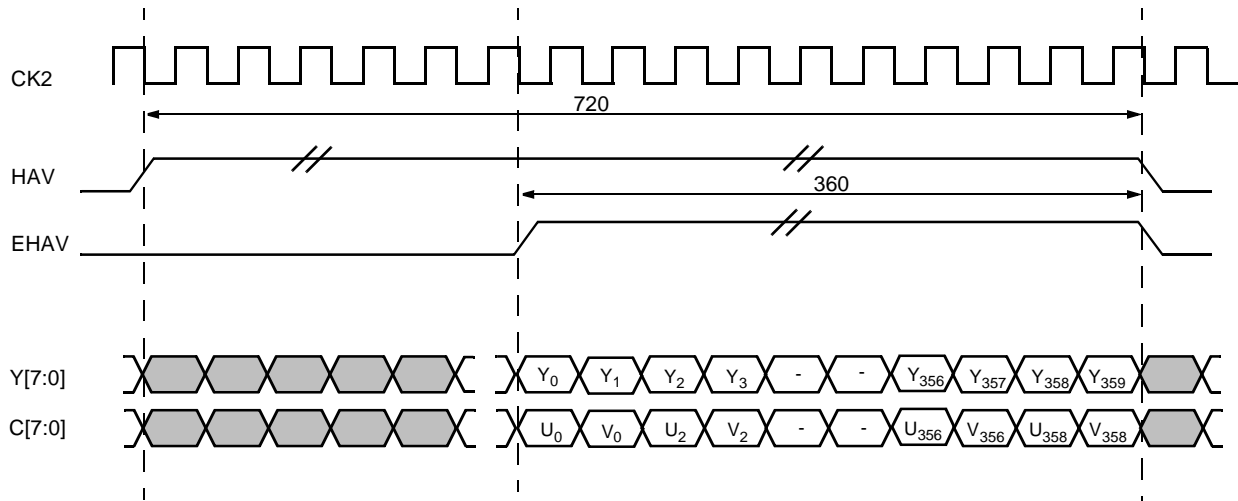


Figure 23. Horizontal Scaler Timing for CIF Output (CCIR 601 Pixel Rate)

Frequency response and group delay for the luma scaler are shown in Figure 24 and Figure 25, respectively. The luma interpolation filter is designed to achieve relatively flat frequency response and minimal group delay up to the normal video bandwidth. A flat full data path frequency response may be obtained with the help of the luma peaking control register **HYPK[1:0]**. The high quality filter ensures minimal artifacts for any scaling ratio.

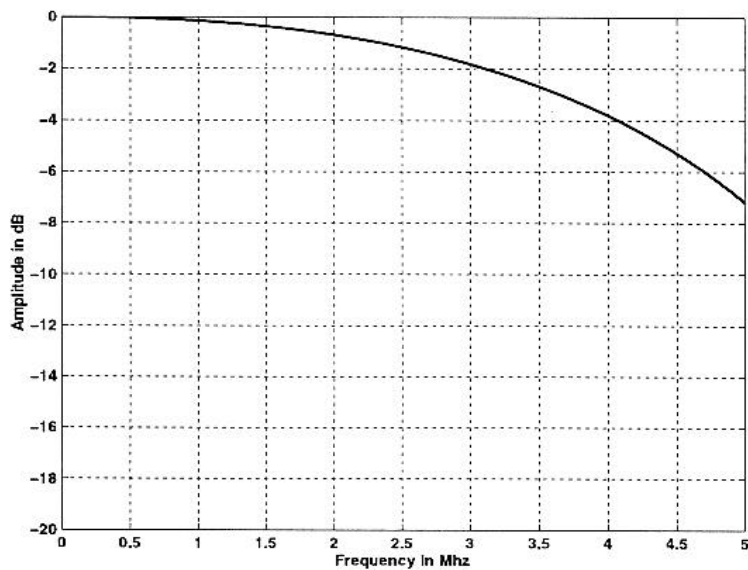


Figure 24. Horizontal Luma Scaler Interpolation Filter Frequency Response

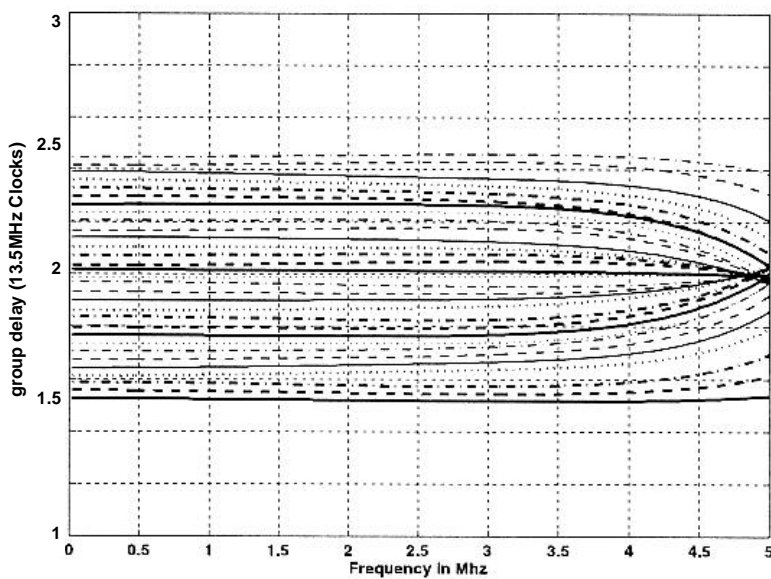


Figure 25. Horizontal Luma Scaler Interpolation Filter Group Delay

Because of the limited bandwidth of the chroma data, a simpler interpolation filter is used for the horizontal chroma scaler. The frequency response and group delay for this filter are shown in Figure 26 and Figure 27, respectively.

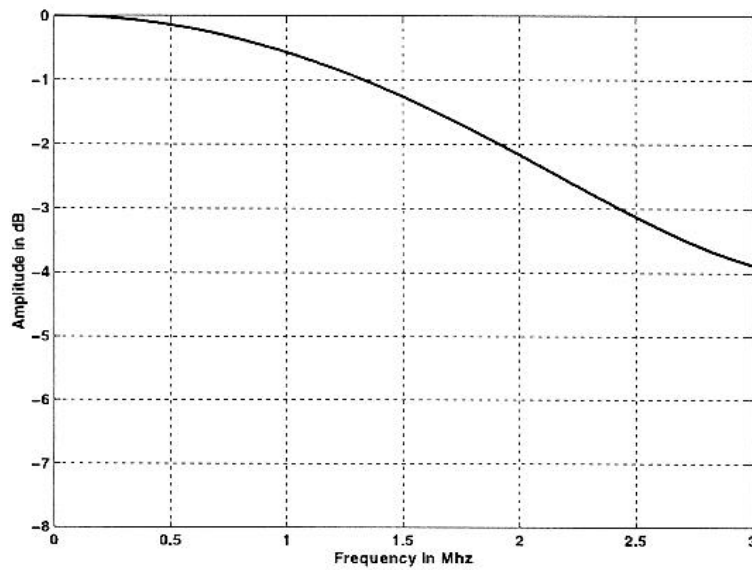


Figure 26. Horizontal Chroma Scaler Interpolation Filter Frequency Response

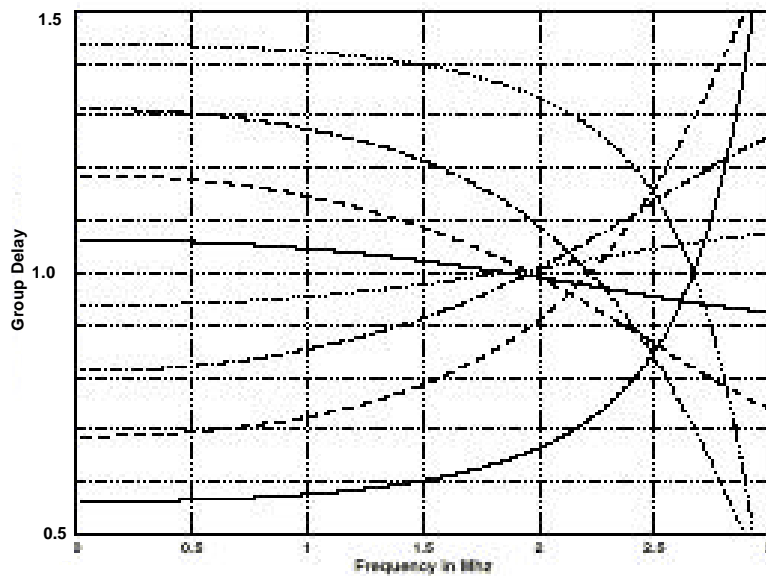


Figure 27. Horizontal Chroma Scaler Interpolation Filter Group Delay

1.6.2. Luma Vertical Scaler

Vertical luma scaling uses either a 3-tap or 5-tap 8-phase interpolation filter depending on the horizontal scaling

ratio.

Vertical scaling ratio is programmed via the 14-bit register **VSCL**. A valid scaled line is indicated by the timing signal EVAV being active. The EVAV can be programmed to be internally gated by the VAV signal so it can only be valid within the vertically cropped region.

Luma horizontal scaling can use either a 3-tap or a 5-tap interpolation filter depending on the horizontal scaling ration. If the scaled horizontal line has less than or equal to 384 pixels, the 5-tap luma interpolation filter can be turned on by programming the VRT2X bit to a "1". Otherwise, the VRT2X bit should be set to "0" and the 3-tap filter be used.

The **VYBW** bit provides additional vertical bandwidth control for vertical scaling. Typically, when the vertical scaling ratio is less than 1/2, this bit should be set to "1" to eliminate any aliasing effect.

Luma vertical scaler interpolation filter frequency response is shown in Figure 28.

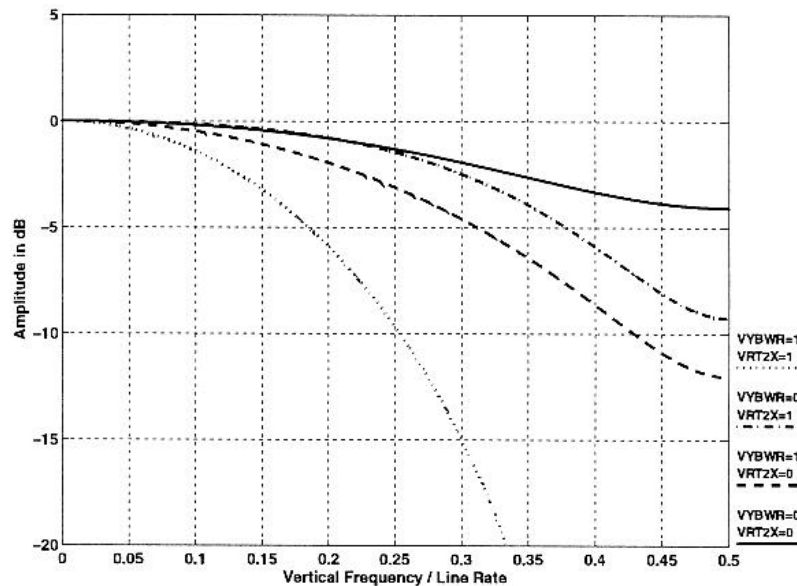


Figure 28. Luma Vertical Scaler Interpolation Filter Frequency Response

In vertical scaling, the start of signal VAV controls the phase of the vertical scaler interpolation filter. If **VAVB**, **VAVE**, **VAVOD0**, **VAVEV0**, and **VSCL** are programmed such that the vertical interpolation filter has the same phase and scaling ratio as that of a memory controller (most memory controller has simple line dropping vertical scaling), it is possible to interface the KS0127B to the memory controller without using EVAV.

1.6.3. Chroma Vertical Scaling

Chroma vertical scaling uses different algorithms depending on video input standard and horizontal scaling ratio. If horizontal scaling results in line with less than or equal to 384 pixels, and the **VRT2X** is set to a "1", a 5-tap interpolation filter will be used for all video inputs. Otherwise, for NTSC, a 3-tap interpolation filter will be used for NTSC input, and decimation (line dropping without filtering) will be used for PAL and SECAM. Filter characteristics for the 3-tap and 5-tap filters are shown in Figure 29.

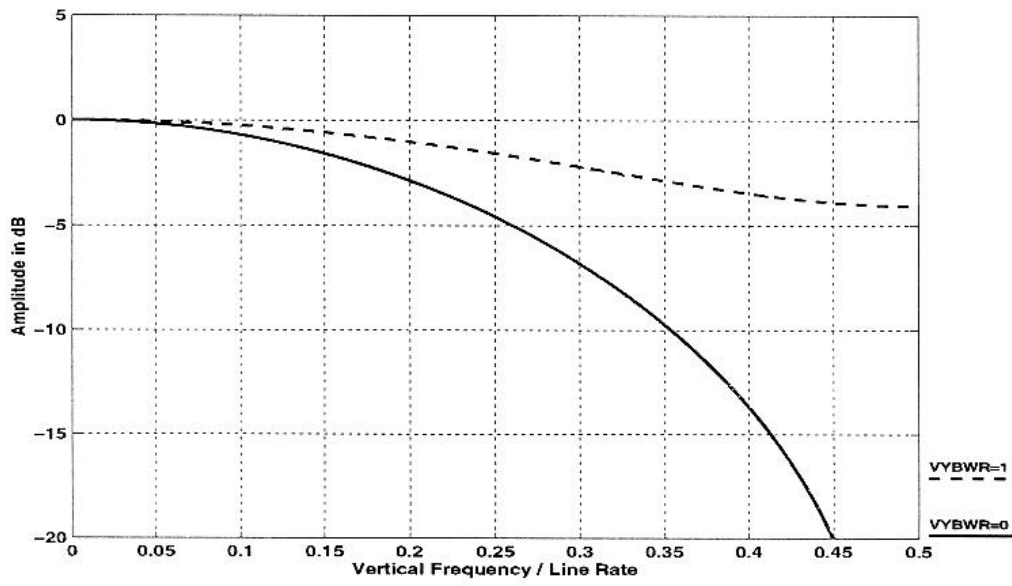


Figure 29. Chroma Vertical Scaler Interpolation Filter Frequency Response

1.7. VBI DATA PROCESSING

The KS0127B VBI data processing is very flexible in that it supports VBI data formats of:

- Closed Caption Line 21 Data Service (EIA-608)
- 525 line / 60Hz Teletext systems B,C,D (ITU-R BT.653-2)
- 625 line / 50Hz Teletext systems A,B,C,D (ITU-R BT.653-2)
- Copy Generation Management System (EIA/IS-702)
- Wide Screen Signalling (WSS ETS 300 294).

Note that the SMPTE data slicing is removed for the KS0127B and replaced with the WSS / CGMS processing. This data can be accessed from the part via four different methods:

- Enabling the 'Raw un-processed 27MHz' Y ADC samples to be output for the appropriate lines in place of the normal YUV data.
- Slicing the data (creating a clock and comparing the data to a threshold at the clock) and bursting this data out on Y output.
- Reading the sliced data from two internal registers via the IIC bus.
- Via 2 external pins that output the sliced VBI data and the time at which the slice is valid.

A simplified block diagram for the VBI section is shown in Figure 30.

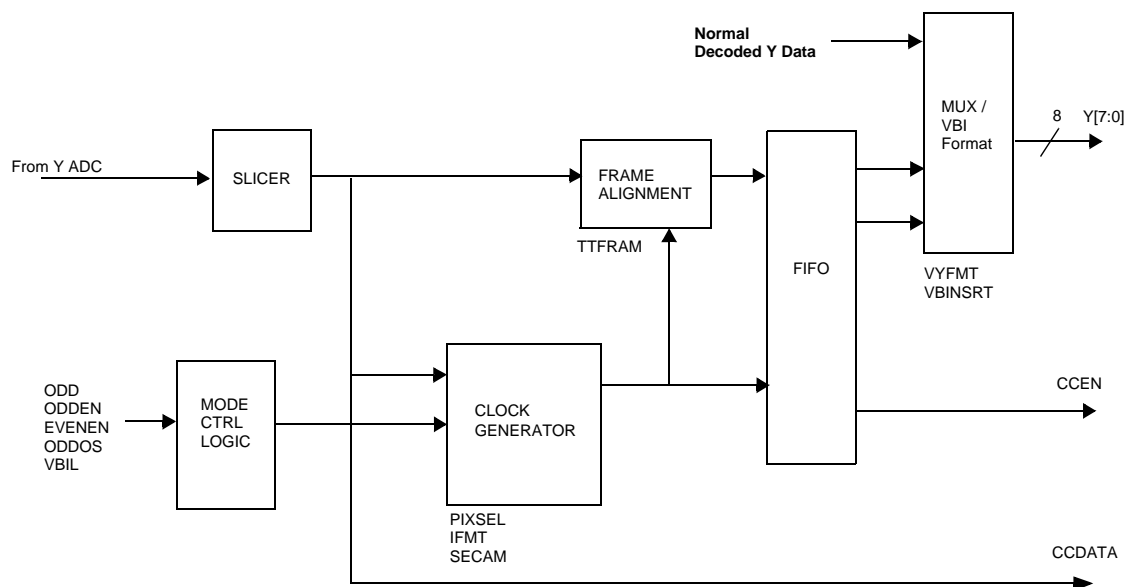


Figure 30. VBI Decoder Block Diagram

Table 7 lists all the video standards that the VBI data slicer supports. Some of these modes are auto detected based on the current video input standard,

Table 7: Video Standards Supported by VBI Decoder

| Mode | Value of Chip Detection Bits | | Required Values of Registers to enable Standard | | Characteristics of the Standard | |
|---|------------------------------|-------|---|--------|---------------------------------|------------------------|
| | Format | SECAM | VBIL0-15 | TT_SYS | Data Rate (MHz) | Number of Bits (bytes) |
| 60Hz Teletext system C (NTSC / Intercast) | 1 | 0 | 2 | 0 | 5.727272 | 272 (34) |
| 50Hz Teletext system B (PAL) | 0 | 0 | 2 | 0 | 6.9375 | 344 (43) |
| 50Hz Teletext system A (SECAM) | 0 | 1 | 2 | 0 | 6.203125 | 304 (38) |
| 60Hz Teletext system B | 0 | 1 | 2 | 1 | 5.727272 | 280 (35) |
| 50Hz Teletext system C | 0 | 1 | 2 | 2 | 5.734375 | 272 (34) |
| 50Hz Teletext system D | 0 | 1 | 2 | 3 | 5.6457875 | 280 (35) |
| 60Hz Teletext system D | 0 | 1 | 2 | 3 | 5.727272 | 280 (35) |
| Closed Caption NTSC 601 | N/A | N/A | 1 | N/A | 0.5035 | 16 (2) |
| CGMS (NTSC 60Hz) | 1 | N/A | 3 | N/A | 0.447443 | 20 (3) |
| WSS (PAL 50Hz) | 0 | N/A | 3 | N/A | 5.0000 | 84 |

Configuring the VBI processing consists of many different steps which are individually explained below.

1.7.1. Enabling the VBI Processor

The VBI processor can be enabled independently for the ODD or EVEN fields with the **ODDEN** and **EVENEN** bits. Some VBI data is only present on line in 1 of the 2 fields, These independent field enables allow control of the total VBI data output from the chip. These controls apply to all VBI Lines, Thus it is not possible to enable Closed caption line 21 for the Even field and line 19 Teletext for both the odd and even field.

1.7.2. Selecting the Type of Output Data

As previously mentioned, there are 4 different ways the VBI data can be extracted. Three of these are selected as shown in the table, the fourth method (CCEN and CCDAT pins) is always available if VBI processing is enabled.

Table 8: VBI Data Output Mode (VBILn != 0)

| VBCVBS | VBINSRT | Output Mode |
|--------|---------|---|
| 0 | 0 | The VBI data is available via the internal registers CCDAT1 and CCDAT2 . Only the last 2 extracted bytes are stored in these registers. Thus, this mode is only useful for extraction of Closed Caption data. |
| 0 | 1 | This mode enables output of the sliced VBI data. |
| 1 | 0 | This mode enables output of direct data from the ADC. |
| 1 | 1 | This mode is invalid. |

The KS0127B adds an additional output mode and flexibility to vary the modes from line to line. If **VBCVBS=0** and **VBINSRT=1** KS0127B will output sliced data on enabled lines. By setting **VBIMID** to 1, any line for which **VBIL=3** will output raw ADC data instead of WSS or CGMS. This mode allows a mixture of sliced and raw data. This can be used to output raw data from a teletext line and sliced data from a closed caption line.

1.7.3. Select Individual Lines Enabled for VBI Processing

The KS0127B allows programmable selection of processing for the various video lines. For example Teletext/Intercast data can be sliced for lines 14 - 17, and closed caption for line 21.

Each 2-bit register **VBIL0** through **VBIL15** defines how a specific VBI line is processed. As can be seen in Figure 36 for 60 Hz and Figure 37 for 50 Hz video, the following alignments exist:

Table 9: VBI Line(s) Selection

| VBIL number | Line Number That the VBIL Processing command applies to (Assuming ODDOS=1) | | | |
|-------------|--|--------------------------|-----------------------|----------------------------|
| | Odd Field 60 Hz | Even Field 60 Hz | Odd Field 50 Hz | Even Field 50Hz |
| VBIL0 | All Lines Except 10-24 | All Lines Except 273-287 | All lines Except 7-21 | All lines Except 320 - 334 |
| VBIL1 | 9&10 | 272&273 | 6&7 | 319&320 |
| VBIL2 | 11 | 274 | 8 | 321 |
| VBIL3 | 12 | 275 | 9 | 322 |
| VBIL4 | 13 | 276 | 10 | 323 |
| VBIL5 | 14 | 277 | 11 | 324 |
| VBIL6 | 15 | 278 | 12 | 325 |
| VBIL7 | 16 | 279 | 13 | 326 |
| VBIL8 | 17 | 280 | 14 | 327 |
| VBIL9 | 18 | 281 | 15 | 328 |
| VBIL10 | 19 | 282 | 16 | 329 |
| VBIL11 | 20 | 283 | 17 | 330 |
| VBIL12 | 21 | 284 | 18 | 331 |
| VBIL13 | 22 | 285 | 19 | 332 |
| VBIL14 | 23 | 286 | 20 | 333 |
| VBIL15 | 24&25 | 287&288 | 21&22 | 334&335 |

The **ODDOS[1:0]** bits allow offset between the odd and even fields. Thus VBIL9 can be lines 17,18 or 19 for ODD fields while VBIL9 is still line 281 for EVEN fields. This extra controls account for variations of VBI data locations from ODD and EVEN fields.

When Intercast or Teletext data is selected, an 8-bit user programmable register (**TTFRAM**) is provided for the framing byte. The frame alignment processor uses this information to properly locate the first data bit on each line

1.7.4. Raw CVBS Data Output Format

When raw ADC data is selected as output in place of the normal YUV or RGB data. The following rules apply:

- For 656 type 8 bit outputs, The ADC data outputs with successive data points in place of the Cb, Y, Cr, Y data stream.
- For 16 bit or 24 bit outputs, The ADC data is output on the Y[7:0] and C[7:0] output pins. At any CK2 clock 2 bytes of ADC data are output. The Y[7:0] bus represents data N while C[7:0] is data N+1.
- ADC data is only output during the region that HAV is active.
- All ADC outputs are limited to the range 1-254, thus a 0 or 255 value will not be output.

For the line selected mode described above using **VBCVBS** and **VBIL**, data is from the luma ADC only. If C ADC data or the entire video line is required, configure **OFMT** bits.

1.7.5. Sliced Data Output Formats

While sliced data is available for many of the output formats, the target application is 656 output format. The description of data format is limited to this mode. The KS0127B allows this data to be output during active video.

Figure 31 shows the timing diagram for **VYFMT[1:0]=3**.

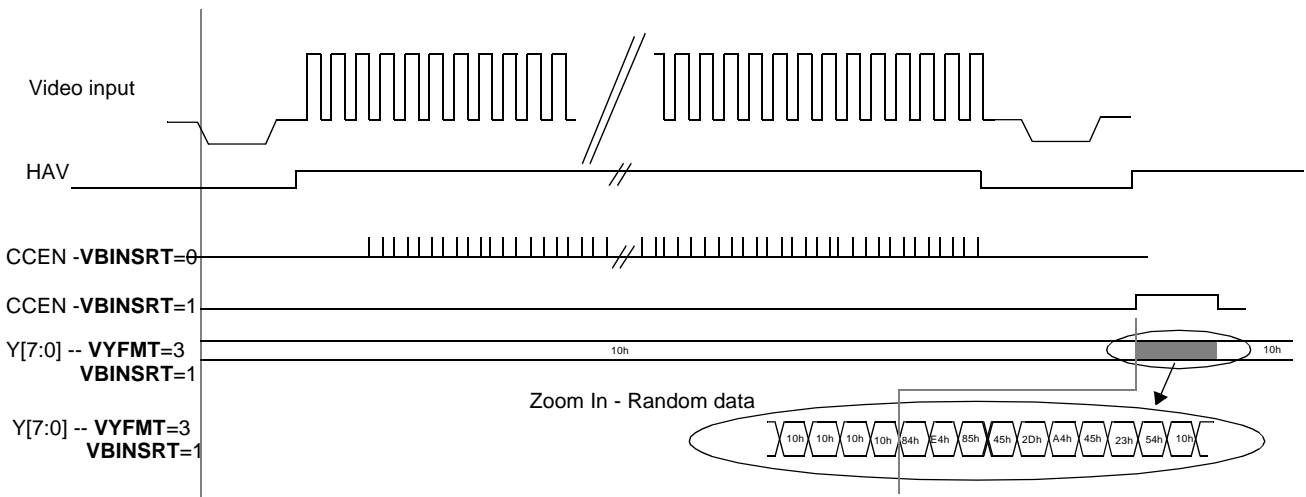


Figure 31. VBI Insertion Timing for VYFMT[1:0]=3

Digitized CVBS data can also be output on the video output port (except for output format 1, 5 and 7). CVBS is always digitized at the CK clock rate. CVBS data is available when HAV is active. Raw CVBS data is output in a

similar fashion as decoded video. For 8-bit output format, data is output at CK rate using the same 8-bit port as the decoded video. For 16-bit and 24-bit output format, data is output at CK2 rate using Y and C ports. The sequence of data output is CVBS_{2n} on Y, and CVBS_{2n+1} on C (note that EXV port is not used in 24-bit format for outputting raw CVBS data).

For Closed Caption data, two read-only registers, **CCDAT1** and **CCDAT2**, are provided so the Closed Caption data can be read via the host interface. The **VBIFLG** bit can be polled to see if data captured in the two registers can be safely read.

1.8. COLOR SPACE CONVERTER

The color space converter processes the video data as YCbCr 4:4:4 when converting to RGB. A programmable limiter (**YCRANG**) can be imposed on the Y/C data to limit the ranges. One can choose to limit the Y/C to 1 - 254, or Y to 16 - 235 and C to 16 - 240.

When selected, YCbCr 4:4:4 is converted to 24 bit RGB according to the following equations:

$$\begin{aligned} R &= C_Y + 1.375C_R \\ G &= C_Y - 0.703C_R - 0.328C_B \\ B &= C_Y + 1.734C_B \end{aligned}$$

For 16-bit RGB output, truncation with dithering is used to convert the data from 24 bit to 16 bit.

1.9. GAMMA CORRECTION

The KS0127B programmable gamma tables allows the customer to apply many different type of corrections. These corrections can be a standard 2.2 factor for NTSC or 2.8 for PAL. These factors can be applied in the RGB or YUV domains.

A basic standard gamma equation of

$$R = R'^{2.2}$$

when applied to the R, G, or B signals, generates the response shown as the upper curve below. It is the inverse of the monitor response and thus compensates to produce a linear response.

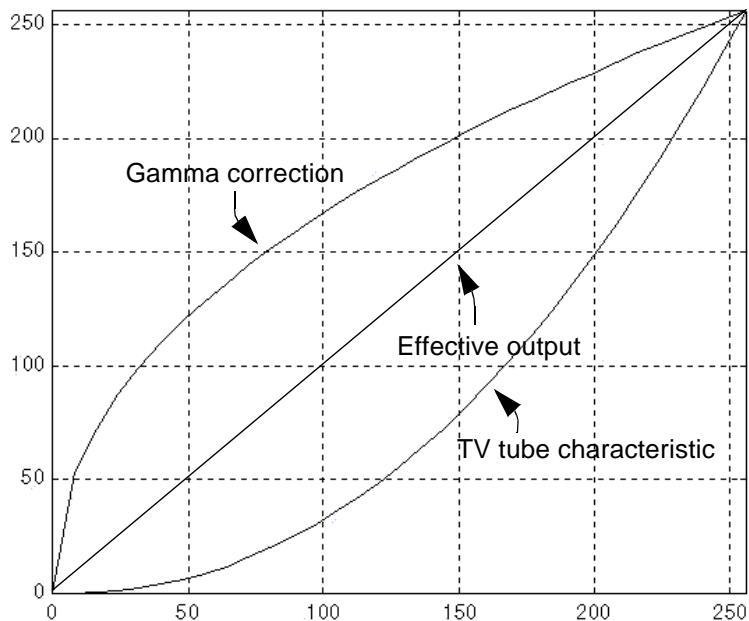


Figure 32. RGB Gamma Correction

1.9.1. Programming the KS0127B

The previous response is easily programmed into the KS0127B loading the 0, 8, 16, 24 etc. values into the GAMMA0,1,2,3 locations. Thus every 8th value is stored. The KS0127B will use linear interpolation to generate the values between every 8th points. This is shown in the following figure.

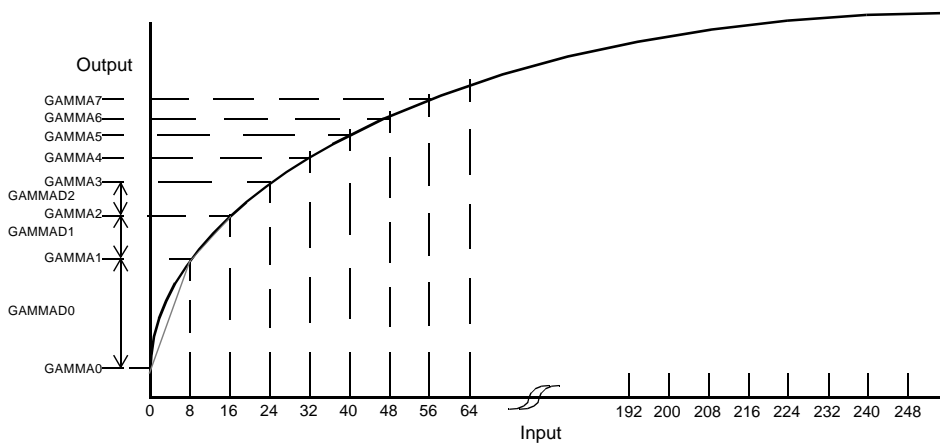


Figure 33. Gamma LUT Programming

For ease of design, the difference between adjacent points must also be loaded. The complete data values for the previous gamma factor of 1/2.2 is shown in the table below.

Table 10: RGB Gamma LUT Values

| Offset | GAMMA program at index Offset+40h | GAMMAD program at index Offset+60h |
|--------|--------------------------------------|---------------------------------------|
| 0 | 0 | 53 |
| 1 | 53 | 20 |
| 2 | 73 | 14 |
| 3 | 87 | 12 |
| 4 | 99 | 11 |
| 5 | 110 | 10 |
| 6 | 120 | 8 |
| 7 | 128 | 8 |
| 8 | 136 | 8 |
| 9 | 144 | 7 |
| A | 151 | 7 |
| B | 158 | 6 |
| C | 164 | 6 |
| D | 170 | 6 |
| E | 176 | 5 |
| F | 181 | 6 |
| 10 | 187 | 5 |
| 11 | 192 | 5 |
| 12 | 197 | 5 |
| 13 | 202 | 5 |
| 14 | 207 | 4 |
| 15 | 211 | 5 |
| 16 | 216 | 4 |
| 17 | 220 | 5 |
| 18 | 225 | 4 |
| 19 | 229 | 4 |
| 1A | 233 | 4 |
| 1B | 237 | 4 |
| 1C | 241 | 4 |
| 1D | 245 | 4 |
| 1E | 249 | 3 |
| 1F | 252 | 4 |

The flexibility of this architecture is shown in the following example. Here it is assumed that the KS0127B is operating in a YUV output mode but some form of Gamma correction is required. By converting the RGB gamma correction function back to the YUV color space, the following function can be applied to the U and V signals for improved color performance. This flexibility can be extended in software to produce many type of customer defined transfer functions.

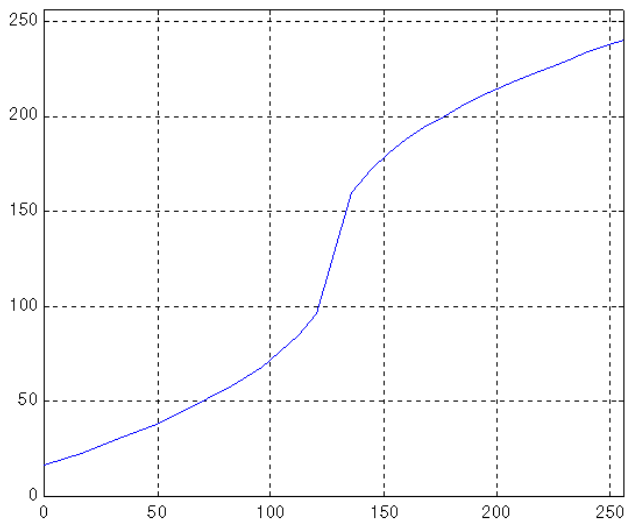


Figure 34. Gamma Correction for Cb and Cr

1.10. DIGITAL VIDEO OUTPUT

The KS0127B can output digital video data in various formats, which are tabulated in Table 11. All 8-bit output

Table 11: Digital Video Output Format

| Clock | CK2 | | | | | | | | | | CK | | | |
|-------|-------------|-----|-------------|-----|-----|-----|-------------|---------|---------|---------|-------------|----|-----|----|
| | 0 | | 1 | | | | 4 | 5 | 6 | 7 | 2, 3 | | | |
| OFMT | YCbCr 4:2:2 | | YCbCr 4:1:1 | | | | YCbCr 4:4:4 | RGB 565 | RGB 888 | RGB 888 | YCbCr 4:2:2 | | | |
| Pin | 2N | +1 | 4N | +1 | +2 | +3 | N | N | N | N | 4N | +1 | +2 | +3 |
| C0 | Cb0 | Cr0 | | | | | Cb0 | B0 | B0 | B3 | | | | |
| C1 | Cb1 | Cr1 | | | | | Cb1 | B1 | B1 | B4 | | | | |
| C2 | Cb2 | Cr2 | | | | | Cb2 | B2 | B2 | B5 | | | | |
| C3 | Cb3 | Cr3 | | | | | Cb3 | B3 | B3 | B6 | | | | |
| C4 | Cb4 | Cr4 | Cr6 | Cr4 | Cr2 | Cr0 | Cb4 | B4 | B4 | B7 | | | | |
| C5 | Cb5 | Cr5 | Cr7 | Cr5 | Cr3 | Cr1 | Cb5 | G0 | B5 | G2 | | | | |
| C6 | Cb6 | Cr6 | Cb6 | Cb4 | Cb2 | Cb0 | Cb6 | G1 | B6 | G3 | | | | |
| C7 | Cb7 | Cr7 | Cb7 | Cb5 | Cb3 | Cb1 | Cb7 | G2 | B7 | G4 | | | | |
| Y0 | Y0 | Y0 | Y0 | Y0 | Y0 | Y0 | Y0 | G3 | G0 | G5 | Cb0 | Y0 | Cr0 | Y0 |
| Y1 | Y1 | Y1 | Y1 | Y1 | Y1 | Y1 | Y1 | G4 | G1 | G6 | Cb1 | Y1 | Cr1 | Y1 |
| Y2 | Y2 | Y2 | Y2 | Y2 | Y2 | Y2 | Y2 | G5 | G2 | G7 | Cb2 | Y2 | Cr2 | Y2 |
| Y3 | Y3 | Y3 | Y3 | Y3 | Y3 | Y3 | Y3 | R0 | G3 | R3 | Cb3 | Y3 | Cr3 | Y3 |
| Y4 | Y4 | Y4 | Y4 | Y4 | Y4 | Y4 | Y4 | R1 | G4 | R4 | Cb4 | Y4 | Cr4 | Y4 |
| Y5 | Y5 | Y5 | Y5 | Y5 | Y5 | Y5 | Y5 | R2 | G5 | R5 | Cb5 | Y5 | Cr5 | Y5 |
| Y6 | Y6 | Y6 | Y6 | Y6 | Y6 | Y6 | Y6 | R3 | G6 | R6 | Cb6 | Y6 | Cr6 | Y6 |
| Y7 | Y7 | Y7 | Y7 | Y7 | Y7 | Y7 | Y7 | R4 | G7 | R7 | Cb7 | Y7 | Cr7 | Y7 |
| EXV0 | | | | | | | Cr0 | | R0 | B0 | | | | |
| EXV1 | | | | | | | Cr1 | | R1 | B1 | | | | |
| EXV2 | | | | | | | Cr2 | | R2 | B2 | | | | |
| EXV3 | | | | | | | Cr3 | | R3 | G0 | | | | |
| EXV4 | | | | | | | Cr4 | | R4 | G1 | | | | |
| EXV5 | | | | | | | Cr5 | | R5 | R0 | | | | |
| EXV6 | | | | | | | Cr6 | | R6 | R1 | | | | |
| EXV7 | | | | | | | Cr7 | | R7 | R2 | | | | |

formats use CK as pixel clock; the other formats use CK2 as pixel clock. The first pixel is always aligned to the leading edge of the HAV signal.

1.10.1. Validation Code Insertion

KS0127B inserts validation codes during inactive video (HAV is inactive), and invalid video (HAV is active but EHAV is inactive) to assist in recognition of scaled data and VBI data. Table 12 lists the available codes, when they are inserted, and related programming registers.

Table 12: Invalid and Unused Code Insertion

| Code | Description |
|--------|---|
| INVALY | This user programmed code is inserted in the Y or G output stream in scaling operation when HAV is active while EHAV is inactive. Insertion of this code is independent of the output format. Related register is INVALY . |
| INVALU | This user programmed code is inserted in the U or B output stream in scaling operation when HAV is active while EHAV is inactive. Insertion of this code is independent of the output format. Related register is INVALU . |
| INVALV | This user programmed code is inserted in the V or R output stream in scaling operation when HAV is active while EHAV is inactive. Insertion of this code is independent of the output format. Related register is INVALV . |
| UNUSEY | This user programmed code is inserted in the Y or G output stream when HAV is inactive and no other reference code is inserted. Insertion of this code is independent of the output format. Related register is UNUSEY . |
| UNUSEU | This user programmed code is inserted in the U or B output stream when HAV is inactive and no other reference code is inserted. Insertion of this code is independent of the output format. Related register is UNUSEU . |
| UNUSEV | This user programmed code is inserted in the V or R output stream when HAV is inactive and no other reference code is inserted. Insertion of this code is independent of the output format. Related register is UNUSEV . |

An example timing diagram for some of the programmable modes is shown in Figure 35. In this diagram, The field rate is 60 Hz, A CCIR 601 sampling rate has been selected thus giving 720 active pixels. The horizontal scaling ratio has been selected for an output of 718 out of 720 pixels.

Legend

- Y₀ Luma Data with pixel number
- U₀ Chroma (Cb) Data with pixel number
- V₀ Chroma (Cr) Data with pixel number
- Y₁ Programmable INVALY data (index 0x32)
- U₁ Programmable INVALU data (index 0x33)
- V₁ Programmable INVALV data (index 0x34)
- Y_U Programmable UNUSEY data (index 0x35)
- U_U Programmable UNUSEU data (index 0x36)
- V_U Programmable UNUSEV data (index 0x37)

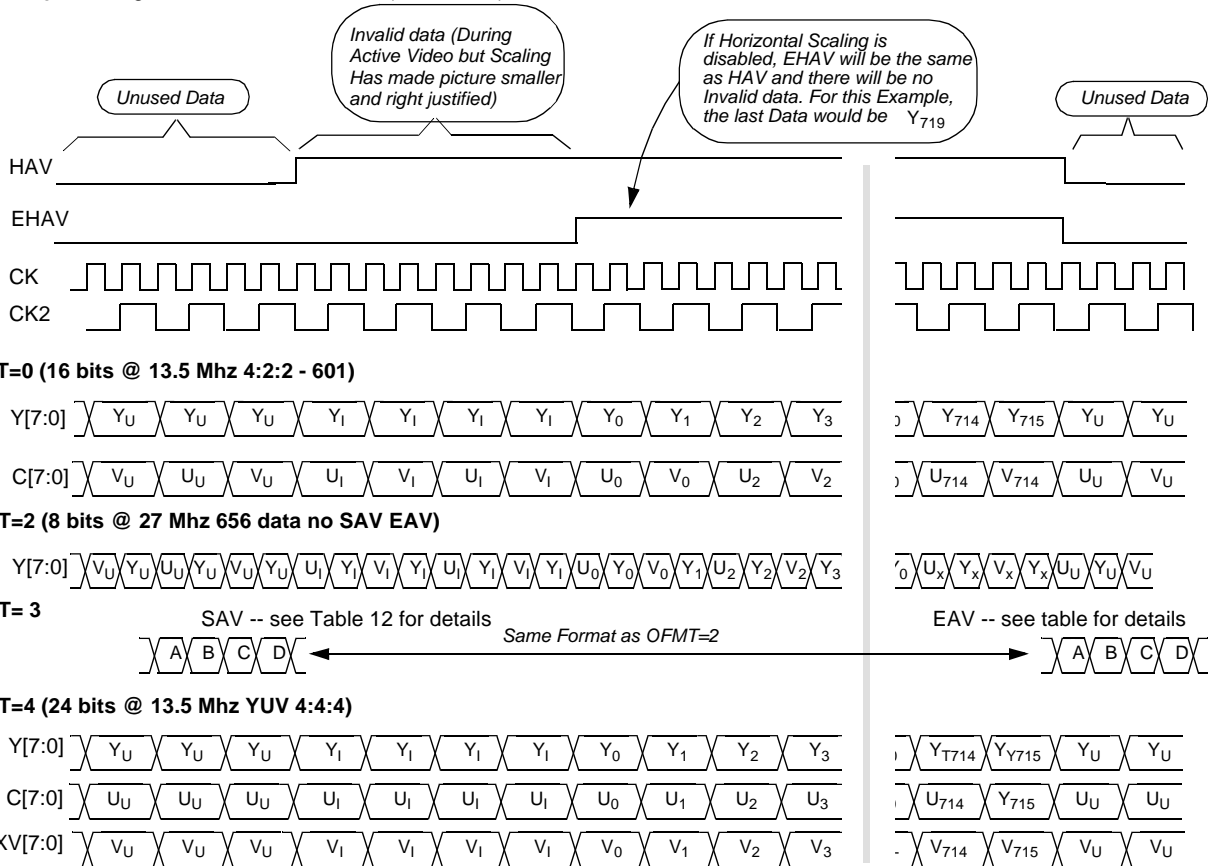


Figure 35. Horizontal Data Timing for Various Output Modes

1.10.2. 656 Op Codes

The KS0127B supports timing synchronization through embedded (656) timing reference codes in the output video data stream. This mode is available for output format 3 (OFMT[3:0] = 3). The 656 Op Codes follow the CCIR 656 standard. An optional set of 656 Op Codes can be enabled to identify VBI data using the **TASKB** bit.

The (A,B,C,D) inserted codes for 656 output modes are explained below. Locations in the data stream are shown in Figure 35. The D' data is substituted for the standard codes shown in column D if **TASKB** bit is set and the current line is processing VBI data (sliced or raw ADC data format).

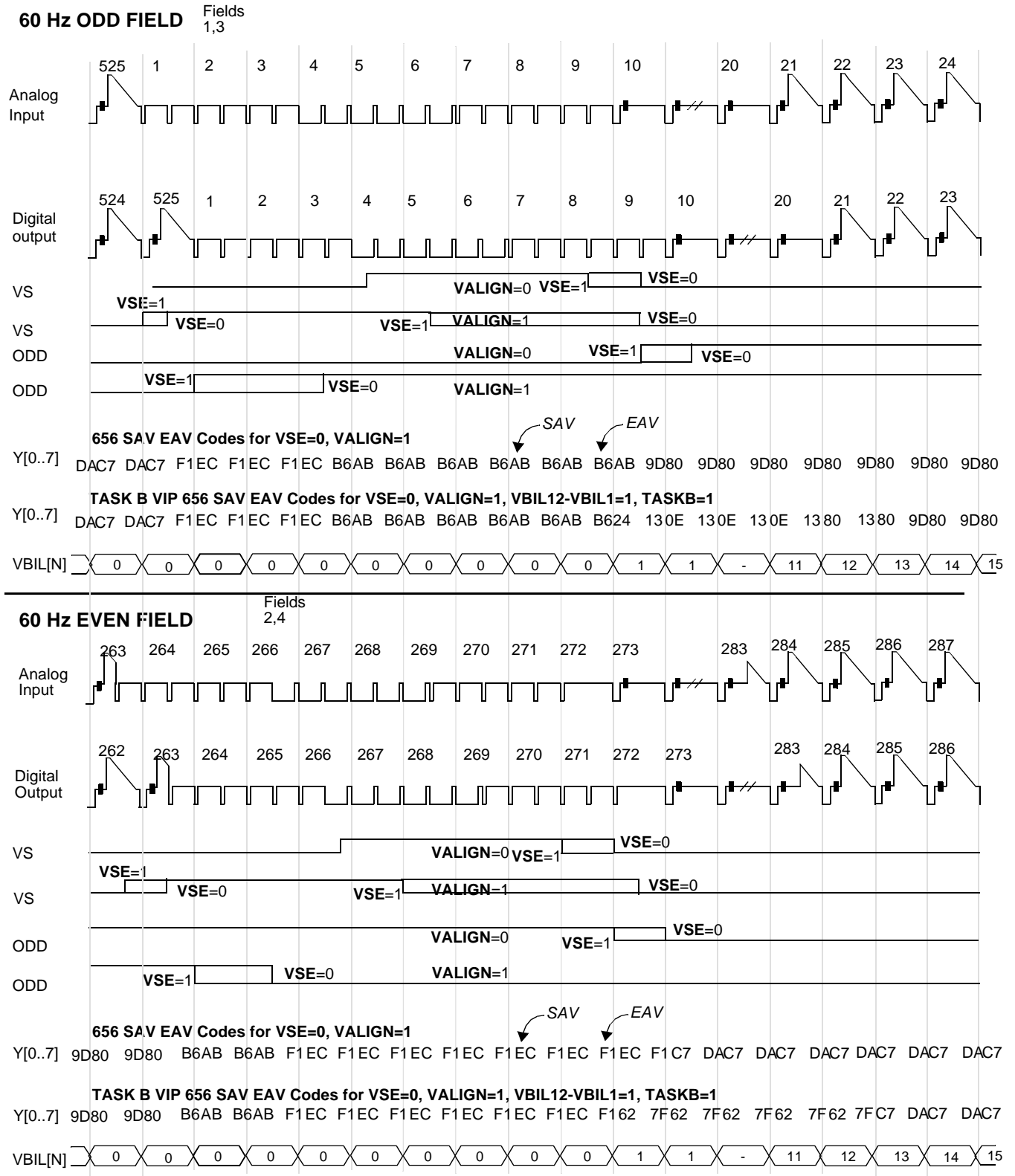


Figure 36. Vertical Timing for 60 Hz Video

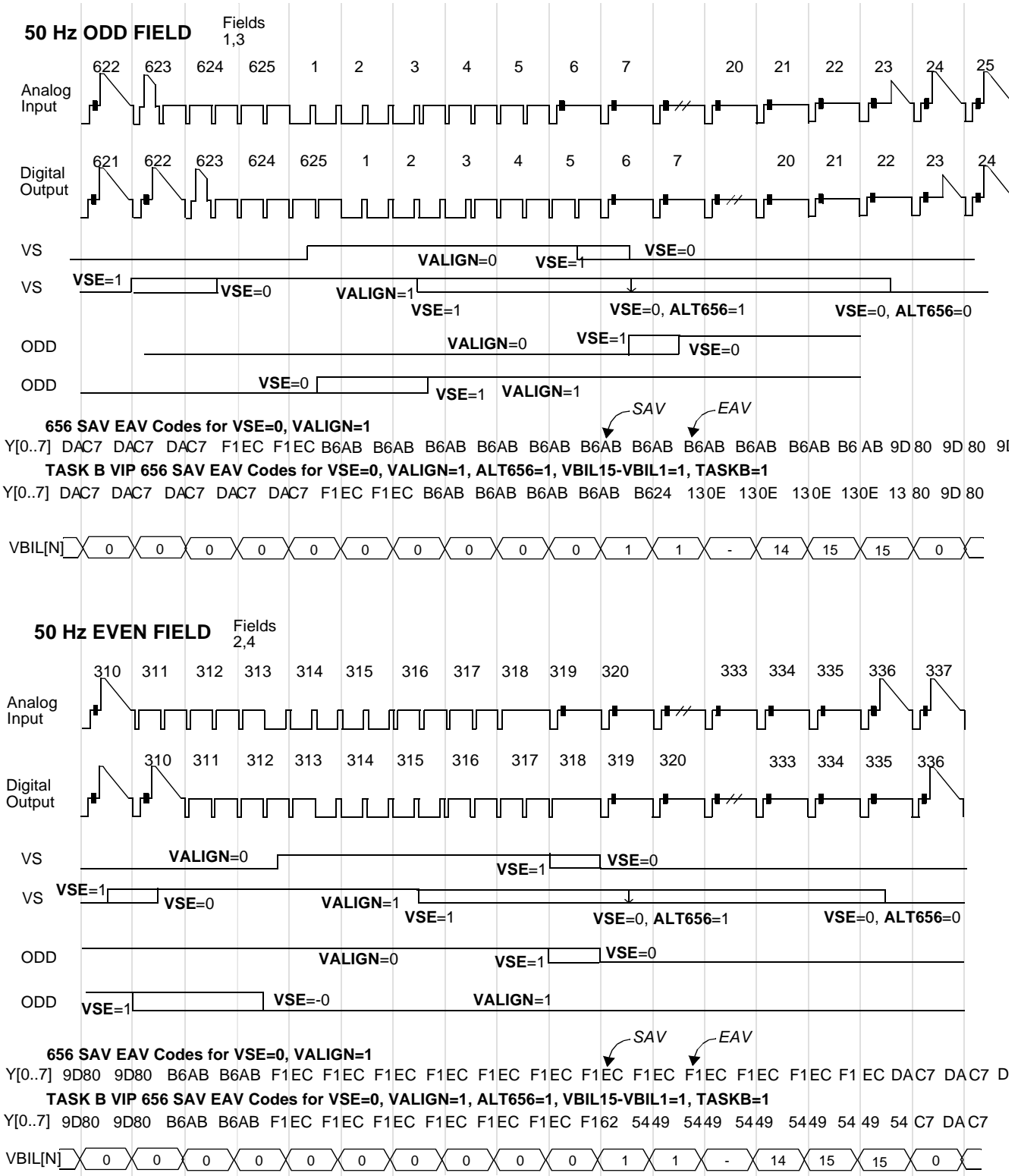


Figure 37. Vertical Timing For 50 Hz Video

Table 13: 656 and TASKB 656 Op Codes

| Condition | | | SAV / EAV Output Sequence -- Reference Output timing pictures | | | | | 656 FVH values | | |
|-----------|-----------------|--------------------|--|-----|-----|-----|-----|----------------|---|---|
| Field | Vertical | Horizontal | A | B | C | D | D' | F | V | H |
| Field 2 | Vertical Blank | End Active Video | FFh | 00h | 00h | F1h | 7Fh | 1 | 1 | 1 |
| Field 2 | Vertical Blank | Start Active Video | FFh | 00h | 00h | ECh | 62h | 1 | 1 | 0 |
| Field 2 | Vertical Active | End Active Video | FFh | 00h | 00h | DAh | 54h | 1 | 0 | 1 |
| Field 2 | Vertical Active | Start Active Video | FFh | 00h | 00h | C7h | 49h | 1 | 0 | 0 |
| Field 1 | Vertical Blank | End Active Video | FFh | 00h | 00h | B6h | 38h | 0 | 1 | 1 |
| Field 1 | Vertical Blank | Start Active Video | FFh | 00h | 00h | ABh | 24h | 0 | 1 | 0 |
| Field 1 | Vertical Active | End Active Video | FFh | 00h | 00h | 9Dh | 13h | 0 | 0 | 1 |
| Field 1 | Vertical Active | Start Active Video | FFh | 00h | 00h | 80h | 0Eh | 0 | 0 | 0 |

1.10.3. 656 Op Code Vertical Transitions

The vertical transition locations of the various 656 Op Codes are shown in Figure 36 and Figure 37. Note that for proper transition locations of the SAV and EAV Op Codes **VSE=0** and **VALIGN=1**.

1.11. HOST INTERFACE

The KS0127B supports the IIC serial interface for programming the chip registers.

1.11.1. IIC Interface

The two wire interface consists of the SCLK and SDAT signals. Data can be written to or read from the KS0127B. For both read and write, each byte is transferred MSB first, and the data bit is valid when the SCLK is high.

To write to the slave device, the host initiates a transfer cycle with a START signal. The START signal is HIGH to LOW transition on the SDAT while the SCLK is high. The host then sends a byte consisting of the 7-bit slave device ID and a 0 in the R/W bit. The arrangement for the slave device ID and the R/W bit is depicted in Figure 38. AEX1 and AEX0 are configuration pins used to configure the KS0127B to use one of the four addresses. Up to four KS0127Bs can be used in one system each with a unique address.

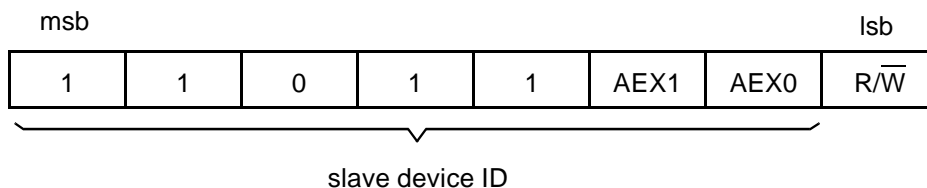


Figure 38. IIC Slave Device ID and R/W Byte

The second byte the host sends is the base register index. The host then sends the data. The KS0127B increments the index automatically after each byte of data is sent. Therefore, the host can write multiple bytes to the slave if they are in sequential order. The host completes the transfer cycle with a STOP signal which is a LOW to HIGH transition when the SCLK is high.

Each byte transfer consists of 9 clocks. When writing to the KS0127B, an acknowledge signal is asserted by the slave device during the 9th clock.

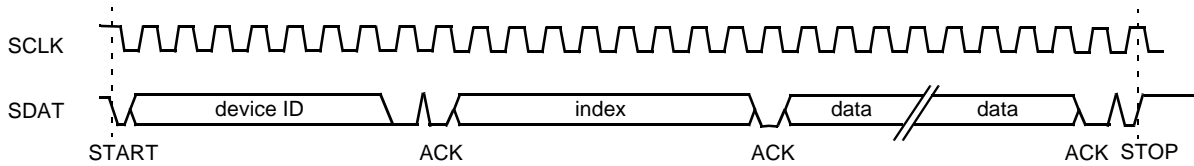


Figure 39. IIC Data Write

A read cycle takes two START-STOP phases. The first phase is a write to the index register. The second phase is the read from the data register.

The host initiates the first phase by sending the START signal. It then sends the slave device ID along with a 0 in the R/W position. The index is then sent followed by the STOP signal.

The second phase also starts with the START signal. It then sends the slave device ID but with a 1 in the R/W position to indicate data is to be read from the slave device. The host uses the SCLK to shift data out from the KS0127B. A typical second phase in a read transaction is depicted in Figure 40. Auto index increment is supported in Read mode.

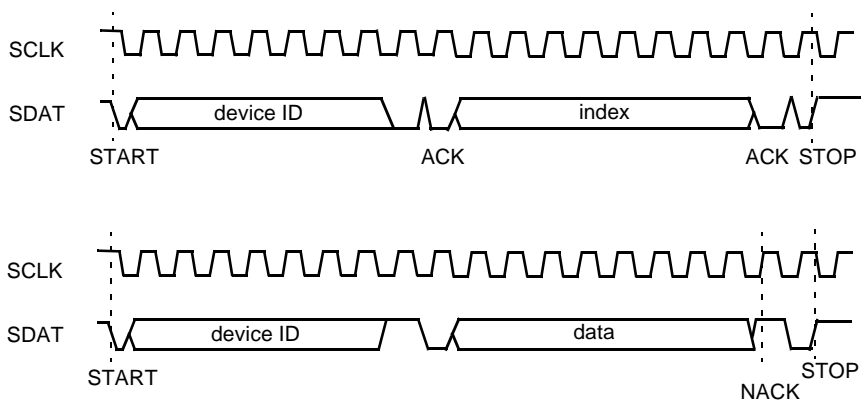


Figure 40. IIC Data Read

2. CONTROL REGISTER DESCRIPTION

This section contains information concerning the programmable control registers. Table 14 provides the default power up values for each index, and a bit map for each register. The following pages describe each register in detail and the possible programming values (an * indicates the power-on default). Gamma correction registers are write only. When the index register points to any of the Gamma correction register, the Gamma look-up table is put into a program mode. Normal operation resumes when the index is outside the range from 0x40 to 0xFF.

Table 14: Register Summary

| Index | Mnemonic | Default | Bit Map | | | | | | | | |
|-------|----------|---------|------------|-------------|------------|-------------|-------------|--------------|--------------|---------|--------|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0x00 | STAT | RO | CHIPID | VBIFLG | NOVID | FFRDET | PALDET | CDET | HLOCK | CLOCK | |
| 0x01 | CMDA | 2C | POWDN | VSE | HFSEL[1:0] | | XT24 | PIXSEL | MNFMT | IFMT | |
| 0x02 | CMDB | 20 | AGCGN | VALIGN | AGCOVF | AGCFRZ | INSEL[3:0] | | | | |
| 0x03 | CMDC | 00 | VMEN | TSTGE1 | 0 | TSTGPK | TSTGPH | TSTGFR[1:0] | | TSTGEN | |
| 0x04 | CMDD | 00 | EAV | 0 | CKDIR | INPSL[1:0] | | SYNDIR | Y1MHZ | GPPOINT | |
| 0x05 | HAVB | 00 | HAVB[7:0] | | | | | | | | |
| 0x06 | HAVE | 00 | HAVE[7:0] | | | | | | | | |
| 0x07 | HS1B | 00 | HS1B[8:1] | | | | | | | | |
| 0x08 | HS1E | 00 | HS1E[8:1] | | | | | | | | |
| 0x09 | HS2B | 00 | HS2B[8:1] | | | | | | | | |
| 0x0A | HS2E | 00 | HS2E[8:1] | | | | | | | | |
| 0x0B | AGC | 50 | AGC[7:0] | | | | | | | | |
| 0x0C | HXTRA | 00 | HAVB[10:8] | | | | HAVE[10:8] | | | HS1BE0 | HS2BE0 |
| 0x0D | CDEM | 00 | OUTHIZ | FSEC | 0 | CIFCMP[1:0] | | 0 | 0 | 0 | |
| 0x0E | PORTAB | 00 | DIRB | DATAB[2:0] | | | DIRA | DATAA[2:0] | | | |
| 0x0F | LUMA | 00 | 0 | UNIT | RGBH | PED | HYBWR | CTRAP | HYPK[1:0] | | |
| 0x10 | CON | 00 | CONT[7:0] | | | | | | | | |
| 0x11 | BRT | 00 | BRT[7:0] | | | | | | | | |
| 0x12 | CHROMA | 08 | ACCFRZ | PALM | PALN | CBW | CORE[1:0] | | CKILL[1:0] | | |
| 0x13 | CHROMB | 00 | CDLY[3:0] | | | | SCHCMP[3:0] | | | | |
| 0x14 | DEMOD | 00 | FSCDET | SECDET | CDMLPF | CTRACK | MNFSC[1:0] | | MNSECAM[1:0] | | |
| 0x15 | SAT | 00 | SAT[7:0] | | | | | | | | |
| 0x16 | HUE | 00 | HUE[7:0] | | | | | | | | |
| 0x17 | VERTIA | 00 | MNYCMB | YCMBCO[2:0] | | | VRT2X | VCTRL[2:0] | | | |
| 0x18 | VERTIB | 00 | HYLPF[2:0] | | | HYBWI | HYDEC | VSCLLEN[1:0] | | 0 | |
| 0x19 | VERTIC | 03 | MNCCMB | CCMBCO[2:0] | | | ACMBEN | VYBW | EVAVEV | EVAVOD | |
| 0x1A | HSCLL | 00 | HSCL[6:0] | | | | | | | | CMBMOD |
| 0x1B | HSCLH | 00 | HSCL[14:7] | | | | | | | | |
| 0x1C | VSCLL | FC | VSCL[5:0] | | | | | | ACMBCO | ACMBRE | |
| 0x1D | VSCLH | FF | VSCL[13:6] | | | | | | | | |
| 0x1E | OFMTA | - | GAMEN[1:0] | | OENC[1:0] | | OFMT[3:0] | | | | |
| 0x1F | OFMTB | 00 | VSVAV | EVAND[1:0] | | EVHS1 | EVHAV | EVEHAV | EVAVG | EVANDL | |

Table 14: Register Summary

| Index | Mnemonic | Default | Bit Map | | | | | | | |
|---------|----------|---------|----------------------------|-------------|------------------------------|--------------|-------------|--------------|-------------|---------|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x20 | VBICTL | 00 | VBCVBS | VYFMT[1:0] | | VBINSRT | ODDEN | EVENEN | ODDOS[1:0] | |
| 0x21 | CCDAT1 | RO | b0 | b1 | b2 | b3 | b4 | b5 | b6 | P1 |
| 0x22 | CCDAT2 | RO | b0 | b1 | b2 | b3 | b4 | b5 | b6 | P2 |
| 0x23 | VBIL30 | 00 | VBIL3 | | VBIL2 | | VBIL1 | | VBIL0 | |
| 0x24 | VBIL74 | 00 | VBIL7 | | VBIL6 | | VBIL5 | | VBIL4 | |
| 0x25 | VBIL118 | 00 | VBIL11 | | VBIL10 | | VBIL9 | | VBIL8 | |
| 0x26 | VBIL1512 | 00 | VBIL15 | | VBIL14 | | VBIL13 | | VBIL12 | |
| 0x27 | TTFRAM | 00 | TTFRAM[7:0] | | | | | | | |
| 0x28 | TESTA | 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x29 | UVOFFH | 00 | TSTCLC | TSTCGN | 0 | TSTCFR | UOFFST[5:4] | | VOFFST[5:4] | |
| 0x2A | UVOFFL | 33 | UOFFST[3:0] | | | | VOFFST[3:0] | | | |
| 0x2B | UGAIN | 00 | UGAIN[7:0] | | | | | | | |
| 0x2C | VGAIN | 00 | VGAIN[7:0] | | | | | | | |
| 0x2D | VAVB | 23 | VAVB[6:1] | | | | | | VAVOD0 | VAVEV0 |
| 0x2E | VAVE | 82 | VAVE[8:1] | | | | | | | |
| 0x2F | CTRACK | 00 | 0 | 0 | DMCTL[1:0] | | CGTC[1:0] | | CFTC[1:0] | |
| 0x30 | POLCTL | 00 | EVAVPL | VSPL | ODDPL | HAVPL | EHAVPL | HS2PL | VAVPL | HS1PL |
| 0x31 | REFCOD | 00 | YCRANG | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x32 | INVALY | 10 | INVALY[7:0] | | | | | | | |
| 0x33 | INVALU | 80 | INVALU[7:0] | | | | | | | |
| 0x34 | INVALV | 80 | INVALV[7:0] | | | | | | | |
| 0x35 | UNUSEY | 10 | UNUSEY[7:0] | | | | | | | |
| 0x36 | UNUSEU | 80 | UNUSEU[7:0] | | | | | | | |
| 0x37 | UNUSEV | 80 | UNUSEV[7:0] | | | | | | | |
| 0x38 | EXCTRL | 00 | 0 | ENINCST | 0 | - | AUCPWD | 0 | 0 | CLEVEL |
| 0x39 | TRACKA | 00 | STCTRL | MAC_DET | VCR_DET | VCR_LEV[1:0] | | ATCTRAP | VCTRAP | AGCLSB |
| 0x3A | VBICTLB | 00 | VBISWAP | TT_SYS[1:0] | | VBIMID | NEW_CC | CC_OVFL | YOFFENB | COFFENB |
| 0x3B | TRACKB | 00 | ALT656 | VBI_PH | VBI_FR | PH_CTRL | VNOISCT | AGC_LPG[1:0] | | AGC_LKG |
| 0x3C | RTC | 00 | RTC.DTO | RTC.PID | 0 | TDMOD | 0 | 0 | 0 | 0 |
| 0x3D | CMDE | 09 | ODFST | VSALG | HCORE[1:0] | | CHIPREVID | | | |
| 0x3E | VSDEL | 00 | TR_MS | NOVIDC | VSDEC[5:0] | | | | | |
| 0x3F | CMDF | 00 | CTRAPPSC | VIPMODE | EVAVY | UVDLEN | UVDLSL | REGUD | TASKB | CBWI |
| 0x40-5F | GAMMA | - | GAMMA0[7:0] - GAMMA31[7:0] | | | | | | | |
| 0x60-7F | GAMMAD | - | - | - | GAMMAD0[5:0] - GAMMAD31[5:0] | | | | | |
| 0xC0-DF | GAMUV | - | GAMUV0[7:0] - GAMUV31[7:0] | | | | | | | |
| 0xE0-FF | GAMUVD | - | - | - | GAMUVD0[5:0] - GAMUVD31[5:0] | | | | | |

| Read Only Status Bits | | | | | | | | | |
|-----------------------|----------|--------|--------|-------|--------|--------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 00h | STAT | CHIPID | VBIFLG | NOVID | FFRDET | PALDET | CDET | HLOCK | CLOCK |

| | |
|--------|--|
| CLOCK | Status for color lock. |
| 0 | Not locked. |
| 1 | Color lock achieved. |
| HLOCK | Status for current line tracking mode. |
| 0 | Chip is in initial tracking mode. |
| 1 | Chip is in steady state tracking mode. |
| CDET | Status for detection of color. |
| 0 | No color signal is detected. |
| 1 | Color signal is detected. |
| PALDET | Status for current detected color format. Information contained in this bit is valid only if CLOCK is 1. |
| 0 | NTSC color format. |
| 1 | PAL color format. |
| FFRDET | Status for current detected field frequency. |
| 0 | 50 Hz field frequency, i.e. N,B,G,H,I,D,K,K1,L system. |
| 1 | 60 Hz field frequency, i.e. M system. |
| NOVID | Video detect flag. This bit should not be used for detecting the presence of a TV channel from the output of a TV tuner. |
| 0 | Sync has been detected for the last 32 lines. |
| 1 | No sync has been detected. |
| VBIFLG | Vertical blanking interval flag. |
| 0 | Video is in active region. |
| 1 | Video is in vertical blanking region. |
| CHIPID | Chip version ID. Please refer to the CHIPREVID bits for additional information |
| 0 | KS0122S. |
| 1 | KS0127. |

| Control Register A | | | | | | | | | |
|--------------------|----------|-------|-------|------------|-------|-------|--------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 01h | CMDA | POWDN | VSE | HFSEL[1:0] | | XT24 | PIXSEL | MNFMT | IFMT |

| | |
|------------|---|
| IFMT | Manual video input standard select. Standard selection can be controlled automatically if MNFMT=0 . |
| 0 | Chip is forced to assume input is 50 Hz.* |
| 1 | Chip is forced to assume input is 60 Hz. |
| MNFMT | Manual input format control override. When this bit is 1 the IFMT bit is enabled. |
| 0 | The chip determines the input video standard based on the detected field rate:* NTSC if 60 Hz. PAL/SECAM if 50 Hz. |
| 1 | Input video standard is selected with the IFMT bit. |
| PIXSEL | Select pixel sampling rate. |
| 0 | Output data is at square pixel rate. |
| 1 | Output data is at CCIR 601 rate.* |
| XT24 | Select the external clock reference frequency. |
| 0 | External clock is 26.8 MHz. |
| 1 | External clock is 24.576 MHz.* |
| HFSEL[1:0] | Horizontal tracking loop frequency select. |
| 0 | Force loop to very fast. |
| 1 | Force loop to fast. |
| 2 | Force loop to VCR time constant.* |
| 3 | Force loop to TV time constant. |
| VSE | Change the vertical end location of the VS. |
| 0 | Line 10/10.5.* |
| 1 | Line 9/9.5. |
| POWDN | Power down mode. |
| 0 | Normal operation.* |
| 1 | All chip functions except microprocessor interface and CK/CK2 generation are disabled. The output of the CK/CK2 pins retains the most recent frequency when the power down mode is enabled. |

| Control Register B | | | | | | | | | |
|--------------------|----------|-------|--------|--------|--------|------------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 02h | CMDB | AGCGN | VALIGN | AGCOVF | AGCFRZ | INSEL[3:0] | | | |

| | |
|------------|--|
| INSEL[3:0] | <p>Analog input channel select.</p> <p>0 AY0 is composite input.*</p> <p>1 AY1 is composite input.</p> <p>2 AY2 is composite input.</p> <p>4 AC0 is composite input.</p> <p>5 AC1 is composite input.</p> <p>6 AC2 is composite input.</p> <p>8 AY0 is luminance input, AC0 is chrominance input.</p> <p>9 AY1 is luminance input, AC1 is chrominance input.</p> <p>A AY2 is luminance input, AC2 is chrominance input.</p> <p>F AY2 is luminance input, AC1 is Cb input, AC2 is Cr input.</p> |
| AGCFRZ | <p>Freeze the analog AGC for the Y and C paths at their current values.</p> <p>0 AGC is running. Reading AGC register returns the current AGC gain.*</p> <p>1 AGC is frozen. Gain can be changed or read with AGC register.</p> |
| AGCOVF | <p>AGC gain control mode.</p> <p>0 AGC gain tracks to sync tip and back porch delta.</p> <p>1 If ADC overflows, AGC gain will be reduced (this has higher priority over normal sync tip - back porch tracking).*</p> |
| VALIGN | <p>VS edge alignment control.</p> <p>0 VS leading edge occurs during serration pulses (typically within the first serration pulse). VS trailing edge is aligned to half line or beginning of the line depending on the field.*</p> <p>1 VS leading edge is aligned to half line or beginning of the line depending on the field. VS trailing edge is always aligned to beginning of the line.</p> |
| AGCGN | <p>AGC gain calculation.</p> <p>0 Normal mode. AGC gain calculation is based on sync tip to back porch difference equal to 68 ADC code.*</p> <p>1 AGC gain calculation is base on sync tip to back porch difference equal to 54 ADC code. This will reduce the AGC gain by a factor of 1/1.25 compare to normal mode. When used in conjunction with PED and RGBH, this effectively increases the input dynamic range.</p> |

| Control register C | | | | | | | | | |
|--------------------|----------|-------|--------|-------|--------|--------|-------------|-------|--------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 03h | CMDC | VMEN | TSTGE1 | 0 | TSTGPK | TSTGPH | TSTGFR[1:0] | | TSTGEN |

| | |
|-------------|--|
| TSTGEN | Enable manual control of horizontal phase and frequency tracking. 0 Auto phase and frequency tracking.* 1 Enable manual control of horizontal phase and frequency with TSTGFR[1:0] and TSTGPH . |
| TSTGFR[1:0] | When TSTGEN == 1, these two bits control the horizontal frequency tracking. 00 Stop frequency tracking and freeze the frequency at the current value.* 01 Horizontal frequency tracks the input. 1X Horizontal frequency tracking ignores video input and runs at nominal value based on the field rate and output pixel rate selected by IFMT and PIXEL bits. |
| TSTGPH | When TSTGEN == 1, this bit controls the horizontal phase tracking. 0 No phase tracking.* 1 Horizontal phase tracks the input video or HS1 input if in slave mode. |
| TSTGPK | If TSTGE1 == 1, this bit controls AGC. 0 AGC clamps to back porch and gain is set based on sync tip-back porch difference.* 1 AGC clamps to sync tip and gain is set based on peak-valley difference. |
| TSTGE1 | Enables the function of TSTGPK . 0 Disables TSTGPK .* 1 Enables TSTGPK . |
| VMEN | Vertical master mode. 0 Normal vertical sync operation.* 1 Vertical sync ignores input and free runs at 50 Hz or 60 Hz. This mode can be used to generate video timing for a slave device. |

| Control Register D | | | | | | | | | |
|--------------------|----------|-------|-------|-------|------------|-------|--------|-------|--------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 04h | CMDD | EAV | 0 | CKDIR | INPSL[1:0] | | SYNDIR | Y1MHZ | GPPORT |

| | |
|------------|---|
| GPPORT | General purpose port. This register is useful only if DATAA[2:0] == 7. If DIRA == 0, this bit is read only and reflects the logic state at PORTA pin. If DIRA == 1, any value written to this bit will appear at PORTA pin. |
| Y1MHZ | Luma bandwidth control. 0 Luma bandwidth is controlled by other luma filters in the luma path.* 1 Luma data is low pass filtered to 1MHz bandwidth. |
| SYNDIR | HS1 and VS pin direction control. 0 HS1 and VS are output.* 1 HS1 and VS are input. |
| INPSL[1:0] | Video input and clock source select. 0 Video source is analog and connected to the chip's analog input. Clock is internally generated.* 1 Video source is 8-bit digital CbYCr and connected to EXV0 through EXV7 pins. 3 Video source is 8-bit digitized CVBS and connected to EXV0 through EXV7 pins. |
| CKDIR | Clock select. 0 Clock is from internal clock generator. A reference clock at XTALI pin is required.* 1 Clock is from CK pin. When this is selected, the CK pin automatically becomes an input. |
| EAV | In 8-bit digital CbYCr input mode, this bit selects the sync source. 0 Horizontal and vertical syncs are from HS1 and VS pins, respectively.* 1 Syncs are embedded in the 8-bit digital data stream (CCIR 656 compatible). |

| HAV Start Control | | | | | | | | | | |
|-------------------|----------|------------|-------|-------|------------|-------|-------|--------|--------|--|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | |
| 05h | HAVB | HAVB[7:0] | | | | | | | | |
| 0Ch | HXTRA | HAVB[10:8] | | | HAVE[10:8] | | | HS1BE0 | HS2BE0 | |

HAVB[10:0] This 11-bit register is used to define the start location of the HAV signal relative to the sync tip (for CVBS input, this is the composite video sync tip. For 8-bit CbYCr input, this is the leading edge of the HS1 or EAV). The content of this register is a 2's complement number which is used as an offset to the default. The resolution for this register is 1 CK clock.

| HAV End Control | | | | | | | | | | |
|-----------------|----------|------------|-------|-------|------------|-------|-------|--------|--------|--|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | |
| 06h | HAVE | HAVE[7:0] | | | | | | | | |
| 0Ch | HXTRA | HAVB[10:8] | | | HAVE[10:8] | | | HS1BE0 | HS2BE0 | |

HAVE[10:0] This 11-bit register is used to define the end location of the HAV signal relative to the sync tip. The content of this register is a 2's complement number which is used as an offset to the default. The resolution for this register is 1 CK clock.

| HS1 Start Control | | | | | | | | | | |
|-------------------|----------|------------|-------|-------|------------|-------|-------|--------|--------|--|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | |
| 07h | HS1B | HS1B[8:1] | | | | | | | | |
| 0Ch | HXTRA | HAVB[10:8] | | | HAVE[10:8] | | | HS1BE0 | HS2BE0 | |

HS1B[8:1] - HS1BE0 If HS1 is programmed as an output, this 9-bit register defines the start location of the HS1 signal. The content of this register is a 2's complement number which is used as an offset to the default. The resolution for this register is 1 CK clock.

| HS1 End Control | | | | | | | | | | |
|-----------------|----------|------------|-------|-------|------------|-------|-------|--------|--------|--|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | |
| 08h | HS1E | HS1E[8:1] | | | | | | | | |
| 0Ch | HXTRA | HAVB[10:8] | | | HAVE[10:8] | | | HS1BE0 | HS2BE0 | |

HS1E[8:1] - If HS1 is programmed as an output, this 9-bit register defines the end location of the HS1 signal. The content of this register is a 2s complement number which is used as an offset to the default. The resolution for this register is 1 CK clock.

HS1BE0

| HS2 Start Control | | | | | | | | | | |
|-------------------|----------|------------|-------|-------|------------|-------|-------|--------|--------|--|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | |
| 09h | HS2B | HS2B[8:1] | | | | | | | | |
| 0Ch | HXTRA | HAVB[10:8] | | | HAVE[10:8] | | | HS1BE0 | HS2BE0 | |

HS2B[8:1] - This 9-bit register defines the start location of the HS2 signal. The content of this register is a 2s complement number which is used as an offset to the default HS2B location. The resolution for this register is 1 CK clock.

HS2BE0

| HS2 End Control | | | | | | | | | | |
|-----------------|----------|------------|-------|-------|------------|-------|-------|--------|--------|--|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | |
| 0Ah | HS2E | HS2E[8:1] | | | | | | | | |
| 0Ch | HXTRA | HAVB[10:8] | | | HAVE[10:8] | | | HS1BE0 | HS2BE0 | |

HS2E[8:1] - This 9-bit register defines the end location of the HS2 signal. The content of this register is a 2s complement number which is used as an offset to the default HS2E location. The resolution for this register is 1 CK clock.

HS2BE0

| AGC Control | | | | | | | | | |
|-------------|----------|----------|-------|-------|-------|-------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x0B | AGC | AGC[7:0] | | | | | | | |

AGC[7:0] This register is used to manually set AGC when **AGCFRZ** is set to "1". The content in the register is unsigned.

| Chroma Demodulation Control | | | | | | | | | |
|-----------------------------|----------|--------|-------|-------|-------------|-------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0Dh | CDEM | OUTHIZ | FSEC | 0 | CIFCMP[1:0] | | 0 | 0 | 0 |

CIFCMP[1:0] IF compensation for the chroma path.
 0 No compensation.*
 1 Upper chroma side band is 1 dB higher than lower side band.
 2 Upper chroma side band is 3 dB higher than lower side band.
 3 Upper chroma side band is 6 dB higher than lower side band.

FSEC Chroma frequency demodulation filter select for SECAM video.
 0 Select SECAM chroma frequency demodulation filter if SECAM video is detected.*
 1 Always use SECAM chroma frequency demodulation filter.

OUTHIZ This is the software output three-state control bit. If this bit is set to a "1", or the OEN pin is at a logic LOW level, output pins can be selectively put in the high impedance state using the additional software control bits **OENC[1:0]**.
 0 This is default setting.*
 1 This will enable the output pins to be three-stated regardless the state of the OEN pin.

| Port A and B Control | | | | | | | | | |
|----------------------|----------|-------|------------|-------|-------|-------|------------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0Eh | PORTAB | DIRB | DATAB[2:0] | | | DIRA | DATAA[2:0] | | |

| | |
|------------|---|
| DATAA[2:0] | Port A data select. For internal gate signal locations. |
| 0 | Port A is disconnected from the internal signal path.* |
| 1 | Port A is connected to the BPG (back porch gate) signal. |
| 2 | Port A is connected to the SYG (sync tip gate) signal. |
| 3 | Port A is connected to the CBG (color burst gate) signal. |
| 4 | Port A is connected to the CBGW (color burst gate wide) signal. The CBGW is high for the entire color burst period. |
| 5 | Port A is connected to the SLICE (mid way of the sync tip) signal. |
| 6 | Port A is connected to the VBI (vertical blanking interval) signal. |
| 7 | Port A is connect to the GPPORT bit. |
| DIRA | Port A direction control. |
| 0 | Port A is configured as input. The input is connected directly to the signal path selected by DATAA[2:0] . The internally generated gate signal is disconnected from the signal path.* |
| 1 | Port A is an output and is driven by the internally generated signal as selected by DATAA[2:0] . |
| DATAB[2:0] | Port B data select. For internal gate signal locations. |
| 0 | Port B is disconnected from the internal signal path.* |
| 1 | Port B is connected to the SCH (sync tip to color burst phase) signal. |
| 2 | Port B is connected to the FH2 (twice per line pulses) signal. |
| 3 | Port B is connected to the FS_PULSE (falling edge of the sync tip) signal. |
| 4 | Port B is connected to the VBI_CVBS (VBI raw ADC) signal. This signal is high for those lines that output data directly from the ADC (not YUV or RGB data). |
| 5 | Port B is connected to the VBI_PROC (VBI sliced) signal. This signal is high for those video lines that output sliced VBI data. |
| 6 | Port B is connected to the VS (Vertical Sync) signal. |
| 7 | Port B is configured as the RTCO (Real Time Control Output). This single pin serial interface transmits phase and frequency information to a video encoder so that it may operate directly from the KS0127B output clock. |
| DIRB | Port B direction control. |
| 0 | Port B is configured as input. The input is connected directly to the signal path selected by DATAB[2:0] . The internally generated gate signal is disconnected from the signal path.* |
| 1 | Port B is an output and is driven by the internally generated signal as selected by DATAB[2:0] . |

| Luma Control Register | | | | | | | | | |
|-----------------------|----------|-------|-------|-------|-------|-------|-------|-----------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x0F | LUMA | 0 | UNIT | RGBH | PED | HYBWR | CTRAP | HYPK[1:0] | |

| | |
|-----------|--|
| HYPK[1:0] | Luminance horizontal peaking control around 3 MHz. |
| 0 | Less than nominal peaking.* |
| 1 | Nominal peaking. |
| 2 | Increased peaking. |
| 3 | Maximum peaking. |
| CTRAP | Chroma trap (notch filter) in the luma path. |
| 0 | No chroma trap. This mode is recommended for S-video or component video input.* |
| 1 | Chroma trap is enabled. |
| HYBWR | Luminance horizontal bandwidth reduction control. |
| 0 | Full bandwidth.* |
| 1 | Reduced bandwidth. |
| PED | Enable gain correction for 7.5 blank-to-black setup (pedestal). |
| 0 | No pedestal. 0% = Y code 16. 100% = Y code 235.* |
| 1 | Gain adjusted for 7.5% blank-to-black setup (pedestal). 7.5% = Y code 16. 7.5% - 100% input produce Y code 16 - 235. |
| RGBH | High gain to produce full range Y for 0% (or 7.5% if PED = 1) to 100% input. |
| 0 | Black (0% or 7.5%) to peak white(100%) input produce Y code 16 to 235.* |
| 1 | Black (0% or 7.5%) to peak white(100%) input produce Y code 0 to 255. |
| UNIT | When PED and RGBH are both set to a "1", setting this bit to a "1" produces a unit gain for CCIR 601 digital input (INPSL[1:0] = 1). |
| 0 | Luma DC gain is controlled by PED and RGBH as described for each bit.* |
| 1 | Luma DC gain is unity for CCIR 601 digital input. |

| Contrast Control | | | | | | | | | |
|------------------|----------|----------|-------|-------|-------|-------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x10 | CON | CON[7:0] | | | | | | | |

CON[7:0] This 8-bit register contains a 2's complement number for contrast control.

| Brightness Control | | | | | | | | | |
|--------------------|----------|----------|-------|-------|-------|-------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x11 | BRT | BRT[7:0] | | | | | | | |

BRT[7:0] Brightness control register. The number contained in the register is 2's complement.

| Chroma Control Register A | | | | | | | | | |
|---------------------------|----------|--------|-------|-------|-------|-----------|-------|------------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x12 | CHROMA | ACCFRZ | PALM | PALN | CBW | CORE[1:0] | | CKILL[1:0] | |

| | |
|------------|--|
| CKILL[1:0] | Color kill. |
| 0 | Auto detect mode. If color burst is too low or no color burst, chroma data is forced to code 128.* |
| 2 | Chroma is always ON. |
| 3 | Chroma data is always forced to code 128. |
| CORE[1:0] | Chroma data coring. |
| 0 | No coring. |
| 1 | Chroma data within the range 128+/-1, inclusive, will be force to 128. |
| 2 | Chroma data within the range 128+/-3, inclusive, will be force to 128.* |
| 3 | Chroma data within the range 128+/-7, inclusive, will be force to 128. |
| CBW | Chroma bandwidth control. |
| 0 | Chroma 3 dB bandwidth is 850 kHz.* |
| 1 | Chroma 3 dB bandwidth is 550 kHz. |
| PALN | Select color tracking for PAL-N, or NTSC-N when input field rate is 50 Hz and Fsc is 3.58 MHz. |
| 0 | Select NTSC-N.* |
| 1 | Select PAL-N. |
| PALM | Select color tracking for PAL-M or NTSC-M when input field rate is 60 Hz. |
| 0 | Select color tracking for NTSC-M.* |
| 1 | Select color tracking for PAL-M. |
| ACCFRZ | Chroma gain tracking freeze control. |
| 0 | Chroma gain tracks the input. Color saturation can be adjusted with SAT .* |
| 1 | Chroma gain freezes at the current saturation level. |

| Chroma Control Register B | | | | | | | | | |
|---------------------------|----------|-----------|-------|-------|-------|-------------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x13 | CHROMB | CDLY[3:0] | | | | SCHCMP[3:0] | | | |

SCHCMP[3:0] Phase constant compare value for color burst phase relative to sync tip. Each step is 22.5 degrees with the value of 0 equal to 0 degree.

CDLY[3:0] Chroma path group delay relative to the luma path (in unit of CK):

| | |
|---|------------|
| 0 | No delay.* |
| 1 | -0.5 |
| 2 | 1 |
| 3 | 0.5 |
| 4 | 2 |
| 5 | 1.5 |
| 6 | 3 |
| 7 | 2.5 |
| 8 | -4 |
| 9 | -4.5 |
| A | -3 |
| B | -3.5 |
| C | -2 |
| D | -2.5 |
| E | -1 |
| F | -1.5 |

| Chroma Demodulation Control and Status | | | | | | | | | |
|--|----------|--------|---------|--------|--------|------------|-------|--------------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x14 | DEMOD | FSCDET | SECDDET | CDMLPF | CTRACK | MNFSC[1:0] | | MNSECAM[1:0] | |

| | |
|--------------|---|
| MNSECAM[1:0] | Enable manual SECAM input detection. |
| 0 | Detection of SECAM input is automatic.* |
| 2 | Force the chip to assume input is not SECAM. |
| 3 | Force the chip to assume input is SECAM. |
| MNFSC[1:0] | Enable manual Fsc detection. |
| 0 | Detection of Fsc frequency is automatic.* |
| 2 | Force chip to assume input Fsc is 4.43 MHz or 4.286 MHz. |
| 3 | Force chip to assume input Fsc is 3.58 MHz. |
| CTRACK | Chroma frequency tracking mode. |
| 0 | Chroma frequency tracking is based on the field rate and Fsc.* |
| 1 | Chroma frequency tracking is based on field rate only. |
| CDMLPF | Bypass the LPF in the chroma demodulator. |
| 0 | Chroma data pass through the LPF for color demodulation.* |
| 1 | Chroma data bypass the LPF. This setting is used for component video input. |
| SECDDET | SECAM detection (read only). |
| 0 | Chip did not detect SECAM input. |
| 1 | Chip detected SECAM input. |
| FSCDET | Color subcarrier detection (read only). |
| 0 | Chip detected 4.43 MHz or 4.286 MHz Fsc. |
| 1 | Chip detected 3.58 MHz Fsc. |

| Color Saturation Control | | | | | | | | | |
|--------------------------|----------|----------|-------|-------|-------|-------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x15 | SAT | SAT[7:0] | | | | | | | |

SAT[7:0] Color saturation control register. Register content is in 2s compliment if **TSTCGN**=0. 0 value corresponds to nominal saturation.

| Hue Control | | | | | | | | | |
|-------------|----------|----------|-------|-------|-------|-------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x16 | HUE | HUE[7:0] | | | | | | | |

HUE[7:0] Hue control register. The register content is in 2s compliment format. It covers the range from -180° to +178.59° degree. The resolution is 1.41°/LSB.

| Vertical Processing Control A | | | | | | | | | |
|-------------------------------|----------|--------|-------------|-------|-------|-------|------------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x17 | VERTIA | MNYCMB | YCMBCO[2:0] | | | VRT2X | VCTRL[2:0] | | |

| | |
|-------------|---|
| VCTRL[2:0] | Luminance vertical filter control. |
| 0 | Scaler uses LPF path, comb uses HPF.* |
| 1 | Scaler uses full bandwidth, comb is disabled. |
| 2 | Scaler is disabled, comb uses full bandwidth. |
| 3 | Scaler uses LPF, comb is disabled. |
| 4 | Scaler is disabled, comb uses HPF. |
| VRT2X | 3/5-tap vertical scaler filter select. |
| 0 | Select 3-tap vertical scaler filter.* |
| 1 | Select 5-tap vertical scaler filter. This option can be used only if horizontally cropped line is less than or equal to 384 pixels. |
| YCMBCO[2:0] | Luma comb filter coefficients selection when the MNYCMB is set to "1". |
| 0 | [1/4 1/2 1/4].* |
| 1 | [3/8 1/2 1/8]. |
| 2 | [1/2 1/2 0]. |
| 3 | [1 0 0]. |
| 4 | [0 1 0]. |
| 5 | [1/2 0 1/2]. |
| 6 | [0 1/2 1/2]. |
| 7 | [1/8 1/2 3/8]. |
| MNYCMB | Select between auto and manual luma comb filter coefficients. |
| 0 | Luma comb filter coefficients are automatically selected based on input video standard.* |
| 1 | Luma comb filter coefficients are selected with YCMBCO[2:0] . |

| Vertical Processing Control B | | | | | | | | | |
|-------------------------------|----------|-------------|-------|-------|-------|-------|--------------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x18 | VERTIB | HYLPPF[2:0] | | | HYBWI | HYDEC | VSCLLEN[1:0] | | 0 |

| | |
|--------------|--|
| VSCLLEN[1:0] | Vertical scaling enable. |
| 0 | Vertical scaling is enabled.* |
| 1 | Vertical scaling is disabled. |
| 2 | Vertical scaling is disabled. Video is 1-line delayed. |
| 3 | Vertical scaling is disabled. Video is 2-line delayed. |
| HYDEC | Luma path decimation filter enable. |
| 0 | Luma path decimation is enabled.* |
| 1 | Luma path decimation is disabled. |
| HYBWI | Luma path decimation filter bandwidth select. |
| 0 | Normal bandwidth.* |
| 1 | Bandwidth is 1 MHz higher. |
| HYLPPF[2:0] | Horizontal luma LPF bandwidth control. |
| 0 | Full bandwidth.* |
| 1 | 4.5 MHz bandwidth. |
| 2 | 3.5 MHz bandwidth. |
| 3 | 2.5 MHz bandwidth. |
| 4 | 1.5 MHz bandwidth. |

| Vertical Processing Control C | | | | | | | | | | |
|-------------------------------|----------|--------|-------------|-------|-------|--------|-------|--------|--------|--|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | |
| 0x19 | VERTIC | MNCCMB | CCMBCO[2:0] | | | ACMBEN | VYBW | EVAVEV | EVAVOD | |

| | |
|-------------|--|
| EVAVOD | Enable VAV signal output during ODD field. |
| 0 | VAV signal is disabled (always inactive) during ODD field. |
| 1 | VAV signal is enabled during ODD field.* |
| EVAVEV | Enable VAV signal output during EVEN field. |
| 0 | VAV signal is disabled (always inactive) during EVEN field. |
| 1 | VAV signal is enabled during EVEN field.* |
| VYBW | Luma vertical bandwidth control. |
| 0 | Full bandwidth.* |
| 1 | Reduced bandwidth. |
| ACMBEN | Enable luma active comb for NTSC. |
| 0 | Active comb is disabled.* |
| 1 | Active comb is enabled. |
| CCMBCO[2:0] | Manual chroma comb filter coefficients select. |
| 0 | Select the coefficient set [1/2 1/2 0] (if VRT2X = 0).* |
| 1 | Select the coefficient set [1/4 1/2 1/4] (if VRT2X = 0). |
| 2 | Select the coefficient set [0 1/2 1/2 0 0] (if VRT2X = 1). |
| 3 | Select the coefficient set [0 1/4 1/2 1/4 0] (if VRT2X = 1). |
| 4 | Select the coefficient set [1 0 0]. |
| 5 | Select the coefficient set [0 1 0]. |
| 6 | Select the coefficient set [0 0 1]. |
| 7 | No output (disabled). |
| MNCCMB | Chroma comb filter coefficients are selected automatically or manually. |
| 0 | Filter coefficients are automatically selected based on the selected video input standard. SECAM must use this value.* |
| 1 | Filter coefficients are selected manually with CCMBCO[2:0] . |

| Horizontal Scaling Ratio | | | | | | | | | | |
|--------------------------|----------|------------|-------|-------|-------|-------|-------|-------|--------|--|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | |
| 0x1A | HSCLL | HSCL[6:0] | | | | | | | CMBMOD | |
| 0x1B | HSCLH | HSCL[14:7] | | | | | | | | |

- CMBMOD** This bit controls when comb is enabled internally.
- 0 Comb is enabled by the internal signal COMB_EN.*
- 1 Comb is enabled when VAV is active.
- HSCL[14:0]** The 15-bit register defines a horizontal scaling ratio of $HSCL[14:0]/2^{15}$. Any change to this value will become effective during the next vertical sync.

| Vertical Scaling Ratio | | | | | | | | | | |
|------------------------|----------|------------|-------|-------|-------|-------|-------|--------|--------|--|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | |
| 0x1C | VSCLL | VSCL[5:0] | | | | | | ACMBCO | ACMBRE | |
| 0x1D | VSCLH | VSCL[13:6] | | | | | | | | |

- ACMBRE** Active comb filter threshold select.
- 0 High threshold.*
- 1 Low threshold.
- ACMBCO** Active comb filter coefficient set select.
- 0 Use the set of coefficients for 100% comb.*
- 1 Use the set of coefficients for 75% comb.
- VSCL[13:0]** The 14-bit register defines a vertical scaling ratio of $VSCL[13:0]/2^{14}$. Any change to this value will become effective during the next vertical sync.

| Output Control A | | | | | | | | | |
|------------------|----------|------------|-------|-----------|-------|-----------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x1E | OFMTA | GAMEN[1:0] | | OENC[1:0] | | OFMT[3:0] | | | |

| | |
|------------|--|
| OFMT[3:0] | Digital video output format select. 16 and 24 bit data are output at CK2 clock rate. 8 bit data are output at CK clock rate. |
| 0 | 16-bit YCbCr 4:2:2 output on the Y and C output ports.* |
| 1 | 12-bit YCbCr 4:1:1 output on the Y and C output ports. |
| 2 | 8-bit YCbCr 4:2:2 without embedded timing reference codes. |
| 3 | 8-bit YCbCr 4:2:2 with embedded timing reference codes. |
| 4 | 24-bit YCbCr 4:4:4. |
| 5 | 16-bit RGB 565. |
| 6 | 24-bit RGB 888 with linear bit ordering. |
| 7 | 24-bit RGB 888, bit ordering is an extension of the 16-bit RGB 565 format. |
| 8 | Same as mode 2 with the additional of 8-bit YCbCr 4:2:2 data output on the EXV port. While the Y port can be scaled down, the EXV port will always be a full size picture. |
| 9 | Same as 8 with the addition of SAV and EAV codes. |
| A | output Y ADC data all the time (including syncs) on the Y port, C port is non-scaled 656 data with no timing codes. |
| B | Output Y ADC data all the time (including syncs) on the Y port, Output C ADC data all the time (including syncs) on the C port, |
| OENC[1:0] | When either the OEN pin is low or the OUTHIZ is a "1", these two bits will determine which output pins are three-stated. |
| 0 | All video pins are three-stated. |
| 1 | All video pins, plus HAV, VAV, EVAV, EHAV, PID, ODD, HS1, HS2, VS, and SCH are three-stated. |
| 2 | All pins listed above, plus CK and CK2 are three-stated. |
| 3 | Always output data. |
| GAMEN[1:0] | Gamma correction enable. |
| 0 | No gamma correction.* |
| 1 | Gamma correction is applied to Y/G data. |
| 2 | Gamma correction is applied to U/B and V/R data. |
| 3 | Gamma correction is applied to Y/G, U/B, and V/R data. |

| Output Control B | | | | | | | | | |
|------------------|----------|-------|------------|-------|-------|-------|--------|-------|--------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x1F | OFMTB | VSAV | EVAND[1:0] | | EVHS1 | EVHAV | EVEHAV | EVAVG | EVANDL |

| | |
|-----------------------|--|
| EVAVG | Gate EVAV with VAV before sending to output. |
| 0 | EVAV is not gated with VAV. EVAV may be active outside of active VAV region.* |
| 1 | EVAV is gated with VAV. EVAV can be active only when VAV is active. |
| EVEHAV | Additional qualifier for EHAV. |
| 0 | No additional qualifier.* |
| 1 | EHAV uses qualifier from EVAND[1:0] . |
| EVHAV | Additional qualifier for HAV. |
| 0 | No additional qualifier.* |
| 1 | HAV uses qualifier from EVAND[1:0] . |
| EVHS1 | Additional qualifier for HS1. |
| 0 | No additional qualifier.* |
| 1 | HS1 uses qualifier from EVAND[1:0] . |
| EVAND[1:0], EVANDL | Qualifier signal that defines active video lines. This control enables 656 codes, HAV, EHAV and HS1. EVANDL is the EVAND LSB. These three bits are grouped together and explained below |
| 0 | Qualifier is active for all lines.* |
| 1 | Qualifier is EVAV. -- Any line during vertical active or blank will be output. |
| 2 | Qualifier is EVAV and VAV -- All lines during vertical blank (VAV==0) and all lines when EVAV is active during vertical active will be output. |
| 3 | Qualifier is VAV -- All lines during vertical active will be output. |
| 4 | Qualifier is EVAV and VAV -- All lines that EVAV is active during vertical active will be output. |
| 5 | Qualifier is EVAV, VAV and VBI_RAW_EN -- All lines as in option 4 plus the VBI RAW ADC lines. |
| 6 | Qualifier is EVAV, VAV, VBI_RAW_EN and VBI_SLC_EN-- All lines as in option 5 plus the VBI Sliced Lines. |
| 7 | All VBI sliced and VBI RAW Lines only. |
| VSAV | Enable VAV to be output to VS. |
| 0 | Output normal VS.* |
| 1 | VS has the same output as VAV |

| VBI Decoder Control | | | | | | | | | |
|---------------------|----------|--------|------------|-------|---------|-------|--------|------------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x20 | VBICTL | VBCVBS | VYFMT[1:0] | | VBINSRT | ODDEN | EVENEN | ODDOS[1:0] | |

| | |
|------------|---|
| ODDOS[1:0] | Line offset for ODD field. See also VBIL [15:0]. |
| 0 | ODD field line offset is -1 compared to EVEN field.* |
| 1 | No offset. |
| 2 | ODD field line offset is 1 compared to EVEN field. |
| 3 | ODD field line offset is 2 compared to EVEN field. |
| EVENEN | VBI data processing for EVEN field. |
| 0 | No processing.* |
| 1 | VBI processing is enabled for EVEN field. |
| ODDEN | VBI data processing for ODD field. |
| 0 | No processing.* |
| 1 | VBI processing is enabled for ODD field. |
| VBINSRT | Enable VBI data to be output on the Y bus. |
| 0 | VBI data is not output on the Y bus.* |
| 1 | VBI data is output on the Y bus. |
| VYFMT[1:0] | When VBINSRT = 1, these bits control how VBI data are output on the Y bus. |
| 0 | 1 bit on Y7 per CK2 clock.* |
| 1 | 1 bit on Y7 plus a "1" on Y3 per CK2 clock. |
| 2 | 4 bits on Y7..Y4, with first bit on Y7, last bit on Y4, plus a "1" on Y3 per CK2 clock. |
| 3 | 8 bits on Y7..Y0, with first bit on Y7, last bit on Y0, per CK2 clock. |
| VBCVBS | Enable digitized CVBS data from ADC to be output for the selected VBI line instead of sliced VBI data. The new VBIMID bit allows simultaneous output (line by line bases) of sliced data and raw ADC data. |
| 0 | Output sliced VBI data for any line whose VBIL value $\neq 0$.* |
| 1 | Output digitized CVBS data for any line whose VBIL value $\neq 0$. |

| First Decoded Close-Caption Data Byte (Read Only) | | | | | | | | | |
|---|----------|-------|-------|-------|-------|-------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x21 | CCDAT1 | b0 | b1 | b2 | b3 | b4 | b5 | b6 | P1 |

CCDAT1 This byte contains the first byte of the decoded close-caption data as defined in EIA-608. In order for this register to receive the CC data, **VBINSRT** must be programmed to a "1", and **VYFMT[1:0]** must be programmed with the value 3. The same applies to **CCDAT2**. For normal NTSC Closed Caption decoding, **ODDEN** should be set to a "1", **VBIL12** should be programmed with the value 1.

| Second Decoded Close-Caption Data Byte (Read Only) | | | | | | | | | |
|--|----------|-------|-------|-------|-------|-------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x22 | CCDAT2 | b0 | b1 | b2 | b3 | b4 | b5 | b6 | P2 |

CCDAT2 This byte contains the second byte of the decoded close-caption data as defined in EIA-608.

| VBI Data Decoding | | | | | | | | | |
|-------------------|----------|--------|-------|--------|-------|--------|-------|--------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x23 | VBIL30 | VBIL3 | | VBIL2 | | VBIL1 | | VBIL0 | |
| 0x24 | VBIL74 | VBIL7 | | VBIL6 | | VBIL5 | | VBIL4 | |
| 0x25 | VBIL118 | VBIL11 | | VBIL10 | | VBIL9 | | VBIL8 | |
| 0x26 | VBIL1512 | VBIL15 | | VBIL14 | | VBIL13 | | VBIL12 | |

VBIL0..VBLI15 These 16 2-bit numbers select how the chip should decode the VBI data for each VBI line. For 60 Hz video, **VBIL1** through **VBIL15** correspond to lines 10 through 24 in the ODD field, and lines 273 through 286 in the EVEN field for NTSC (refer to NTSC line numbering convention). For 50 Hz video, **VBIL1** corresponds to line 7 in the ODD field, and line 320 in the EVEN field. **VBIL0** is used for all other lines not covered by **VBIL1** through **VBIL15**.

- 0 Decode normal video.*
- 1 Decode Closed Caption data.
- 2 Decode Teletext data.
- 3 Decode WSS data.

| Teletext Frame Alignment Pattern | | | | | | | | | |
|----------------------------------|----------|-------------|-------|-------|-------|-------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x27 | TTFRAM | TTFRAM[7:0] | | | | | | | |

TTFRAM[7:0] User programmable Teletext frame alignment pattern.

| UV Offset Adjustment | | | | | | | | | |
|----------------------|----------|-------------|--------|-------|--------|-------------|-------|-------------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x29 | UVOFFH | TSTCLC | TSTCGN | 0 | TSTCFR | UOFFST[5:4] | | VOFFST[5:4] | |
| 0x2A | UVOFFL | UOFFST[3:0] | | | | VOFFST[3:0] | | | |

VOFFST[5:0], UOFFST[5:0] These two 6-bit 2's complement values are for offset adjustment to the U and V components of the chroma data. The resolution is 1/4 LSB of the 8-bit U and V.

TSTCFR Chroma frequency tracking control.
 0 Chroma frequency tracking is enabled.*
 1 Chroma frequency tracking is open loop.

TSTCGN Chroma gain control.
 0 Chroma gain tracks input.*
 1 Chroma gain is controlled by SAT only.

TSTCLC Cloche filter bypass.
 0 Cloche filter is enabled for SECAM input.*
 1 DC bypass of the cloche filter.

| U Component Gain Adjustment | | | | | | | | | |
|-----------------------------|----------|------------|-------|-------|-------|-------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x2B | UGAIN | UGAIN[7:0] | | | | | | | |

UGAIN[7:0] U component gain adjustment. The nominal value is 0.

| V Component Gain Adjustment | | | | | | | | | |
|-----------------------------|----------|------------|-------|-------|-------|-------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x2C | VGAIN | VGAIN[7:0] | | | | | | | |

VGAIN[7:0] V component gain adjustment. The nominal value is 0.

| VAV Begin | | | | | | | | | |
|-----------|----------|-----------|-------|-------|-------|-------|-------|--------|--------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x2D | VAVB | VAVB[6:1] | | | | | | VAVOD0 | VAVEV0 |

VAVEV0 The LSB for VAVB and VAVE for the even field.

VAVOD0 The LSB for VAVB and VAVE for the odd field.

VAVB[6:1] The 6 MSBs of a 7-bit unsigned number which defines the start of VAV. The value "0" corresponds to line 4.

| VAV End | | | | | | | | | |
|---------|----------|-----------|-------|-------|-------|-------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x2E | VAVE | VAVE[8:1] | | | | | | | |

VAVE[8:1] The 8 MSBs of a 9-bit unsigned number which defines the end of VAV. The value "0" corresponds to line 4.

| Chroma Tracking Control Register | | | | | | | | | |
|----------------------------------|----------|-------|-------|------------|-------|-----------|-------|-----------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x2F | CTRACK | 0 | 0 | DMCTL[1:0] | | CGTC[1:0] | | CFTC[1:0] | |

CFTC[1:0] Chroma frequency tracking time constant.

- 0 Slower.*
- 1 Slow.
- 2 Fast.
- 3 Faster.

CGTC[1:0] Chroma gain tracking time constant.

- 0 Slower.*
- 1 Slow.
- 2 Fast.
- 3 Faster.

DMCTL[1:0] Chroma demodulation bypass mode.

- 0 Chroma demodulation is enabled.*
- 1 Chroma demodulation is bypassed for digital YCbCr input.
- 2 Chroma demodulation is bypassed for analog YCbCr input. Cb path is phase delayed by one half of CK2 clock period.
- 3 Chroma demodulation is bypassed for analog YCbCr input. Cr path is phase delayed by one half of CK2 clock period.

| Timing Signal Polarity Control | | | | | | | | | |
|--------------------------------|----------|--------|-------|-------|-------|--------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x30 | POLCTL | EVAVPL | VSPL | ODDPL | HAVPL | EHAVPL | HS2PL | VAVPL | HS1PL |

| | |
|--------|---|
| HS1PL | HS1 polarity. |
| | 0 Active high.* |
| | 1 Active low. |
| VAVPL | VAV polarity. |
| | 0 Active high.* |
| | 1 Active low. |
| HS2PL | HS2 polarity. |
| | 0 Active high.* |
| | 1 Active low.* |
| EHAVPL | EHAV polarity. |
| | 0 Active high.* |
| | 1 Active low. |
| HAVPL | HAV polarity. |
| | 0 Active high.* |
| | 1 Active low. |
| ODDPL | ODD polarity (this also affects the F bit in 656 code). |
| | 0 Active high.* |
| | 1 Active low. |
| VSPL | VS polarity (this also affect the V bit in 656 code). |
| | 0 Active high.* |
| | 1 Active low. |
| EVAVPL | EVAV polarity. |
| | 0 Active high.* |
| | 1 Active low. |

| Reference Code Insertion Control | | | | | | | | | |
|----------------------------------|----------|--------|-------|-------|-------|-------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x31 | REFCOD | YCRANG | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

YCRANG Digital video output range control.

0 Y and C ranges are limited to 1 - 254; R, G, and B ranges are limited to 1 - 254.*

1 Y range is limited to 16 - 235; C range is limited to 16 - 240; R, G, and B ranges are limited to 16 - 240.

| Invalid Y Code | | | | | | | | | |
|----------------|----------|-------------|-------|-------|-------|-------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x32 | INVALY | INVALY[7:0] | | | | | | | |

INVALY[7:0] User programmed code to be output for Y data when HAV is active but EHAV is inactive.

| Invalid U Code | | | | | | | | | |
|----------------|----------|-------------|-------|-------|-------|-------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x33 | INVALU | INVALU[7:0] | | | | | | | |

INVALU[7:0] User programmed code to be output for U data when HAV is active but EHAV is inactive.

| Invalid V Code | | | | | | | | | |
|----------------|----------|-------------|-------|-------|-------|-------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x34 | INVALV | INVALV[7:0] | | | | | | | |

INVALV[7:0] User programmed code to be output for V data when HAV is active but EHAV is inactive.

| Unused Y Code | | | | | | | | | |
|---------------|----------|-------------|-------|-------|-------|-------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x35 | UNUSEY | UNUSEY[7:0] | | | | | | | |

UNUSEY[7:0] User programmed code to be output for Y data when HAV is inactive.

| Unused U Code | | | | | | | | | |
|---------------|----------|-------------|-------|-------|-------|-------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x36 | UNUSEU | UNUSEU[7:0] | | | | | | | |

UNUSEU[7:0] User programmed code to be output for U data when HAV is inactive.

| Unused V Code | | | | | | | | | |
|---------------|----------|-------------|-------|-------|-------|-------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x37 | UNUSEV | UNUSEV[7:0] | | | | | | | |

UNUSEV[7:0] User programmed code to be output for V data when HAV is inactive.

| Extra Control Bits for the KS0127B Version | | | | | | | | | |
|--|----------|-------|---------|-------|-------|--------|-------|-------|--------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x38 | EXCTRL | 0 | ENINCST | 0 | - | AUCPWD | 0 | 0 | CLEVEL |

| | |
|---------|--|
| CLEVEL | Programmable CKILL burst level select bit. |
| 0 | Burst peak level is 11 IRE.* |
| 1 | Burst peak level is 5.5 IRE. |
| AUCPWD | Auto chroma ADC power down mode enabled when appropriate input format is selected. |
| 0 | Chroma ADC powered down only during entire chip power down mode.* |
| 1 | Chroma ADC is power downed when CVBS input or case 0'condition. |
| ENINCST | Scaler enable control bit during VBI. |
| 0 | Scaler on during VBI interval (defined by VAV).* |
| 1 | Scaler off during VBI interval. |

| Tracking Configuration Controls A | | | | | | | | | |
|-----------------------------------|----------|--------|---------|---------|--------------|-------|---------|---------|--------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x39 | TRACKA | STCTRL | MAC_DET | VCR_DET | VCR_LEV[1:0] | | ATCTRAP | VBCTRAP | AGCLSB |

| | |
|---------|--|
| AGCLSB | AGC LSB for control of the 9 bit AGC gain value. This bit only write to AGC when AGCFRZ is 1. |
| 0 | Write 0'to AGC 9 bit control LSB if AGCFRZ = 1.* |
| 1 | Write 1'to AGC 9 bit control LSB if AGCFRZ = 1. |
| VBCTRAP | Chroma trap enabled during the VBI. |
| 0 | Chroma trap is controlled by CTRAP only.* |
| 1 | Chroma trap enabled during VBI. |
| ATCTRAP | Auto Chroma Trap on luma path when VCR input is detected. |
| 0 | Chroma trap is controlled by CTRAP only.* |
| 1 | If VCR type input is detected, then CTRAP is enabled. |
| VCR_LEV | Set the Fh variation from nominal for detection of VCR type input. |
| 0 | 50 PPM.* |
| 1 | 100 PPM. |
| 2 | 200 PPM. |
| 3 | 400 PPM. |
| VCR_DET | Status bit. Detect input that is not SCH locked such as consumer type VCR (Read only). |
| 0 | SCH locked video. |
| 1 | Color burst not locked to Fh (VCR). |
| MAC_DET | Status bit. Macrovision Encoded Data detected as input video source (Read only). |
| 0 | Standard video detected. |
| 1 | Macrovision Encoded data detected. |
| STCTRL | State machine transition control. |
| 0 | Normal state machine transitions.* |
| 1 | Steady state sync level removed as condition for lock. |

| VBI Control Register B | | | | | | | | | |
|------------------------|----------|---------|-------------|-------|--------|--------|---------|---------|---------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x3A | VBICTLB | VBISWAP | TT_SYS[1:0] | | VBIMID | NEW_CC | CC_OVFL | YOFFENB | COFFENB |

| | |
|---------|---|
| COFFENB | Disable control for the C-path clamp control. |
| 0 | C-path clamp works as normal.* |
| 1 | C-path clamp disabled. |
| YOFFENB | Disable control for the Y-path clamp control.* |
| 0 | Y-path clamp works as normal.* |
| 1 | Y-path clamp disabled. |
| CC_OVFL | Defines when the current CCDAT1,2 data has over written previous data that was not read. (Read Only) |
| 0 | Current data has not generated an overflow condition. |
| 1 | Current data as written over data that was not read. |
| NEW_CC | Defines when new Closed Caption data is ready for reading from the CCDAT1,2 bytes. (Read Only) |
| 0 | Current data in CCDAT1,2 has already been read. |
| 1 | Current data in CCDAT1,2 is new. |
| VBIMID | Changes function of WSS enable (per line bases during VBI) to a raw CVBS enable. |
| 0 | When VBIL (0-15) = 3, current line is enabled for WSS slicing.* |
| 1 | When VBIL (0-15) = 3, current line is enabled for raw ADC output. |
| TT_SYS | Select Teletext input system when auto detect is not possible. |
| 0 | Auto Teletext Select.* |
| 1 | Teletext System B. |
| 2 | Teletext System C. |
| 3 | Teletext System D. |
| VBISWAP | Reverse the bit order for data output from the closed caption or Teletext slicer. |
| 0 | Same as KS0127 -- First bit sliced is located in MSB position.* |
| 1 | First bit sliced (in time) is located in LSB position. |

| Tracking Configuration Controls B | | | | | | | | | |
|-----------------------------------|----------|--------|--------|--------|---------|---------|--------------|-------|---------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x3B | TRACKB | ALT656 | VBI_PH | VBI_FR | PH_CTRL | VNOISCT | AGC_LPG[1:0] | | AGC_LKG |

| | |
|---------|---|
| AGC_LKG | AGC gain tracking loop time constant for initial tracking mode. |
| 0 | Same as steady state time constant.* |
| 1 | 2X faster than selected steady state time constant. |
| AGC_LPG | AGC gain steady state tracking loop time constant. |
| 0 | Fastest.* |
| 1 | Fast. |
| 2 | Slow. |
| 3 | Slowest. |
| VNOISCT | Vertical sync noise control enable. |
| 0 | Vertical sync adjusts with all sync phase changes.* |
| 1 | Vertical sync large phase errors must occur for 4 lines to activate a phase change. |
| PH_CTRL | Controls phase detector response. |
| 0 | Syncs after the '0' point reference have priority.* |
| 1 | Syncs prior to '0' point reference have priority. |
| VBI_FR | Disables frequency compensation for VCR head switch lines only. |
| 0 | Frequency tracking independent of this control.* |
| 1 | Frequency tracking disabled for VCR head switch lines. |
| VBI_PH | Enables phase compensation for VCR head switch lines only. |
| 0 | Phase tracking independent of this control.* |
| 1 | Phase tracking enabled for VCR head switch lines only. |
| ALT656 | Alternate 656 Vertical blank location for 50 Hz video. |
| 0 | Vertical blank size per the ITU 656 Specification (ends at 656 digital line 23).* |
| 1 | Vertical blank size same as 60 Hz (ends at 656 digital line (50 Hz) 6). |

| RTC Genlock output signal control | | | | | | | | | |
|-----------------------------------|----------|---------|---------|-------|-------|-------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x3C | RTC | RTC_DTO | RTC_PID | 0 | TDMOD | 0 | 0 | 0 | 0 |

| | |
|---------|---|
| TDMOD | Test bit for chroma demodulation mode. |
| 0 | Normal operation.* |
| 1 | Test mode. |
| RTC_PID | Polarity control for PAL ID transferred within the RTC data stream. |
| 0 | Same polarity as default PID pin.* |
| 1 | Inverted polarity. |
| RTC_DTO | Enables a DTO reset inside the KS0127B and sends a DTO reset within the RTC data stream. Function is activated on the rising edge of RTC_DTO. |
| 0 | Function disabled.* |
| 1 | Function enabled one time when set to 1. |

| Command Register E | | | | | | | | | |
|--------------------|----------|-------|-------|------------|-------|-----------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x3D | CMDE | ODFST | VSALG | HCORE[1:0] | | CHIPREVID | | | |

| | |
|-----------|---|
| CHIPREVID | Four additional bits for determination of current Revision and differentiation from the KS0127. |
| 0 | KS0127. |
| 9 | KS0127B Revision A.* |
| HCORE | Luma path horizontal coring. Noise limiter for high frequency portion of luma. |
| 0 | Coring function is disabled.* |
| 1 | 1 bit of coring. |
| 2 | 2 bits of coring. |
| 3 | 4 bits of coring. |
| VSALG | Vertical scaling line dropping algorithm. |
| 0 | Vertical scaling drops the same lines in the Odd and Even fields -- good for fast motion video.* |
| 1 | Vertical scaling drops lines based on the final de-interlaced video. This is a better vertical scaling but may be sensitive to fast motion video. |
| ODFST | Alternate the first scaling line between Odd and Even fields. |
| 0 | Even field is the first scaled field.* |
| 1 | Odd field is the first scaled field. |

| VS Delay Control | | | | | | | | | | |
|------------------|----------|-------|--------|------------|-------|-------|-------|-------|-------|--|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | |
| 0x3E | VSDEL | TR_MS | NOVIDC | VSDEL[5:0] | | | | | | |

| | |
|------------|--|
| VSDEL[5:0] | When the chip is programmed for digital video input operation, this register provides an offset for the internal line counter to align with input video (VS can be either from the VS pin or from embedded timing code). The register content is unsigned. |
| NOVIDC | Allows NOVID bit to be output to PORTB (pin 24). 0 Normal operation.* 1 The NOVID bit is output to PORTB if DATAB[2:0]=1 and DIRB=1 . |
| TR_MS | Enable alternative initial tracking mode state machine. 0 Normal operation - Horizontal tracking mode is controlled by the HFSEL[1:0] bits.* 1 Variable tracking modes during locking time. |

| Command Register F | | | | | | | | | |
|--------------------|----------|----------|---------|-------|--------|--------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x3F | CMDF | CTRAPFSC | VIPMODE | EVAVY | UVDLEN | UVDLSL | REGUD | TASKB | CBWI |

| | |
|----------|--|
| CBWI | Chroma bandwidth increase. This function should be used for digital video input mode only. |
| 0 | Normal chroma bandwidth.* |
| 1 | Increased chroma bandwidth. |
| TASKB | Select between task A and B as described in "VIP Specification V. 1.0" |
| 0 | Select CCIR 656 timing codes (T-bit is always 1).* |
| 1 | Select between task A and B when VBI data is output. If active video is output, T-bit is set to 1(task A). If VBI data is output, T-bit is set to 0 (task B). |
| REGUD | Control register update control. |
| 0 | Registers are updated immediately after being written to.* |
| 1 | The following registers and register bits are updated only during the start of vertical sync after they are written to: Index 0x02, indices 0x17 through 0x1D, bit 0 of index 0x04, bits [2:0] and [6:4] of index 0x0E. |
| UVDLSL | U or V delay control when UVDLEN is set to 1. |
| 0 | V is delayed by 1 CK period.* |
| 1 | U is delayed by 1 CK period. |
| UVDLEN | Enable the function of UVDLSL . |
| 0 | UVDLSL is disabled.* |
| 1 | UVDLSL is enabled. |
| EVAVY | Control the output of INVALY, INVALU, and INVALV codes when EVAV is inactive. |
| 0 | Output of these codes are not affected by EVAV.* |
| 1 | These codes are output when EVAV is inactive (line is being dropped by the vertical scaler). |
| VIPMODE | Allows transfer of hardware sliced VBI data as ancillary data during the following lines' horizontal blanking period. |
| 0 | Standard KS0127 original sliced VBI data transfer.* |
| 1 | Optional ancillary sliced VBI data transfer. |
| CTRAPFSC | Enable chroma trap location based on Fsc frequency instead of field rate. |
| 0 | Chroma trap based on field rate (same as KS0127).* |
| 1 | Chroma trap based on detected Fsc frequency. |

| Gamma Base | | | | | | | | | |
|------------|----------|--------------|-------|-------|-------|-------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x40 | GAMMA0 | GAMMA0[7:0] | | | | | | | |
| 0x41 | GAMMA1 | GAMMA1[7:0] | | | | | | | |
| : | : | : | | | | | | | |
| : | : | : | | | | | | | |
| 0x5F | GAMMA31 | GAMMA31[7:0] | | | | | | | |

GAMMA0 Gamma correction base. The desired output for 8*N, where N = 0, .., 31, is programmed into
 -GAMMA31 **GAMMAN**. Note that data written into these addresses are simultaneously written into
 addresses 0xC0 through 0xDF.

| Gamma Correction Delta | | | | | | | | | |
|------------------------|----------|-------|-------|---------------|-------|-------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0x60 | GAMMAD0 | - | - | GAMMAD0[5:0] | | | | | |
| 0x61 | GAMMAD1 | - | - | GAMMAD1[5:0] | | | | | |
| : | : | : | : | : | | | | | |
| : | : | : | : | : | | | | | |
| 0x7F | GAMMAD31 | - | - | GAMMAD31[5:0] | | | | | |

GAMMAD0 The Nth location of the 32 locations is programmed with a 6-bit unsigned number which
 ..GAMMAD31 represents the gamma correction delta for the gamma bases N and N + 1. The last location
 will contain the gamma correction delta for gamma base 31 and presumed base 32 which has
 the value of 256. Note that data written into these addresses are simultaneously written into
 addresses 0xE0 through 0xFF.

| U/V Gamma Base | | | | | | | | | |
|----------------|----------|--------------|-------|-------|-------|-------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0xC0 | GAMUV0 | GAMUV0[7:0] | | | | | | | |
| 0xC1 | GAMUV1 | GAMUV1[7:0] | | | | | | | |
| : | : | : | | | | | | | |
| : | : | : | | | | | | | |
| 0xDF | GAMUV31 | GAMUV31[7:0] | | | | | | | |

GAMUV0 U and V gamma correction base. The desired output for $8*N$, where $N = 0, \dots, 31$, is
 -GAMUV31 programmed into **GAMUVN**.

| U/V Gamma Correction Delta | | | | | | | | | |
|----------------------------|----------|-------|-------|---------------|-------|-------|-------|-------|-------|
| Index | Mnemonic | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0xE0 | GAMUVD0 | - | - | GAMUVD0[5:0] | | | | | |
| 0xE1 | GAMUVD1 | - | - | GAMUVD1[5:0] | | | | | |
| : | : | : | : | : | | | | | |
| : | : | : | : | : | | | | | |
| 0xFF | GAMUVD31 | - | - | GAMUVD31[5:0] | | | | | |

GAMUVD0 U and V gamma correction delta. The Nth location of the 32 locations is programmed with a
 ..GAMUVD31 6-bit unsigned number which represents the gamma correction delta for the gamma bases N and N + 1. The last location will contain the gamma correction delta for gamma base 31 and presumed base 32 which has the value of 256.

ABSOLUTE MAXIMUM RATINGS

| Characteristics | Symbol | Value | Units |
|--|------------|--------------------------|-------|
| 5-V supply voltage (measured to VSS) | V_{DD} | -0.5 to + 7.0 | V |
| 3.3-V supply voltage (measured to VSS) | V_{DD3} | -0.5 to + 4.5 | V |
| Voltage on any digital pin | V_{PIN} | -0.5 to ($V_{DD}+0.5$) | V |
| Ambient operating temperature (case) | T_A | -35 to + 100 | °C |
| Storage temperature | T_S | -65 to + 150 | °C |
| Junction temperature | T_J | 150 | °C |
| Vapor phase soldering (1 min.) | T_{vsol} | 220 | °C |

Notes: 1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions.

2. Functional operation under any of these conditions is not implied.

3. Applied voltage must be current limited to a specified range.

OPERATING CONDITIONS

| Characteristics | Symbol | Min | Typ | Max | Units |
|--|-----------|------|-----|------|-------|
| 5-V supply voltage (measured to VSS) | V_{DD5} | 4.75 | 5.0 | 5.25 | V |
| 3.3-V supply voltage (measured to VSS) | V_{DD3} | 3.0 | 3.3 | 3.6 | V |
| Ambient operating temperature, still air | T_A | -20 | | 70 | °C |

ELECTRICAL CHARACTERISTICS

| Characteristics | Symbol | Min | Typ | Max | Units |
|-----------------|--------|-----|-----|-----|-------|
|-----------------|--------|-----|-----|-----|-------|

Supply

| | | | | | |
|--|------------------|--|-----|--|----|
| +5V (VDD, VDDA, VDDA1), normal operation | I _{DD5} | | 150 | | mA |
| +3.3V (VDD3), normal operation | I _{DD3} | | 141 | | mA |
| +5V (VDD, VDDA, VDDA1), power down mode | I _{DD5} | | 90 | | mA |
| +3.3V (VDD3), power down mode | I _{DD3} | | 5 | | mA |

Analog Characteristics

| | | | | | |
|---|--------------------|-----|-----|-----|-----------------|
| Integral linearity error (AGC/ADC only) | E _{I-ADC} | | 1.0 | 3.0 | lsb |
| Differential linearity error (AGC/ADC only) | E _{D-ADC} | | 0.5 | 1.5 | lsb |
| Total harmonic distortion (4 MHz full scale) | THD | | 54 | | dB |
| Signal to noise ratio (4 MHz full scale) | SNR | | 42 | | dB |
| Analog bandwidth (50 IRE to 3 dB point) | BW | 4 | | | MHz |
| Input voltage range (peak-peak) 100 IRE input | V _{I(PP)} | 0.5 | | 1.5 | V _{pp} |
| Input resistance AY0-AY2,AC0-AC2 | R _{IN} | 200 | | | kΩ |
| Input capacitance for analog video inputs | C _{IN} | | 10 | | pF |
| Charge current for offset control | I _{OFF} | | ±4 | | μA |
| Cross talk between analog inputs | a | | -42 | -50 | dB |

Video Performance

| | | | | | |
|---|---------------------|--|---------|--|--------|
| Luminance frequency response (maximum variation to 4.2 MHz - multi burst) | F _{LUMA} | | 1.5 | | dB |
| Differential gain - complete chip (Modulated 40 IRE ramp) | D _G | | 1.5 | | % |
| Differential phase - complete chip (Modulated 40 IRE ramp) | D _P | | 1.0 | | degree |
| Chrominance frequency response (3 dB point) - CBWR=0/1 | F _{CHROMA} | | 800/500 | | kHz |
| Chroma nonlinear gain distortion (NTC-7 Combination) | C _{NGD} | | 1 | | % |
| Chroma nonlinear phase distortion (NTC-7 Combination) | C _{NPD} | | 1.25 | | degree |
| Chroma to luma intermodulation (NTC-7 Combination) | C _{LI} | | 1 | | IRE |
| Chroma luma gain equality (NTC-7 Composite) | DEL _{CL} | | ±20 | | ns |
| Chroma luma delay equality (NTC-7 Composite) | AMP _{CL} | | 98-101 | | % |
| Noise level for unified weighting 10 kHz-5 MHz (100 IRE unmodulated ramp) | N _{LUMA} | | -58 | | dB |
| Chroma AM noise (red field) | N _{CAM} | | -60 | | dB |
| Chroma PM noise (red field) | N _{CPM} | | -54 | | dB |

| Characteristics | Symbol | Min | Typ | Max | Units |
|---|--------------|---------|-----|---------|---------|
| Digital I/O Characteristics | | | | | |
| Input low voltage (other digital I/O) | V_{IL} | VSS-0.5 | | 0.8 | V |
| Input high voltage (other digital I/O) | V_{IH} | 2.0 | | VDD+0.5 | V |
| Input low voltage (SCLK,SDAT,RST) | V_{IL12C} | VSS-0.5 | | 0.3VDD | V |
| Input high voltage (SCLK,SDAT,RST) | V_{IH12C} | 0.7VDD | | VDD+0.5 | V |
| Input low current ($V_{IN} = 0.4$ V) | I_{IL} | | | -1 | μ A |
| Input high current($V_{IN}=2.4$) | I_{IH} | | | -1 | μ A |
| Digital output low voltage ($I_{OL}=3.2$ mA) | V_{OL} | | | 0.4 | V |
| Digital output high voltage ($I_{OH}=400$ μ A) | V_{OH} | 2.4 | | | V |
| Digital three-state current | I_{OZ} | | | 50 | μ A |
| Digital output capacitance | C_{OUT} | | | 7 | pF |
| Maximum capacitance load for digital data pins | C_{L-DATA} | | | 30 | pF |
| Maximum capacitance load for CK and CK2 outputs | C_{L-CK} | | | 60 | pF |

Timing Characteristics - Digital Inputs

| | | | | | |
|------------------------------|------------|----|----|--|----|
| XTALI input pulse width low | t_{pwlX} | 15 | 20 | | ns |
| XTALI input pulse width high | t_{pwhX} | 15 | 20 | | ns |

Clock and Data Timing

| | | | | | |
|---|----------------------------|----|------|----|----|
| Analog video input to digital video output delay | t_{dCHIP} | | 120 | | CK |
| Pulse width high for CK (KS0112 operates at frequencies from 24.5 MHz to 29 MHz) | t_{pwhCK} | 15 | 18.5 | 22 | ns |
| Pulse width high for CK2 | t_{pwhCK2} | 30 | 37 | 44 | ns |
| Delay from rising edge of CK to CK2 | t_{CK2} | | 4 | | ns |
| Delay from rising edge CK to data change (including pins Y0-Y7, C0-C7, HAV, VAV, EHAV, EVAV, HS1, HS2, VS, ODD, PID, SCH) | t_{dD} (CK is output) | | 16 | 23 | ns |
| | t_{dD} (CK is input) | | 14 | 21 | ns |
| Minimum hold time from rising edge of CK for data output) | t_{hD} | 7 | | | ns |
| Delay from falling edge of OEN to data bits in 3-state | t_{zD} | | | 20 | ns |
| Delay from rising edge OEN to data bits enabled | t_{enD} | | | 18 | ns |

Timing Characteristics -IIC Host Interface

| | | | | | |
|---------------------------------------|------------|-----|--|-----|---------|
| SCLK clock frequency | f_{SCLK} | 0 | | 400 | kHz |
| Capacitive load for each bus line | C_b | | | 400 | pF |
| Hold time for START condition | t_{hSTA} | 0.6 | | | μ s |
| Setup time for STOP condition | t_{sSTO} | 0.6 | | | μ s |
| Rise and fall times for SCLK and SDAT | t_R, t_F | 20 | | 300 | ns |

| Characteristics | Symbol | Min | Typ | Max | Units |
|---|---------------|-----|-----|-----|---------|
| SCLK minimum pulse width low | $t_{pwlSCLK}$ | 1.3 | | | μ S |
| SCLK minimum pulse width high | $t_{pwhSCLK}$ | 0.6 | | | μ S |
| SDAT setup time to rising edge of SCLK | t_{sSDAT} | 100 | | | ns |
| SDAT hold time from rising edge of SCLK | t_{hSDAT} | 0 | | | ns |

Note: AC/DC characteristics provided are per design specifications.

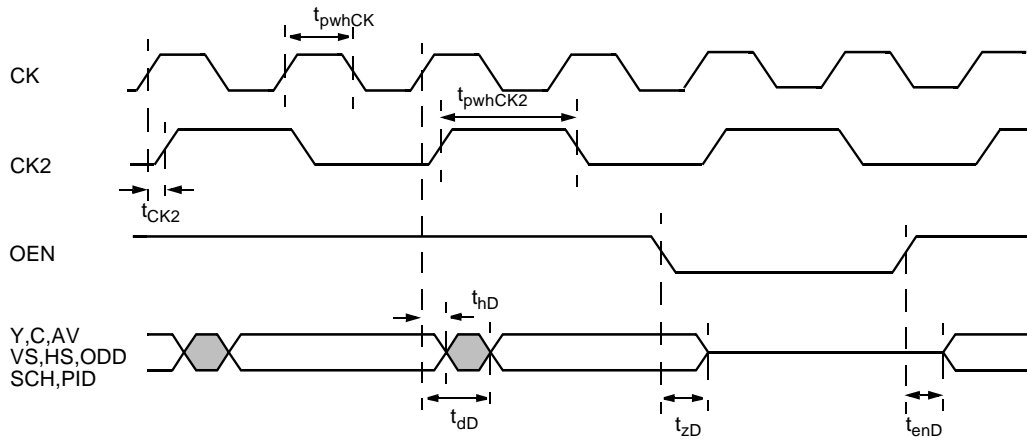


Figure 41. Data Output

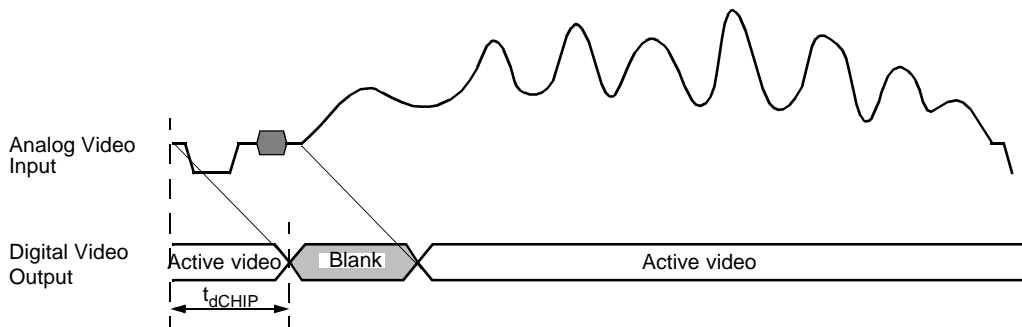


Figure 42. Analog Video Input to Digital Video Output Delay

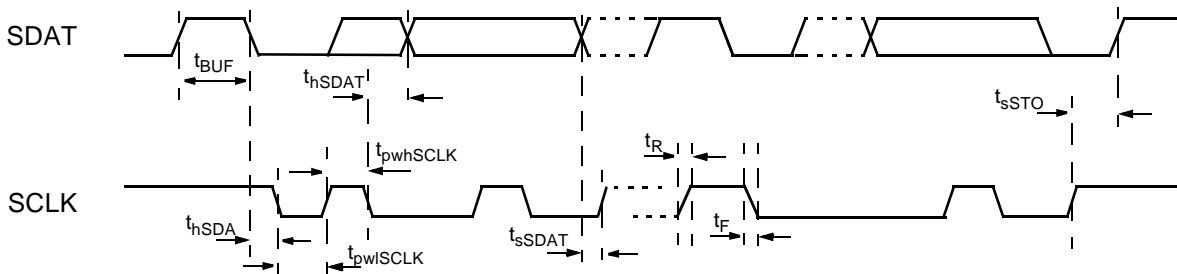
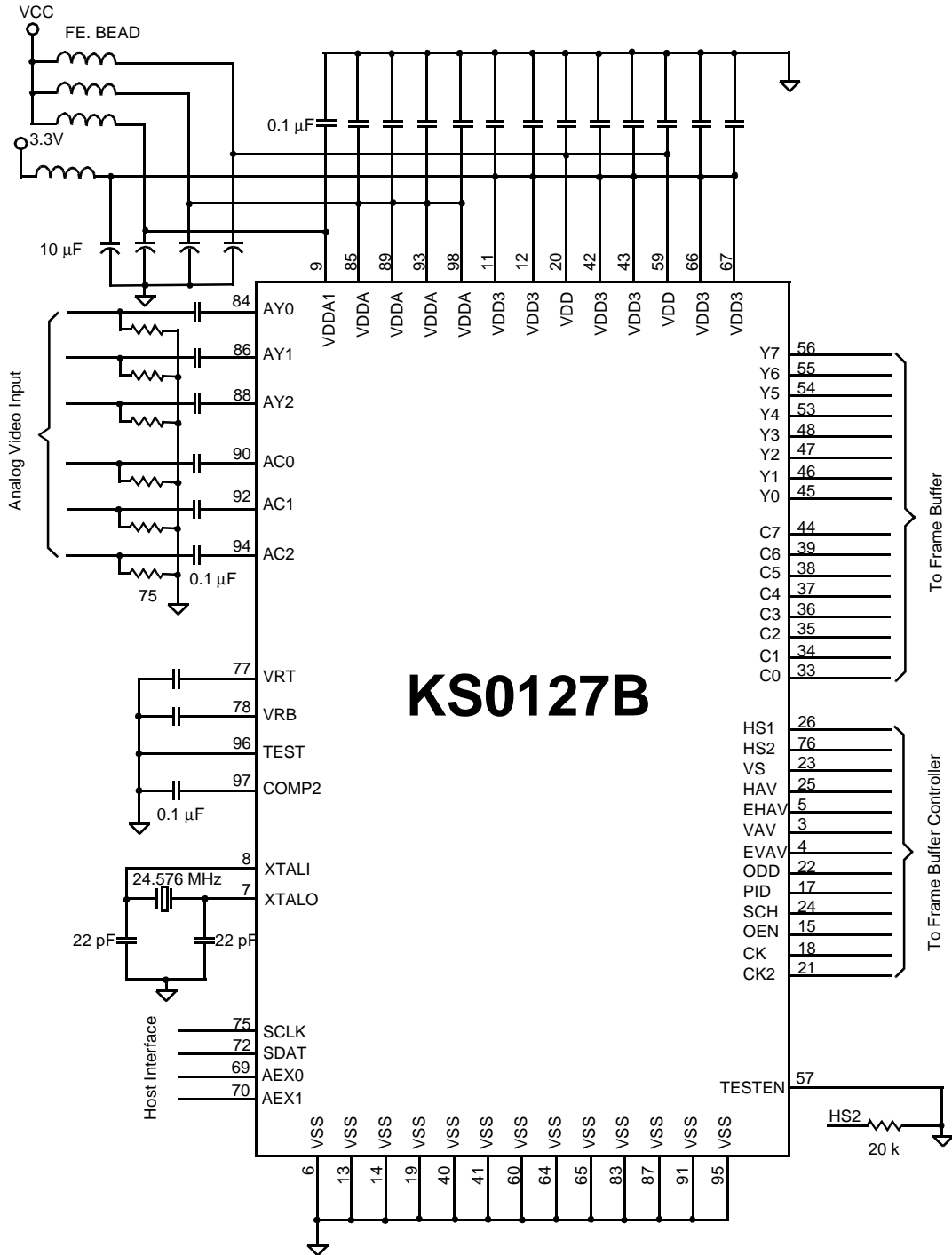


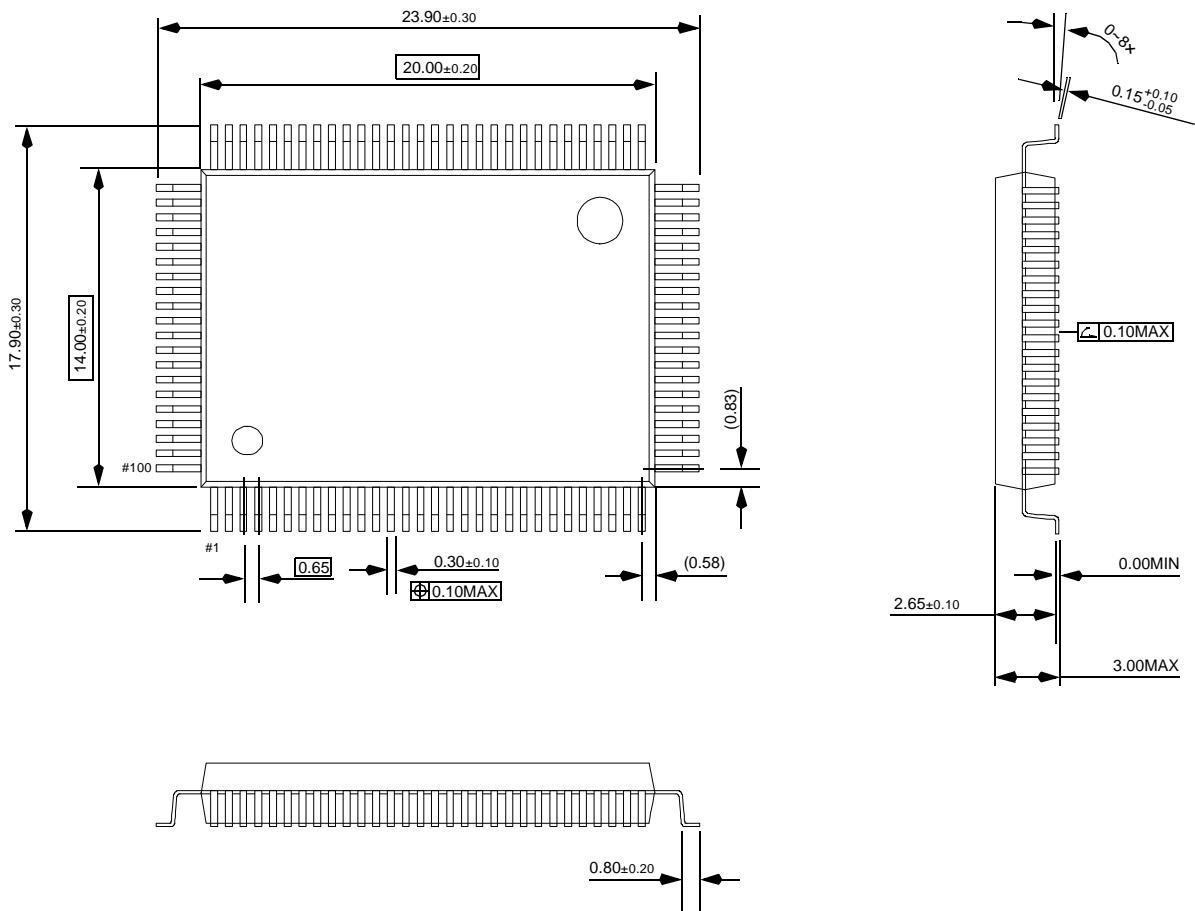
Figure 43. IIC Host Interface Detailed Timing



KS0127B

Package Dimension

100-QFP-1420D



Dimensions are in Millimeters

SAMSUNG SEMICONDUCTOR WORLDWIDE OFFICES**HEAD OFFICE**

8/11FL., SAMUNG MAIN BLDG.
250, 2-KA, TAEPYUNG-RO,
CHUNG-KU, SEOUL, KOREA
TEL: 2-727-7114
FAX: 2-753-0967

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84-11, 5-KA, NAMDAEMOON-RO
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TEL: 2-259-1114
FAX: 2-259-2468

SAMSUNG SEMICONDUCTOR INC.

3655 NORTH FIRST STREET
SAN JOSE, CA 95134, U.S.A.
TEL: 408-954-7000
FAX: 408-954-7873

SAMSUNG SEMICONDUCTOR EUROPE GMBH

SAMSUNG HOUSE
AM KRONBERGER HANG 6
65824, SCHWALBACH/TS
TEL: 49-6196-663300
FAX: 49-6196-663311

SAMSUNG SEMICONDUCTOR EUROPE LTD.

GREAT WEST HOUSE
GREAT WEST ROAD, BRENTFORD
MIDDLESEX TW8 9DQ
TEL: 181-380-7132
FAX: 181-380-7220

SAMSUNG ELECTRONICS JAPAN CO., LTD.

HAMACHO CENTER BLDG.
31-1, NIHONBASHI-HAMACHO, 2-CHOME
CHUO-KU, TOKYO 103, JAPAN
TEL: 3-5641-9850
FAX: 3-5641-9851

SAMSUNG ELECTRONICS HONG KONG CO., LTD.

65TH FL., CENTRAL PLAZA
18 HARBOUR ROAD
WANCHAI, HONG KONG
TEL: 852-2862-6900
FAX: 852-2866-1343

SAMSUNG ELECTRONICS TAIWAN CO., LTD.

30FL., NO.333 KEELUNG RD.
SEC 1, TAIPEI, TAIWAN, R.O.C
TEL: 886-2-757-9292
FAX: 886-2-757-7311

SAMSUNG ASIA PRT., LTD.

80 ROBINSON RD., #20-01
SINGAPORE 068898
TEL: 65-535-2808
FAX: 65-227-2792

**SAMSUNG ELECTRONICS CO., LTD.
SHANGHAI OFFICE**

9F, SHANGHAI INTERNATIONAL TRADE CENTRE
NO.2200 YANAN(W) RD.
SHANGHAI, P.R.C. 200335
TEL: 8621-6270-4168
FAX: 8621-6275-2975

**SAMSUNG ELECTRONICS CO., LTD.
SEMICONDUCTOR BUSINESS BEIJING OFFICE**

15FL., BRIGHT CHINA CHANG AN BLDG.,
NO.7, JIANGUOMEN, NEI AVENUE
BEIJING, CHINA 100005
TEL: 8610-6510-1234(0)

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