Integrated Circuit Systems, Inc.

ICS9FG108
Advance Information

Programmable FTG for Differential P4™ CPU, PCI-Express & SATA Clocks

Recommended Application:

Frequency Timing Generator for Differential CPU, PCI-Express & SATA clocks

Features:

- Generates common frequencies from 14.318 MHz or 25 MHz
- Crystal or reference input
- 8 - 0.7V current-mode differential output pairs
- Supports Serial-ATA at 100 MHz
- Two spread spectrum modes: 0 to -0.5 downspread and +/-0.25% centerspread
- Unused inputs may be disabled in either driven or Hi-Z state for power management.

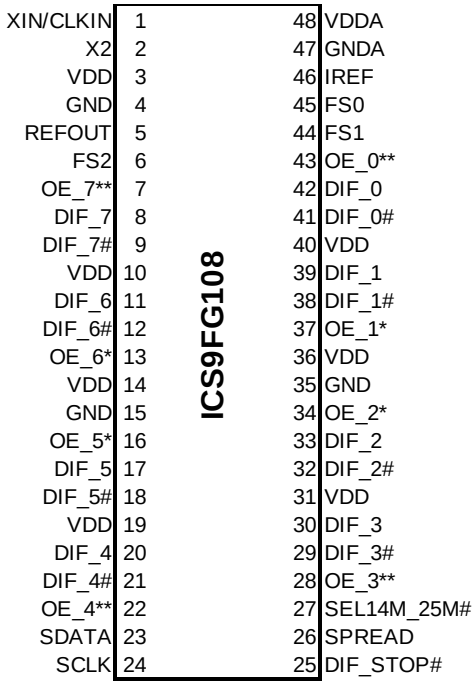
Key Specifications:

- Output cycle-to-cycle jitter < 85 ps
- Output to output skew < 85 ps
- +/-300 ppm frequency accuracy on output clocks

Frequency Select Table

SEL14M_25M# (FS3)	FS2	FS1	FS0	OUTPUT(MHz)
0	0	0	0	100.00
0	0	0	1	125.00
0	0	1	0	133.33
0	0	1	1	166.67
0	1	0	0	200.00
0	1	0	1	266.66
0	1	1	0	333.33
0	1	1	1	400.00
1	0	0	0	100.00
1	0	0	1	125.00
1	0	1	0	133.33
1	0	1	1	166.67
1	1	0	0	200.00
1	1	0	1	266.66
1	1	1	0	333.33
1	1	1	1	400.00

Pin Configuration



Note:

Pin names followed by '**' have 120 Kohm pull DOWN resistors
Pin names followed by an '*' have 120 Kohm pull UP resistors

48-pin SSOP & TSSOP

ADVANCE INFORMATION documents contain information on products in the formative or design phase development. Characteristic data and other specifications are design goals.
Third party brands and names are the property of their respective owners

Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	XIN/CLKIN	IN	Crystal input or Reference Clock input
2	X2	OUT	Crystal output, Nominally 14.318MHz
3	VDD	PWR	Power supply, nominal 3.3V
4	GND	PWR	Ground pin.
5	REFOUT	IN	Reference Clock output
6	FS2	IN	Frequency select pin.
7	OE_7**	IN	Active high input for enabling outputs. 0 = tri-state outputs, 1= enable outputs
8	DIF_7	OUT	0.7V differential true clock outputs
9	DIF_7#	OUT	0.7V differential complement clock outputs
10	VDD	PWR	Power supply, nominal 3.3V
11	DIF_6	OUT	0.7V differential true clock outputs
12	DIF_6#	OUT	0.7V differential complement clock outputs
13	OE_6*	IN	Active high input for enabling outputs. 0 = tri-state outputs, 1= enable outputs
14	VDD	PWR	Power supply, nominal 3.3V
15	GND	PWR	Ground pin.
16	OE_5*	IN	Active high input for enabling outputs. 0 = tri-state outputs, 1= enable outputs
17	DIF_5	OUT	0.7V differential true clock outputs
18	DIF_5#	OUT	0.7V differential complement clock outputs
19	VDD	PWR	Power supply, nominal 3.3V
20	DIF_4	OUT	0.7V differential true clock outputs
21	DIF_4#	OUT	0.7V differential complement clock outputs
22	OE_4**	IN	Active high input for enabling outputs. 0 = tri-state outputs, 1= enable outputs
23	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.
24	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.

Note:
Pin names followed by '**' have 120 Kohm pull DOWN resistors
Pin names followed by '*' have 120 Kohm pull UP resistors

Pin Description (Continued)

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
25	DIF_STOP#	IN	Active low input to stop differential output clocks.
26	SPREAD	IN	Asynchronous, active high input to enable spread spectrum functionality.
27	SEL14M_25M#	IN	Select 14.31818 MHz or 25 Mhz input frequency. 1 = 14.31818 MHz, 0 = 25 MHz
28	OE_3**	IN	Active high input for enabling outputs. 0 = tri-state outputs, 1= enable outputs
29	DIF_3#	OUT	0.7V differential complement clock outputs
30	DIF_3	OUT	0.7V differential true clock outputs
31	VDD	PWR	Power supply, nominal 3.3V
32	DIF_2#	OUT	0.7V differential complement clock outputs
33	DIF_2	OUT	0.7V differential true clock outputs
34	OE_2*	IN	Active high input for enabling outputs. 0 = tri-state outputs, 1= enable outputs
35	GND	PWR	Ground pin.
36	VDD	PWR	Power supply, nominal 3.3V
37	OE_1*	IN	Active high input for enabling outputs. 0 = tri-state outputs, 1= enable outputs
38	DIF_1#	OUT	0.7V differential complement clock outputs
39	DIF_1	OUT	0.7V differential true clock outputs
40	VDD	PWR	Power supply, nominal 3.3V
41	DIF_0#	OUT	0.7V differential complement clock outputs
42	DIF_0	OUT	0.7V differential true clock outputs
43	OE_0**	IN	Active high input for enabling outputs. 0 = tri-state outputs, 1= enable outputs
44	FS1	IN	Frequency select pin.
45	FS0	IN	Frequency select pin.
46	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
47	GNDA	PWR	Ground pin for the PLL core.
48	VDDA	PWR	3.3V power for the PLL core.

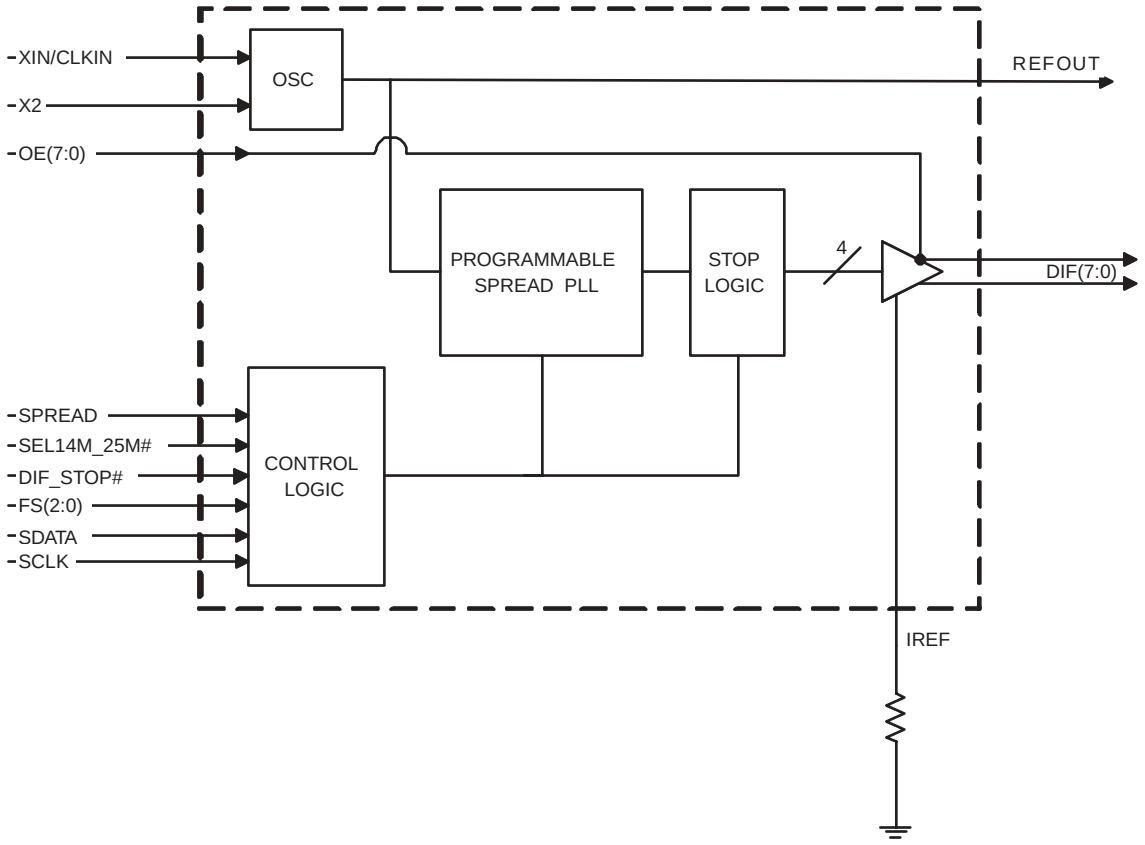
Note:
Pin names followed by '**' have 120 Kohm pull DOWN resistors
Pin names followed by '*' have 120 Kohm pull UP resistors

General Description

ICS9FG108 is a Frequency Timing Generator that provides 8 differential output pairs that are compliant to the Intel CK410 specification. It also provides support for PCI-Express, next generation I/O, and SATA. The part synthesizes several output frequencies from either a 14.31818 Mhz crystal or a 25 MHz crystal. The device can also be driven by a reference input clock instead of a crystal. It provides outputs with cycle-to-cycle jitter of less than 85 ps and output-to-output skew of less than 85 ps.

ICS9FG108 also provides a copy of the reference clock. Frequency selection can be accomplished via strap pins or SMBus control.

Block Diagram



Power Groups

Pin Number		Description
VDD	GND	
3	4	REFOUT, Digital Inputs, SMBus
10,14,19,31,36,40	15,35	DIF Outputs
N/A	47	IREF
48	47	Analog VDD & GND for PLL Core

Absolute Max

Symbol	Parameter	Min	Max	Units
VDD_A	3.3V Core Supply Voltage		V_{DD} + 0.5V	V
VDD_In	3.3V Logic Input Supply Voltage	GND - 0.5	V_{DD} + 0.5V	V
Ts	Storage Temperature	-65	150	°C
Tambient	Ambient Operating Temp	0	70	°C
Tcase	Case Temperature		115	°C
ESD prot	Input ESD protection human body model	2000		V

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage	V_{IH}	3.3 V +/-5%	2		V_{DD} + 0.3	V	
Input Low Voltage	V_{IL}	3.3 V +/-5%	V_{SS} - 0.3		0.8	V	
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	uA	
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA	
Operating Supply Current	$I_{DD3.3OP}$	Full Active, C_L = Full load; f = 400 MHz			250	mA	
		Full Active, C_L = Full load; f = 100 MHz			200	mA	
Input Frequency[3]	F_i	V_{DD} = 3.3 V	14		25	MHz	3
Pin Inductance[1]	L_{pin}				7	nH	1
Input/Output Capacitance[1]	C_{IN}	Logic Inputs	1.5		5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
Clk Stabilization[1,2]	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization to 1st clock			1.8	ms	1,2
Modulation Frequency	f_{MOD}	Triangular Modulation	30		40	kHz	1
DIF output enable	t_{DIFOE}	DIF output enable after DIF_Stop# de-assertion			10	ns	1
Input Rise and Fall times	t_R/t_F	20% to 80% of VDD			5	ns	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]See timing diagrams for timing requirements.

[3] Input frequency should be measured at the REFOUT pin and tuned to ideal 14.31818MHz or 25 MHz to meet ppm frequency accuracy on PLL outputs.

TARGET SPECIFICATION SUBJECT TO CHANGE WITH FULL PRODUCT CHARACTERIZATION

Electrical Characteristics - DIF 0.7V Current Mode Differential Pair

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo[1]	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660		850	mV	1
Voltage Low	VLow		-150		150		1
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300				1
Crossing Voltage (abs)	Vcross(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Average period	Tperiod	400MHz nominal	2.4993		2.5008	ns	2
		400MHz spread	2.4993		2.5133	ns	2,3
		333.33MHz nominal	2.9991		3.0009	ns	2
		333.33MHz spread	2.9991		3.016	ns	2,3
		266.66MHz nominal	3.7489		3.7511	ns	2
		266.66MHz spread	3.7489		3.77	ns	2,3
		200MHz nominal	4.9985		5.0015	ns	2
		200MHz spread	4.9985		5.0266	ns	2,3
		166.66MHz nominal	5.9982		6.0018	ns	2
		166.66MHz spread	5.9982		6.0320	ns	2,3
		133.33MHz nominal	7.4978		7.5023	ns	2
		133.33MHz spread	7.4978		5.4000	ns	2,3
		100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2,3
Absolute min period	T_{absmin}	400MHz nominal/spread	2.4143			ns	1,2
		333.33MHz nominal/spread	2.9141			ns	1,2
		266.66MHz nominal/spread	3.6639			ns	1,2
		200MHz nominal/spread	4.8735			ns	1,2
		166.66MHz nominal/spread	5.8732			ns	1,2
		133.33MHz nominal/spread	7.3728			ns	1,2
		100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r				125	ps	1
Fall Time Variation	d-t_f				125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Skew	t_{sk3}	V_T = 50%			50	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom			50	ps	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz or 25 MHz

[3] Figures are for down spread.

TARGET SPECIFICATION SUBJECT TO CHANGE FOR PRODUCTION CHARACTERIZATION

Electrical Characteristics - REF-14.318/25 MHz

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300	0	300	ppm	1
Clock period	T_{period}	14.318MHz output nominal	69.8270	69.8413	69.8550	ns	1,2
Clock period	T_{period}	25.000MHz output nominal	39.9880	40.0000	40.0120	ns	1,2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V, V_{OH}@MAX = 3.135 V	-29		-23	mA	1
Output Low Current	I_{OL}	V_{OL} @MIN = 1.95 V, V_{OL} @MAX = 0.4 V	29		27	mA	1
Rise Time	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1	1.6	2	ns	1
Fall Time	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1	1.6	2	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V		150	200	ps	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818 or 25.00 MHz

TARGET SPECIFICATION SUBJECT TO CHANGE WITH FULL PRODUCT CHARACTERIZATION

I²C Table: Device Control Register, READ/WRITE ADDRESS (DC/DD)

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	27	FS3[1]		RW	See Frequency Selection Table, Page 1		Pin 27
Bit 6	5	FS2[1]		RW			Pin 5
Bit 5	44	FS1[1]		RW			Pin 44
Bit 4	7	FS0[1]		RW			Pin 7
Bit 3	26	Spread Enable[1]		RW	Off	On	Pin 26
Bit 2	-	Enable Software Control of Frequency, Spread Enable (Spread Type always Software Control)		RW	Hardware Select	Software Select	0
Bit 1	-	DIF_STOP# drive mode		RW	Driven	Hi-Z	0
Bit 0	-	SPREAD TYPE		RW	Down	Center	0

Notes:
1. These bits reflect the state of the corresponding pins at power up, but may be written to if Byte 0, bit 2 is set to '1'. FS3 is the SEL14M_25M# pin.

I²C Table: Output Enable Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	DIF_7	Output Control	RW	Disable	Enable	1
Bit 6	-	DIF_6	Output Control	RW	Disable	Enable	1
Bit 5	-	DIF_5	Output Control	RW	Disable	Enable	1
Bit 4	-	DIF_4	Output Control	RW	Disable	Enable	1
Bit 3	-	DIF_3	Output Control	RW	Disable	Enable	1
Bit 2	-	DIF_2	Output Control	RW	Disable	Enable	1
Bit 1	-	DIF_1	Output Control	RW	Disable	Enable	1
Bit 0	-	DIF_0	Output Control	RW	Disable	Enable	1

I²C Table: Output Stop Mode Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	DIF_7	Output Control	RW	Free-run	Stop-able	0
Bit 6	-	DIF_6	Output Control	RW	Free-run	Stop-able	0
Bit 5	-	DIF_5	Output Control	RW	Free-run	Stop-able	0
Bit 4	-	DIF_4	Output Control	RW	Free-run	Stop-able	0
Bit 3	-	DIF_3	Output Control	RW	Free-run	Stop-able	0
Bit 2	-	DIF_2	Output Control	RW	Free-run	Stop-able	0
Bit 1	-	DIF_1	Output Control	RW	Free-run	Stop-able	0
Bit 0	-	DIF_0	Output Control	RW	Free-run	Stop-able	0

I²C Table: Frequency Select Readback Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	27	SEL14M_25M#[1] (FS3)	State of pin 27	R	See Frequency Selection Table, Page 1		Pin 27
Bit 6	6	FS2[1]	State of pin 6	R			Pin 6
Bit 5	44	FS1[1]	State of pin 44	R			Pin 44
Bit 4	45	FS0[1]	State of pin 45	R			Pin 45
Bit 3	26	SPREAD[1]	State of pin 26	R	Off	On	Pin 26
Bit 2		RESERVED		R	RESERVED		X
Bit 1		RESERVED		R	RESERVED		X
Bit 0		RESERVED		R	RESERVED		X

Notes:

1. These bits reflect the state of the corresponding pins, regardless of whether software programming is enabled or not.

I²C Table: Vendor & Revision ID Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	REVISION ID	R	-	-	0
Bit 6	-	RID2		R	-	-	0
Bit 5	-	RID1		R	-	-	0
Bit 4	-	RID0		R	-	-	0
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

I²C Table: DEVICE ID

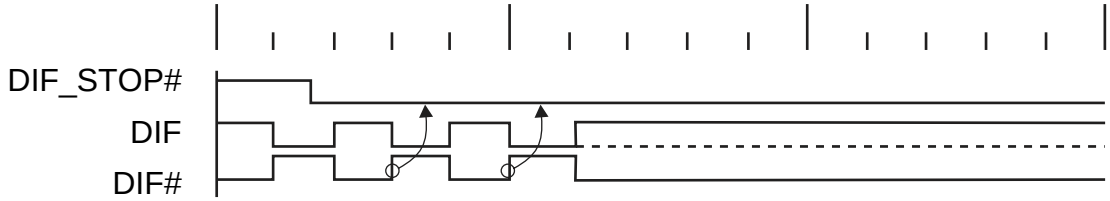
Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Device ID = 08 hex		R	RESERVED		0
Bit 6	-			R	RESERVED		0
Bit 5	-			R	RESERVED		0
Bit 4	-			R	RESERVED		0
Bit 3	-			R	RESERVED		1
Bit 2	-			R	RESERVED		0
Bit 1	-			R	RESERVED		0
Bit 0	-			R	RESERVED		0

I²C Table: Byte Count Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Writing to this register will configure how many bytes will be read back, default is 07 = 7 bytes.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	0
Bit 2	-	BC2		RW	-	-	1
Bit 1	-	BC1		RW	-	-	1
Bit 0	-	BC0		RW	-	-	1

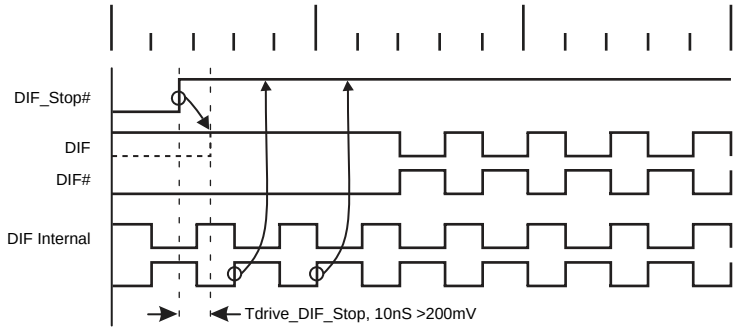
DIF_STOP# - Assertion (transition from '1' to '0')

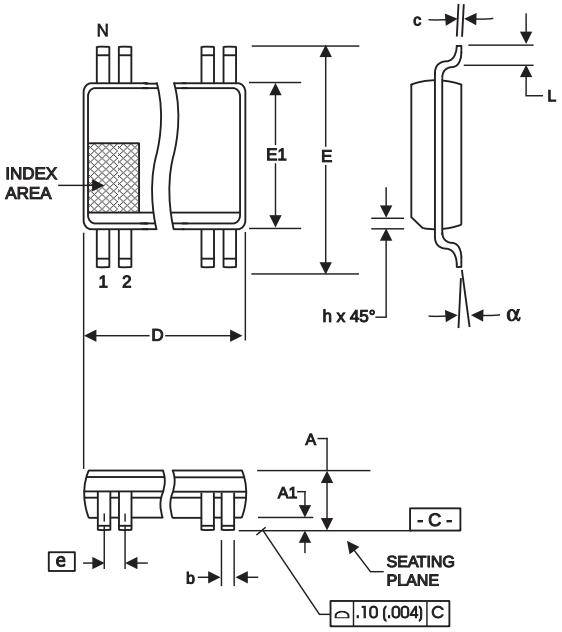
Asserting DIF_STOP# pin stops all DIF outputs that are set to be stoppable after their next transition. When the I2C DIF_STOP tri-state bit corresponding to the DIF output of interest is programmed to a '0', DIF output will stop DIF_True = HIGH and DIF_Complement = LOW. When the I2C DIF_STOP tri-state bit corresponding to the DIF output of interest is programmed to a '1', DIFoutputs will be tri-stated.



DIF_STOP# - De-assertion (transition from '0' to '1')

With the de-assertion of DIF_STOP# all stopped DIF outputs will resume without a glitch. The maximum latency from the de-assertion to active outputs is 2 - 6 DIF clock periods. If the control register tristate bit corresponding to the output of interest is programmed to '1', then the stopped DIF outputs will be driven High within 10nS of DIF_Stop# de-assertion to a voltage greater than 200mV.





SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS9FG108yFLF-T

Example:

ICS XXXX y F - LF T

Designation for tape and reel packaging
Lead Free (if required)

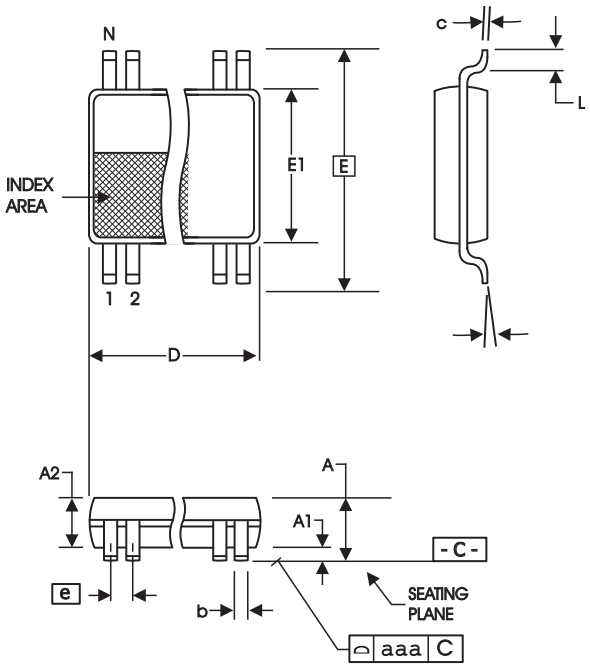
Package Type
F = SSOP

Revision Designator (will not correlate with datasheet revision)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV = Standard Device

0823—04/02/04



48-Lead, 6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

ICS9FG108yGLF-T

Example:

ICS XXXX y G - LF T

Designation for tape and reel packaging
Lead Free (if required)
Package Type
G = TSSOP
Revision Designator (will not correlate with datasheet revision)
Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS, AV = Standard Device

0823—04/02/04