## DATA SHEET



# MOS FIELD EFFECT TRANSISTOR **2SK2137**

### SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

#### DESCRIPTION

The 2SK2137 is N-Channel MOS Field Effect Transistor designed for high voltage switching applications.

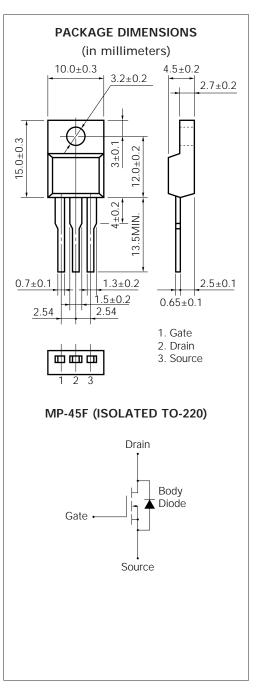
#### FEATURES

- Low On-Resistance  $2SK2137: \ R_{DS(on)} = 2.4 \ \Omega \ (V_{GS} = 10 \ V, \ I_{D} = 2.0 \ A)$
- Low Ciss Ciss = 550 pF TYP.
- High Avalanche Capability Ratings
- Isolate TO-220 Package

#### ABSOLUTE MAXIMUM RATINGS (TA = 25 °C)

Drain to Source Voltage	Vdss	600	V
Gate to Source Voltage	Vgss	±30	V
Drain Current (DC)	D(DC)	±4.0	А
Drain Current (pulse)*	D(pulse)	±16	А
Total Power Dissipation (Tc = 25 °C)	Pt1	30	W
Total Power Dissipation (T <sub>A</sub> = 25 °C)	Pt2	2.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg -5	5 to +150	°C
Single Avalanche Current**	las	4.0	А
Single Avalanche Energy**	Eas	5.3	mJ
* $PW < 10 \mu s$ Duty Cycle < 1 %			

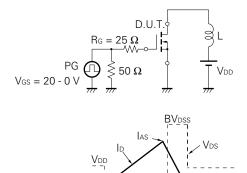
- \* PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1 %
- \*\* Starting Tch = 25 °C, RG = 25  $\Omega,$  VGs = 20 V  $\rightarrow$  0



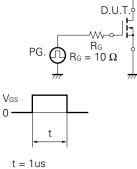
#### ELECTRICAL CHARACTERISTICS (TA = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-State Resistance	RDS(on)		1.7	2.4	Ω	$V_{GS} = 10 \text{ V}, \text{ Id} = 2.0 \text{ A}$
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	2.5		3.5	V	$V_{DS} = 10 V, I_{D} = 1 mA$
Forward Transfer Admittance	y <sub>fs</sub>	1.0			S	$V_{DS} = 10 V, I_{D} = 2.0 A$
Drain Leakage Current	IDSS			100	μΑ	Vds = Vdss, Vgs = 0
Gate to Source Leakage Current	Igss			±100	nA	$V_{GS} = \pm 30 \text{ V}, \text{ V}_{DS} = 0$
Input Capacitance	Ciss		550		pF	$V_{DS} = 10 V$
Output Capacitance	Coss		130		pF	Vgs = 0
Reverse Transfer Capacitance	Crss		25		pF	f = 1 MHz
Turn-On Delay Time	td(on)		11		ns	ID = 2.0 A
Rise Time	tr		6		ns	$V_{GS(on)} = 10 V$
Turn-Off Delay Time	td(off)		45		ns	$V_{DD} = 150 V$
Fall Time	tr		7		ns	$R_{G}=10~\Omega~R_{L}=75~\Omega$
Total Gate Charge	Q <sub>G</sub>		20		nC	$I_{D} = 4.0 A$
Gate to Source Charge	Qgs		4		nC	$V_{DD} = 480 V$
Gate to Drain Charge	Qgd		10		nC	V <sub>GS</sub> = 10 V
Body Diode Forward Voltage	VF(S-D)		1.0		V	IF = 4.0 A, VGS = 0
Reverse Recovery Time	trr		320		ns	IF = 4.0 A, VGS = 0
Reverse Recovery Charge	Qrr		1.2		μC	di/dt = 50 A/µs

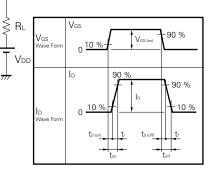
#### Test Circuit 1 Avalanche Capability



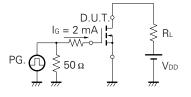




Duty Cycle ≤ 1 %

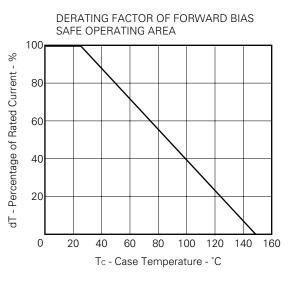


Test Circuit 3 Gate Charge



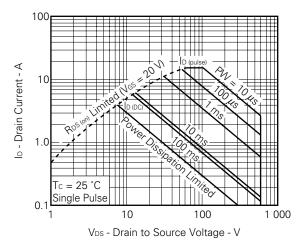
-Starting Tch

The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

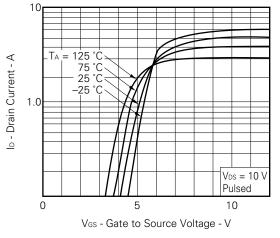


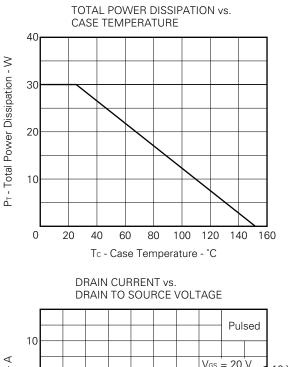


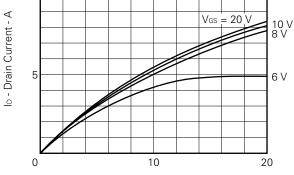




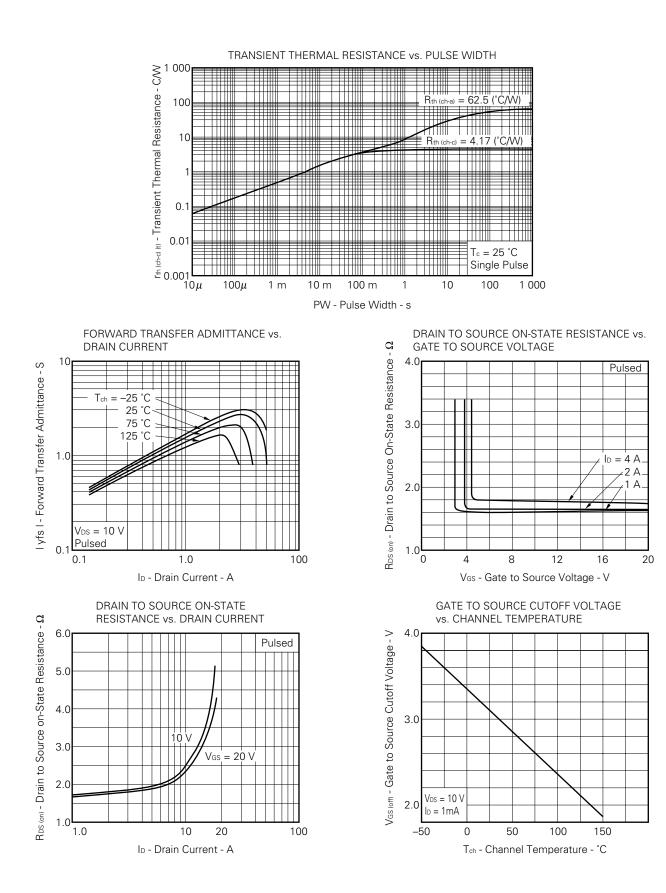


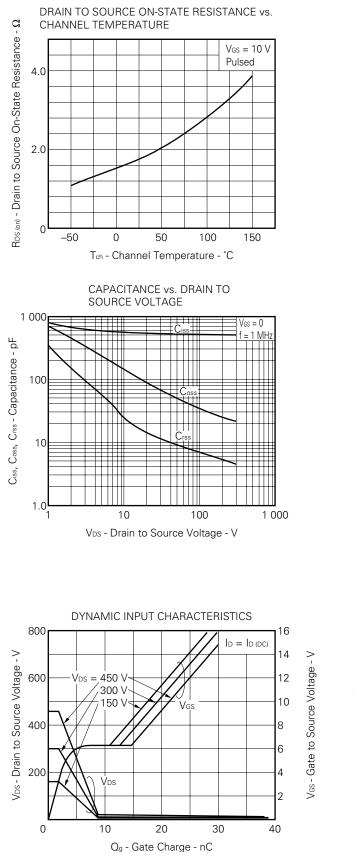


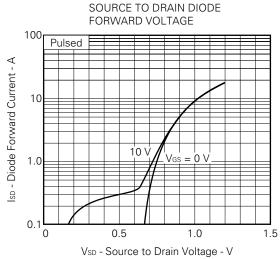




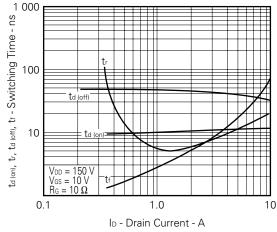


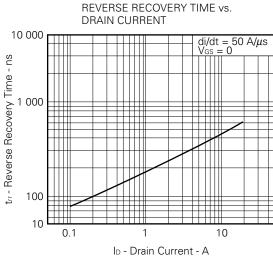


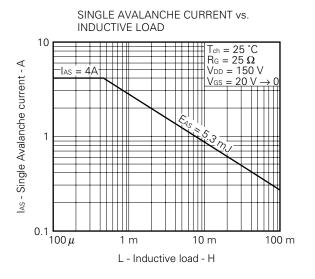


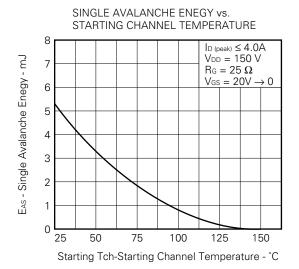












#### REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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Anti-radioactive design is not implemented in this product.