

**50A, 60V, 0.022 Ohm, N-Channel Power MOSFETs**

These N-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA49018.

**Ordering Information**

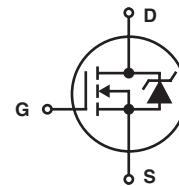
PART NUMBER	PACKAGE	BRAND
RFG50N06	TO-247	RFG50N06
RFP50N06	TO-220AB	RFP50N06
RF1S50N06SM	TO-263AB	F1S50N06

NOTE: When ordering, use the entire part number. Add the suffix, 9A, to obtain the TO-263AB variant in tape and reel, i.e. RF1S50N06SM9A.

**Features**

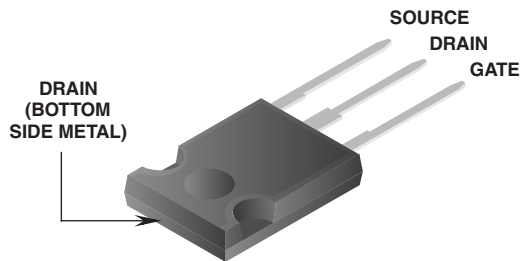
- 50A, 60V
- $r_{DS(ON)} = 0.022\Omega$
- Temperature Compensating PSPICE® Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature

**Symbol**

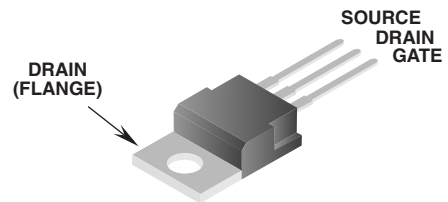


**Packaging**

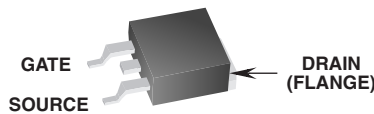
JEDEC STYLE TO-247



JEDEC TO-220AB



JEDEC TO-263AB



# RFG50N06, RFP50N06, RF1S50N06SM

## Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

	RFG50N06, RFP50N06 RF1S50N06SM	UNITS
Drain to Source Voltage (Note 1) . . . . .	60	V
Drain to Gate Voltage ( $R_{GS} = 20\text{k}\Omega$ ) (Note 1) . . . . .	60	V
Gate to Source Voltage . . . . .	$\pm 20$	V
Continuous Drain Current (Figure 2) . . . . .	50	A
Pulsed Drain Current . . . . .	(Figure 5)	
Pulsed Avalanche Rating . . . . .	(Figure 6)	
Power Dissipation . . . . .	131	W
Linear Derating Factor . . . . .	0.877	W/ $^\circ\text{C}$
Operating and Storage Temperature . . . . .	-55 to 175	$^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s . . . . .	300	$^\circ\text{C}$
Package Body for 10s, see Techbrief 334 . . . . .	260	$^\circ\text{C}$

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**NOTE:**

1.  $T_J = 25^\circ\text{C}$  to  $150^\circ\text{C}$ .

## Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$ (Figure 11)	60	-	-	V	
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$ (Figure 10)	2	-	4	V	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60\text{V}$ , $V_{GS} = 0\text{V}$	$T_C = 25^\circ\text{C}$	-	-	1	$\mu\text{A}$
			$T_C = 150^\circ\text{C}$	-	-	50	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA	
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 50\text{A}$ , $V_{GS} = 10\text{V}$ (Figures 9)	-	-	0.022	$\Omega$	
Turn-On Time	$t_{ON}$	$V_{DD} = 30\text{V}$ , $I_D = 50\text{A}$ $R_L = 0.6\Omega$ , $V_{GS} = 10\text{V}$ $R_{GS} = 3.6\Omega$ (Figure 13)	-	-	95	ns	
Turn-On Delay Time	$t_{d(ON)}$		-	12	-	ns	
Rise Time	$t_r$		-	55	-	ns	
Turn-Off Delay Time	$t_{d(OFF)}$		-	37	-	ns	
Fall Time	$t_f$		-	13	-	ns	
Turn-Off Time	$t_{OFF}$		-	-	75	ns	
Total Gate Charge	$Q_g(TOT)$	$V_{GS} = 0$ to $20\text{V}$	$V_{DD} = 48\text{V}$ , $I_D = 50\text{A}$ , $R_L = 0.96\Omega$ $I_g(REF) = 1.45\text{mA}$ (Figure 13)	-	125	150	nC
Gate Charge at 10V	$Q_g(10)$	$V_{GS} = 0$ to $10\text{V}$		-	67	80	nC
Threshold Gate Charge	$Q_g(TH)$	$V_{GS} = 0$ to $2\text{V}$		-	3.7	4.5	nC
Input Capacitance	$C_{ISS}$	$V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$ (Figure 12)	-	2020	-	pF	
Output Capacitance	$C_{OSS}$		-	600	-	pF	
Reverse Transfer Capacitance	$C_{RSS}$		-	200	-	pF	
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)	-	-	1.14	$^\circ\text{C/W}$	
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-247	-	-	30	$^\circ\text{C/W}$	
		TO-220, TO-263	-	-	62	$^\circ\text{C/W}$	

## Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	$V_{SD}$	$I_{SD} = 50\text{A}$	-	-	1.5	V
Reverse Recovery Time	$t_{rr}$	$I_{SD} = 50\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	125	ns

Typical Performance Curves Unless Otherwise Specified

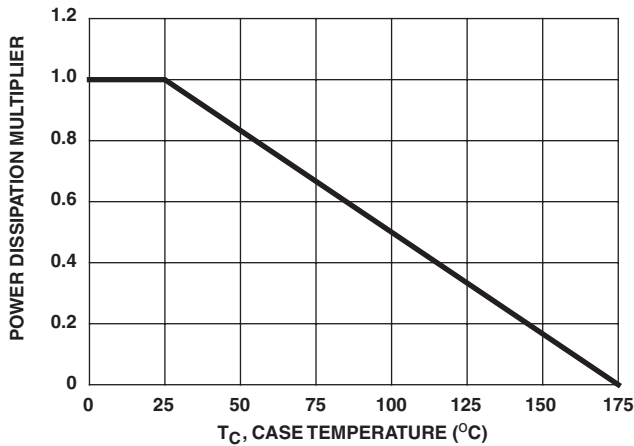


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

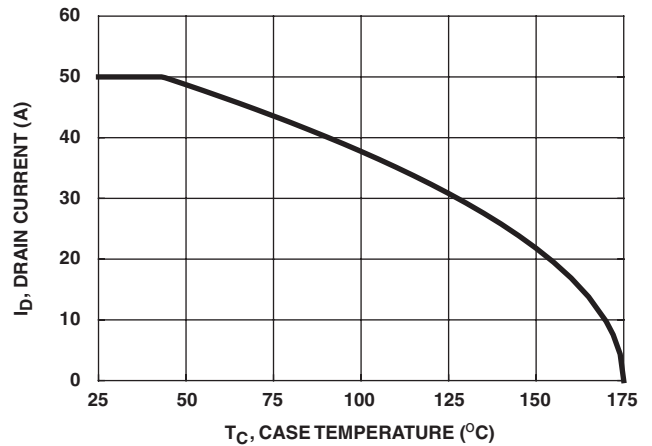


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

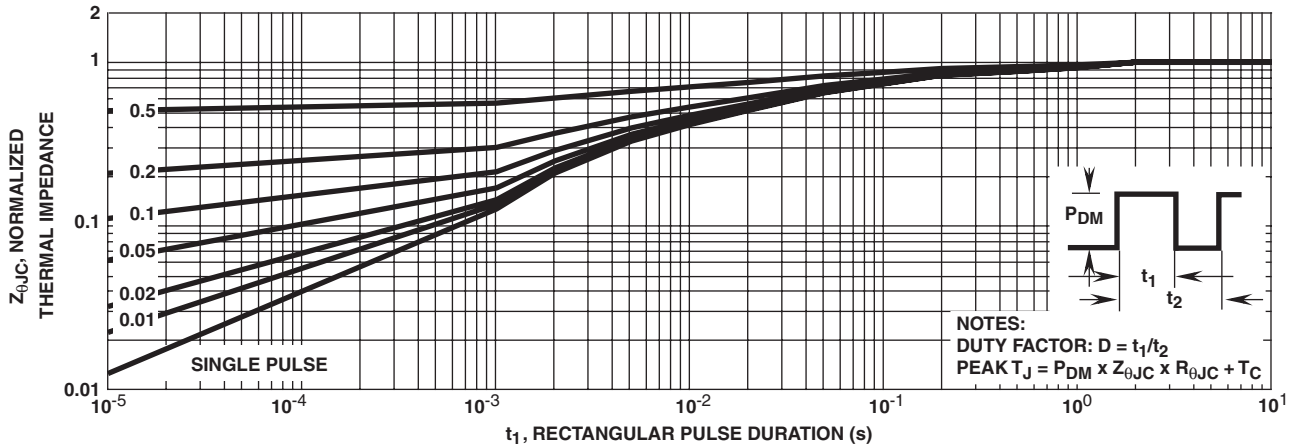


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

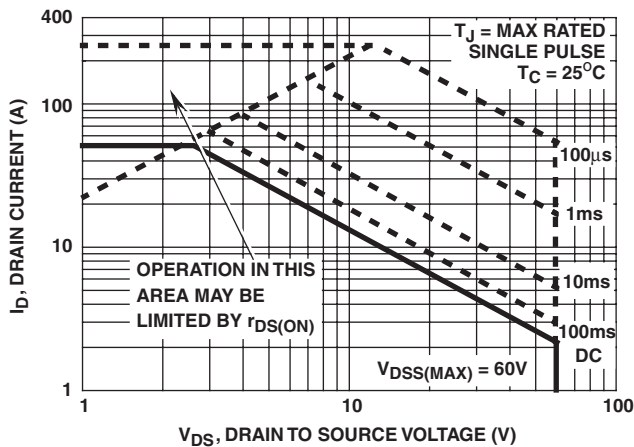


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

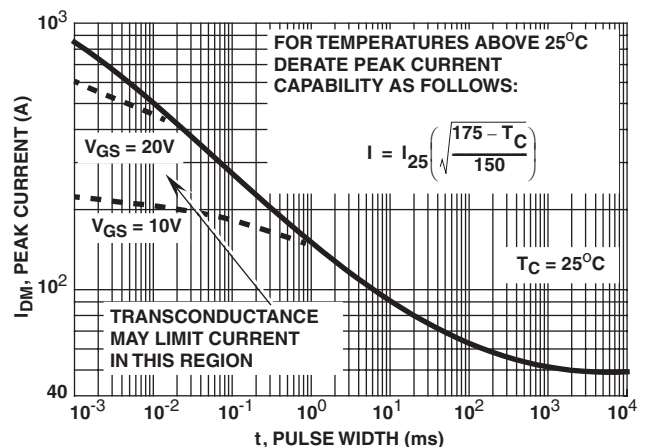
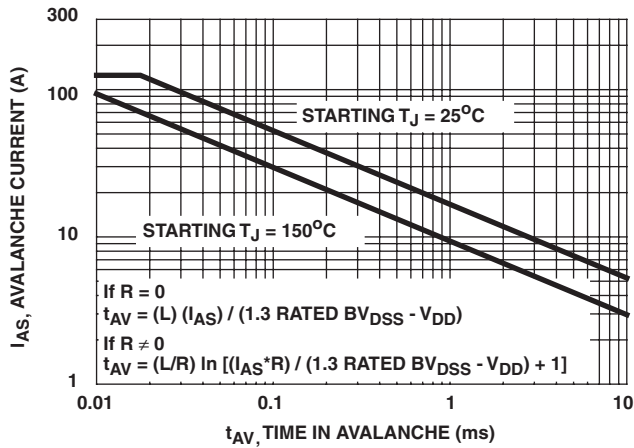


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified (Continued)



NOTE: Refer to Fairchild Application Notes 9321 and 9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

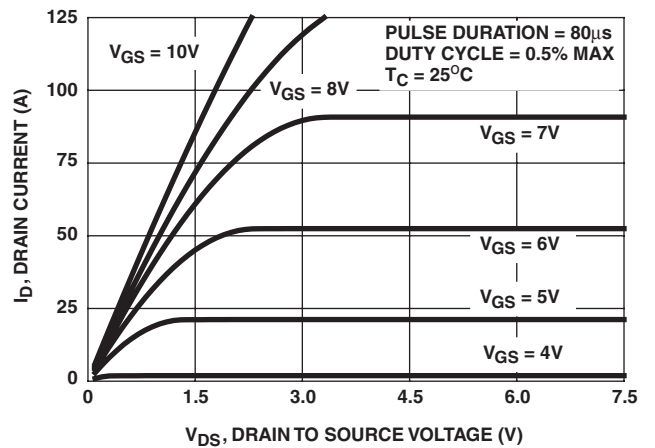


FIGURE 7. SATURATION CHARACTERISTICS

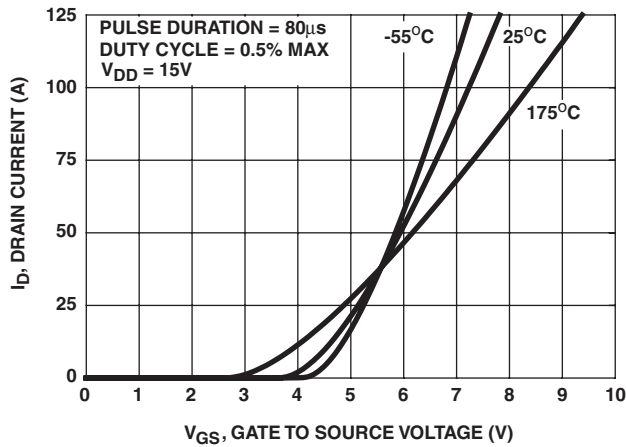


FIGURE 8. TRANSFER CHARACTERISTICS

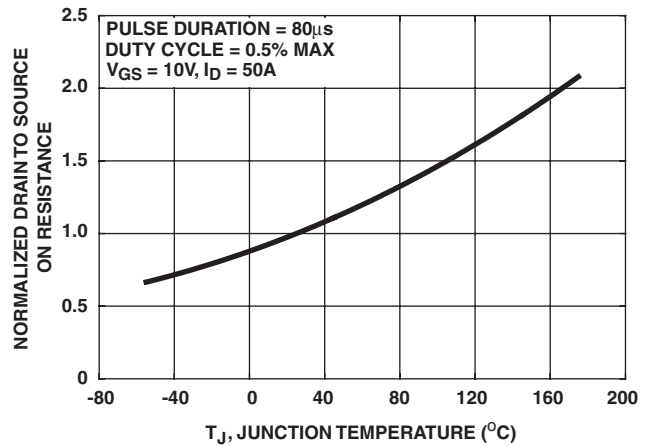


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

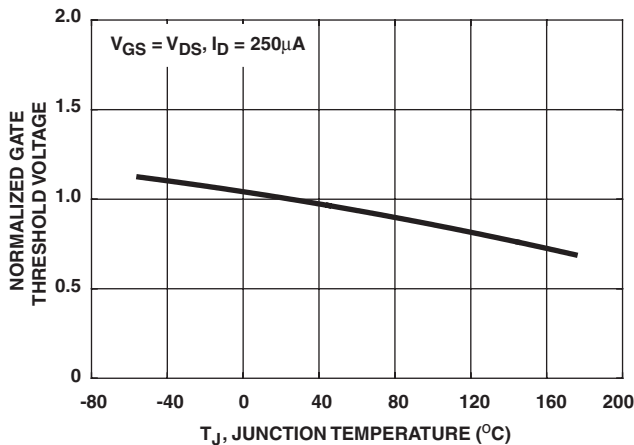


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

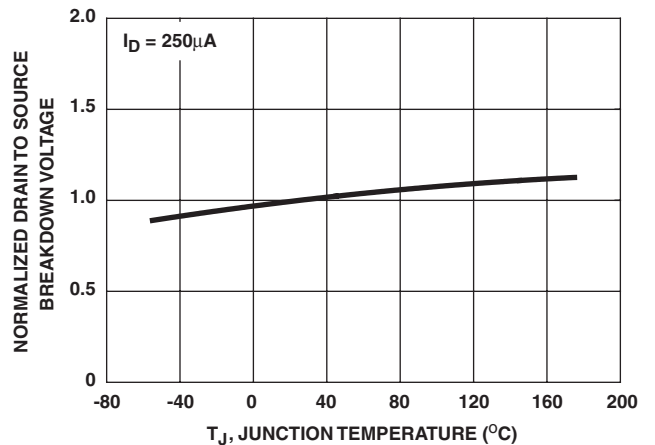


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

**Typical Performance Curves** Unless Otherwise Specified (Continued)

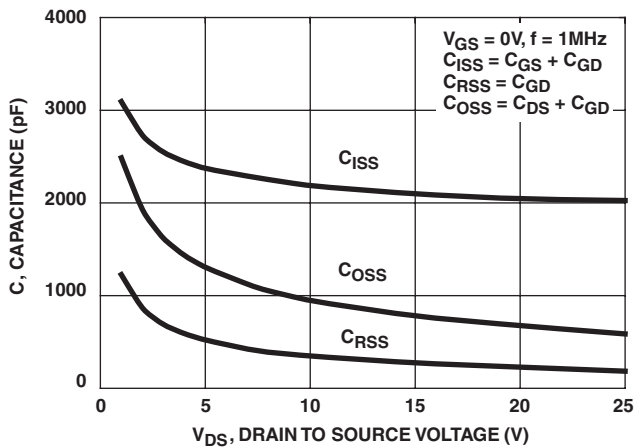
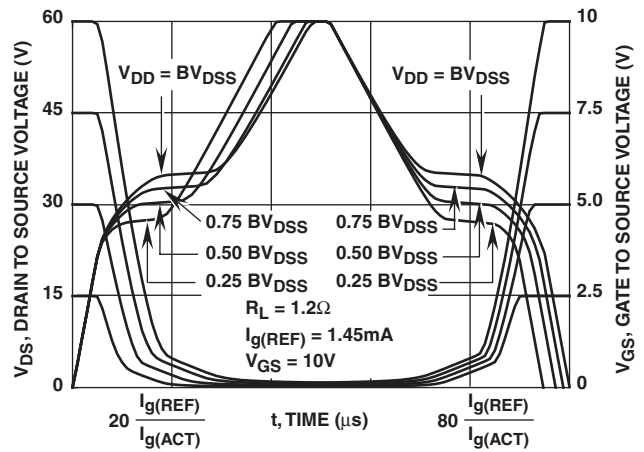


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 13. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

**Test Circuits and Waveforms**

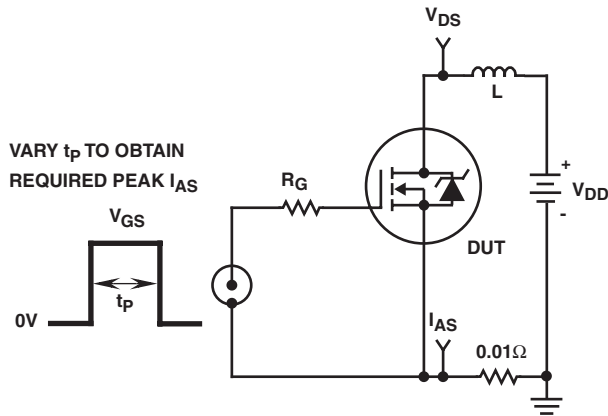


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

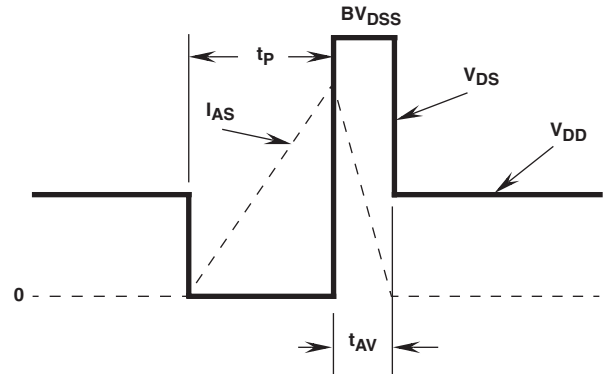


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

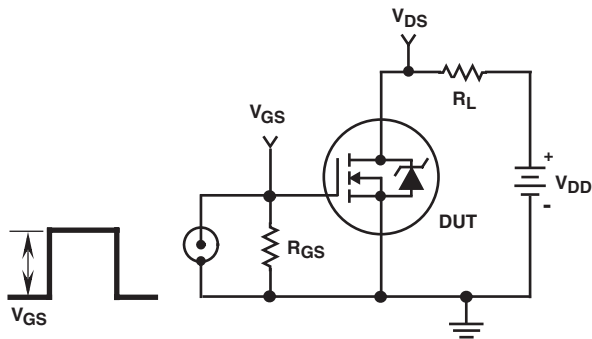


FIGURE 16. SWITCHING TIME TEST CIRCUIT

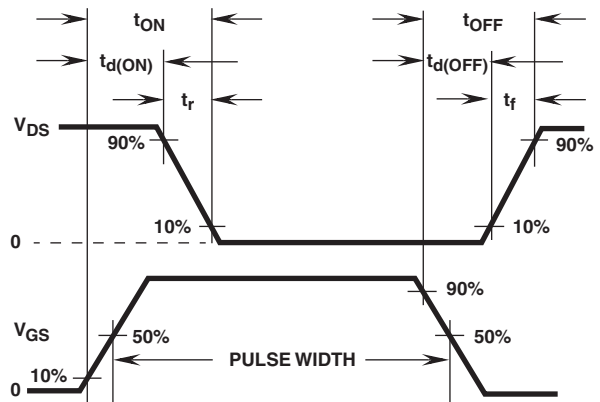


FIGURE 17. SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

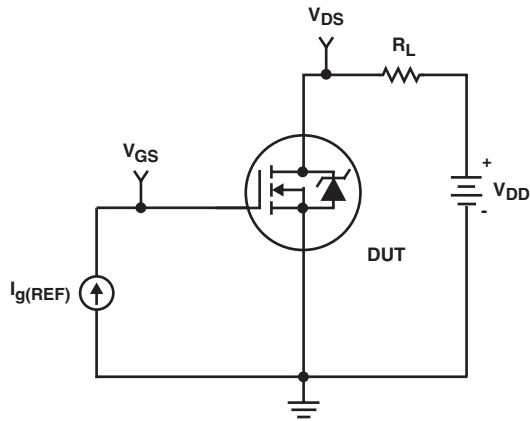


FIGURE 18. GATE CHARGE TEST CIRCUIT

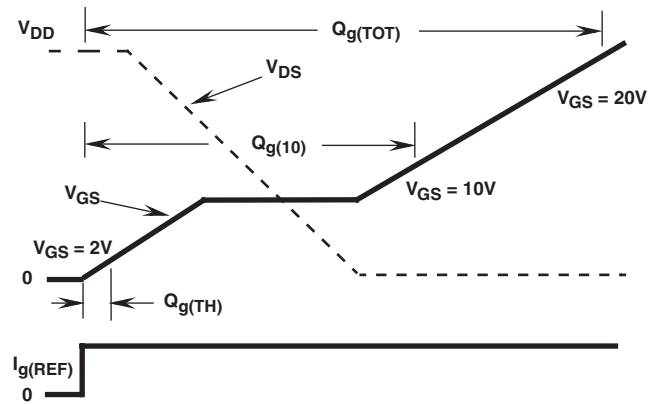


FIGURE 19. GATE CHARGE WAVEFORMS



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CROSSVOLT <sup>TM</sup>	GlobalOptoisolator <sup>TM</sup>	POPT <sup>TM</sup>	SuperSOT <sup>TM</sup> -3	
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DOME <sup>TM</sup>	HiSeC <sup>TM</sup>	PowerTrench <sup>®</sup>	SuperSOT <sup>TM</sup> -8	
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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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