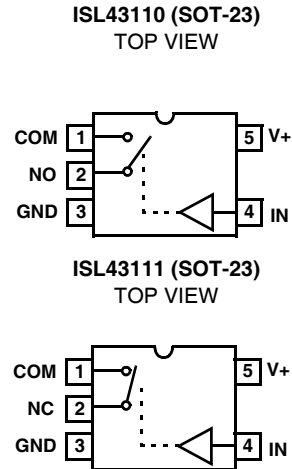
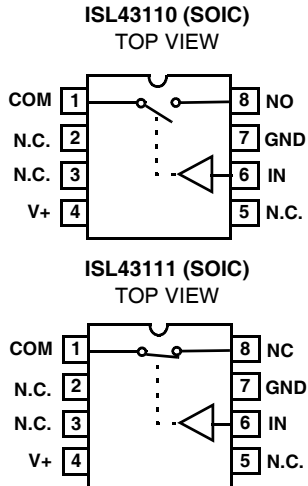


Pinouts (Note 1)



NOTE:

1. Switches Shown for Logic "0" Input.

Pin Descriptions

PIN	FUNCTION
V+	System Power Supply Input (+2.4V to +12V)
GND	Ground Connection
IN	Digital Control Input
COM	Analog Switch Common Pin
NO	Analog Switch Normally Open Pin
NC	Analog Switch Normally Closed Pin
N.C.	No Internal Connection

Truth Table

LOGIC	ISL43110	ISL43111
0	OFF	ON
1	ON	OFF

NOTE: Logic "0" ≤ 0.8V. Logic "1" ≥ 2.4V.

Absolute Maximum Ratings

V+ to GND	-0.3 to 15V
Input Voltages	
IN (Note 2)	-0.3 to ((V+) + 0.3V)
NO, NC (Note 2)	-0.3 to ((V+) + 0.3V)
Output Voltages	
COM (Note 2)	-0.3 to ((V+) + 0.3V)
Continuous Current (Any Terminal)	20mA
Peak Current NO, NC, or COM (Pulsed 1ms, 10% Duty Cycle, Max)	30mA
ESD Rating (Per MIL-STD-883 Method 3015)	>2kV

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
5 Ld SOT-23 Package	225
8 Ld SOIC Package	170
Maximum Junction Temperature (Plastic Package)	150°C
Moisture Sensitivity (See Technical Brief TB363)	
All Packages	Level 1
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) (Lead Tips Only)	300°C

Operating Conditions

Temperature Range	
ISL4311XIX	-40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

2. Signals on NO, NC, COM, or IN exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current ratings.
3. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications: 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 4), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V _{ANALOG}		Full	0	-	V+	V
ON Resistance, R _{ON}	V+ = 4.5V, I _{COM} = 1.0mA, V _{COM} = 3.5V, See Figure 4	25	-	11	20	Ω
		Full	-	15	25	Ω
R _{ON} Flatness, R _{FLAT(ON)}	I _{COM} = 1.0mA, V _{COM} = 1V, 2V, 3V	25	-	1.5	3	Ω
		Full	-	2.5	5	Ω
NO or NC OFF Leakage Current, I _{NO(OFF)} or I _{NC(OFF)}	V+ = 5.5V, V _{COM} = 1V, 4.5V, V _{NO} or V _{NC} = 4.5V, 1V, Note 6	25	-1	0.01	1	nA
		Full	-10	-	10	nA
COM OFF Leakage Current, I _{COM(OFF)}	V+ = 5.5V, V _{COM} = 4.5V, 1V, V _{NO} or V _{NC} = 1V, 4.5V, Note 6	25	-1	0.01	1	nA
		Full	-10	-	10	nA
COM ON Leakage Current, I _{COM(ON)}	V+ = 5.5V, V _{COM} = 1V, 4.5V, or V _{NO} or V _{NC} = 1V, 4.5V, Note 6	25	-1	0.01	1	nA
		Full	-20	-	20	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V _{INH}		Full	2.4	-	-	V
Input Voltage Low, V _{INL}		Full	-	-	0.8	V
Input Current, I _{INH} , I _{INL}	V+ = 5.5V, V _{IN} = 0V or V+	Full	-1	-	1	μA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t _{ON}	V _{NO} or V _{NC} = 3V, R _L = 300Ω, C _L = 35pF, V _{IN} = 0 to 3V, See Figure 1	25	-	45	80	ns
		Full	-	50	120	ns
Turn-OFF Time, t _{OFF}	V _{NO} or V _{NC} = 3V, R _L = 300Ω, C _L = 35pF, V _{IN} = 0 to 3V, See Figure 1	25	-	20	50	ns
		Full	-	28	75	ns
Charge Injection, Q	C _L = 1.0nF, V _G = 0V, R _G = 0Ω, See Figure 2	25	-	2	10	pC
OFF Isolation	R _L = 50Ω, C _L = 15pF, f = 100kHz, See Figure 3	25	-	>90	-	dB

ISL43110, ISL43111

Electrical Specifications: 5V Supply

Test Conditions: $V_+ = +4.5V$ to $+5.5V$, $GND = 0V$, $V_{INH} = 2.4V$, $V_{INL} = 0.8V$ (Note 4), Unless Otherwise Specified (Continued)

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
Power Supply Rejection Ratio	$R_L = 50\Omega$, $C_L = 5pF$, $f = 1MHz$	25	-	60	-	dB
NO or NC OFF Capacitance, C_{OFF}	$f = 1MHz$, V_{NO} or $V_{NC} = V_{COM} = 0V$, See Figure 5	25	-	15	-	pF
COM OFF Capacitance, $C_{COM(OFF)}$	$f = 1MHz$, V_{NO} or $V_{NC} = V_{COM} = 0V$, See Figure 5	25	-	15	-	pF
COM ON Capacitance, $C_{COM(ON)}$	$f = 1MHz$, V_{NO} or $V_{NC} = V_{COM} = 0V$, See Figure 5	25	-	40	-	pF
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I_+	$V_+ = 5.5V$, $V_{IN} = 0V$ or V_+ , Switch On or Off	Full	-1	-	1	μA

NOTES:

4. V_{IN} = input voltage to perform proper function.
5. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. Leakage parameter is 100% tested at high temp, and guaranteed by correlation at 25°C.

Electrical Specifications: 12V Supply

Test Conditions: $V_+ = +10.8V$ to $+13V$, $GND = 0V$, $V_{INH} = 5V$, $V_{INL} = 0.8V$ (Note 4), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V_+	V
ON Resistance, R_{ON}	$V_+ = 10.8V$, $I_{COM} = 1.0mA$, $V_{COM} = 10V$	25	-	7	10	Ω
		Full	-	8	15	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	$I_{COM} = 1.0mA$, $V_{COM} = 3V, 6V, 9V$	25	-	1	3	Ω
		Full	-	1.5	5	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	$V_+ = 13V$, $V_{COM} = 1V, 10V$, V_{NO} or $V_{NC} = 10V, 1V$, Note 6	25	-1	-	1	nA
		Full	-10	-	10	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	$V_+ = 13V$, $V_{COM} = 10V, 1V$, V_{NO} or $V_{NC} = 1V, 10V$, Note 6	25	-1	-	1	nA
		Full	-10	-	10	nA
COM ON Leakage Current, $I_{COM(ON)}$	$V_+ = 13V$, $V_{COM} = 1V, 10V$, or V_{NO} or $V_{NC} = 1V, 10V$, Note 6	25	-1	-	1	nA
		Full	-20	-	20	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}		Full	4	3	-	V
Input Voltage Low, V_{INL}		Full	-	-	0.8	V
Input Current, I_{INH} , I_{INL}	$V_+ = 13V$, $V_{IN} = 0V$ or V_+	Full	-1	-	1	μA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V_{NO} or $V_{NC} = 10V$, $R_L = 300\Omega$, $C_L = 35pF$	25	-	37	80	ns
		Full	-	42	120	ns
Turn-OFF Time, t_{OFF}	V_{NO} or $V_{NC} = 10V$, $R_L = 300\Omega$, $C_L = 35pF$	25	-	21	50	ns
		Full	-	26	75	ns
Charge Injection, Q	$C_L = 1.0nF$, $V_G = 0V$, $R_G = 0\Omega$	25	-	8	20	pC
OFF Isolation	$R_L = 50\Omega$, $C_L = 15pF$, $f = 100kHz$	25	-	>90	-	dB
Power Supply Rejection Ratio	$R_L = 50\Omega$, $C_L = 5pF$, $f = 1MHz$	25	-	67	-	dB
NO or NC OFF Capacitance, C_{OFF}	$f = 1MHz$, V_{NO} or $V_{NC} = V_{COM} = 0V$	25	-	15	-	pF

ISL43110, ISL43111

Electrical Specifications: 12V Supply

Test Conditions: $V_+ = +10.8V$ to $+13V$, $GND = 0V$, $V_{INH} = 5V$, $V_{INL} = 0.8V$ (Note 4), Unless Otherwise Specified (Continued)

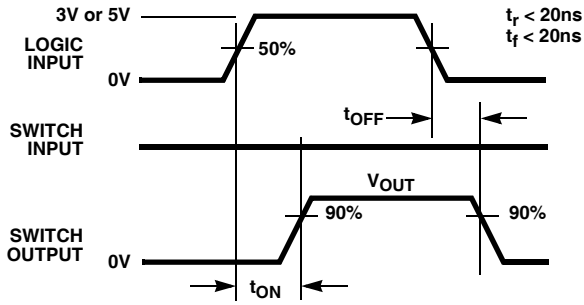
PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
COM OFF Capacitance, $C_{COM(OFF)}$	$f = 1MHz$, V_{NO} or $V_{NC} = V_{COM} = 0V$	25	-	15	-	pF
COM ON Capacitance, $C_{COM(ON)}$	$f = 1MHz$, V_{NO} or $V_{NC} = V_{COM} = 0V$	25	-	40	-	pF
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I_+	$V_+ = 13V$, $V_{IN} = 0V$ or V_+ , Switch On or Off	Full	-1	-	1	μA

Electrical Specifications: 3.3V Supply

Test Conditions: $V_+ = +3.0V$ to $+3.6V$, $GND = 0V$, $V_{INH} = 2.4V$, $V_{INL} = 0.8V$ (Note 4), Unless Otherwise Specified

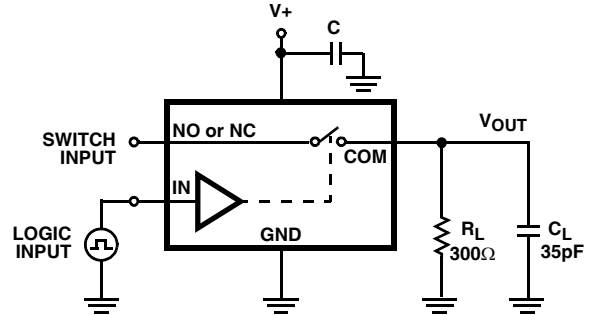
PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V_+	V
ON Resistance, R_{ON}	$V_+ = 3V$, $I_{COM} = 1.0mA$, $V_{COM} = 1.5V$	25	-	15	30	Ω
		Full	-	18	40	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	$I_{COM} = 1.0mA$, $V_{COM} = 0.5V, 1V, 1.5V$	25	-	3	5.5	Ω
		Full	-	4	7	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	$V_+ = 3.6V$, $V_{COM} = 1V, 3V$, V_{NO} or $V_{NC} = 3V, 1V$, Note 6	25	-1	-	1	nA
		Full	-10	-	10	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	$V_+ = 3.6V$, $V_{COM} = 3V, 1V$, V_{NO} or $V_{NC} = 1V, 3V$, Note 6	25	-1	-	1	nA
		Full	-10	-	10	nA
COM ON Leakage Current, $I_{COM(ON)}$	$V_+ = 3.6V$, $V_{COM} = 1V, 3V$, or V_{NO} or $V_{NC} = 1V, 3V$, or floating, Note 6	25	-1	-	1	nA
		Full	-20	-	20	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}		Full	2.4	-	-	V
Input Voltage Low, V_{INL}		Full	-	-	0.8	V
Input Current, I_{INH} , I_{INL}	$V_+ = 3.6V$, $V_{IN} = 0V$ or V_+	Full	-1	-	1	μA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V_{NO} or $V_{NC} = 1.5V$, $R_L = 300\Omega$, $C_L = 35pF$, $V_{IN} = 0$ to $3V$	25	-	55	100	ns
		Full	-	70	150	ns
Turn-OFF Time, t_{OFF}	V_{NO} or $V_{NC} = 1.5V$, $R_L = 300\Omega$, $C_L = 35pF$, $V_{IN} = 0$ to $3V$	25	-	28	60	ns
		Full	-	35	85	ns
Charge Injection, Q	$C_L = 1.0nF$, $V_G = 0V$, $R_G = 0\Omega$	25	-	2	10	pC
OFF Isolation	$R_L = 50\Omega$, $C_L = 15pF$, $f = 100kHz$	25	-	>90	-	dB
Power Supply Rejection Ratio	$R_L = 50\Omega$, $C_L = 5pF$, $f = 1MHz$	25	-	58	-	dB
NO or NC OFF Capacitance, C_{OFF}	$f = 1MHz$, V_{NO} or $V_{NC} = V_{COM} = 0V$	25	-	15	-	pF
COM OFF Capacitance, $C_{COM(OFF)}$	$f = 1MHz$, V_{NO} or $V_{NC} = V_{COM} = 0V$	25	-	15	-	pF
COM ON Capacitance, $C_{COM(ON)}$	$f = 1MHz$, V_{NO} or $V_{NC} = V_{COM} = 0V$	25	-	40	-	pF
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I_+	$V_+ = 3.6V$, $V_{IN} = 0V$ or V_+ , Switch On or Off	Full	-1	-	1	μA

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS



C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO \text{ or } NC)} \frac{R_L}{R_L + R_{(ON)}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

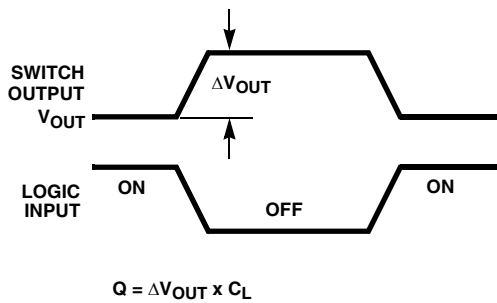


FIGURE 2A. MEASUREMENT POINTS

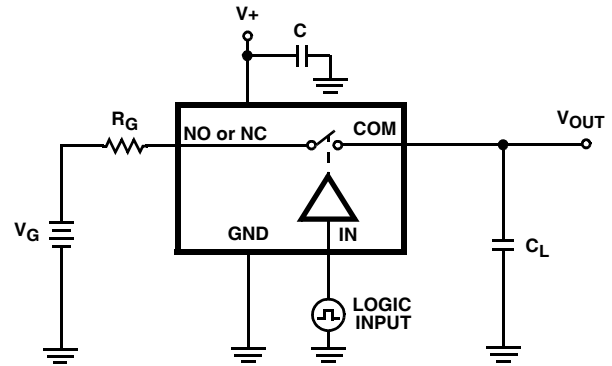


FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

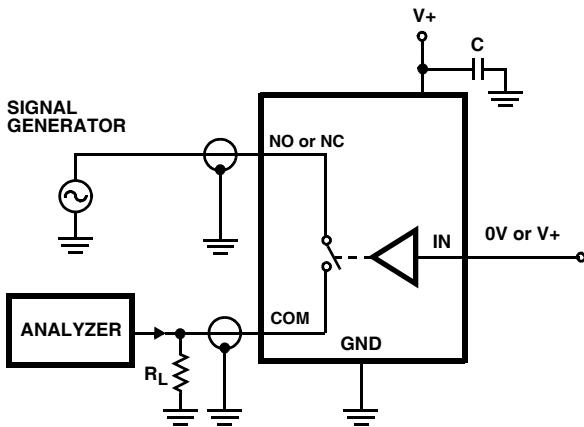


FIGURE 3. OFF ISOLATION TEST CIRCUIT

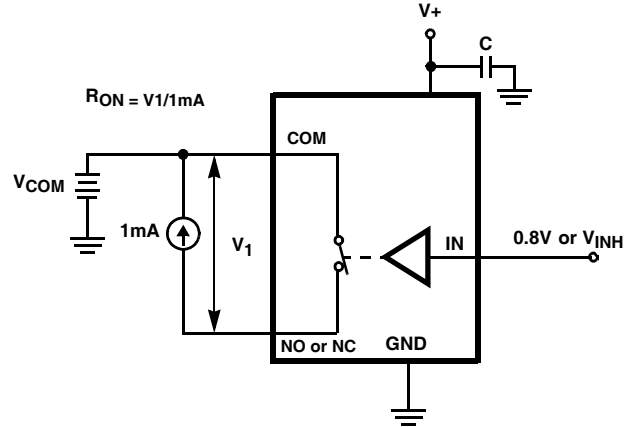


FIGURE 4. R_{ON} TEST CIRCUIT

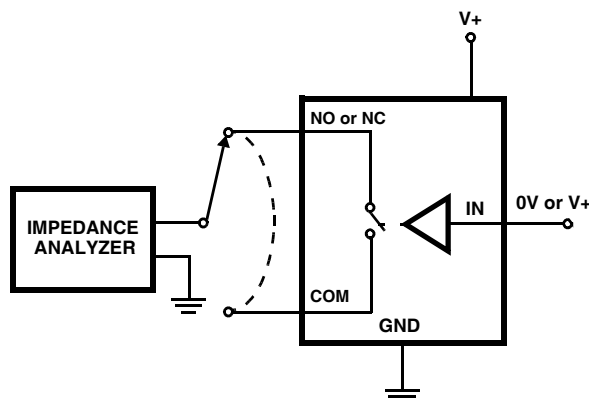
Test Circuits and Waveforms (Continued)

FIGURE 5. CAPACITANCE TEST CIRCUIT

Detailed Description

The ISL43110 and ISL43111 analog switches offer precise switching capability from a single 2.4V to 12V supply with low on-resistance and high speed operation. The devices are especially well suited to portable battery powered equipment thanks to the low operating supply voltage (2.4V), low power consumption (5 μ W), low leakage currents (1nA max), and the tiny SOT-23 packaging. High frequency applications also benefit from the wide bandwidth, and the very high off isolation.

Supply Sequencing And Overvoltage Protection

As with any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to GND (see Figure 6). To prevent forward biasing these diodes, V+ must be applied before any input signals, and input signal voltages must remain between V+ and GND. If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a 1k Ω resistor in series with the input (see Figure 6). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

Adding a series resistor to the switch input defeats the purpose of using a low R_{ON} switch, so two small signal diodes can be added in series with the supply pins to provide overvoltage protection for all pins (see Figure 6). These additional diodes limit the analog signal from 1V below V+ to 1V above GND. The low leakage current performance is

unaffected by this approach, but the switch resistance may increase, especially at low supply voltages.

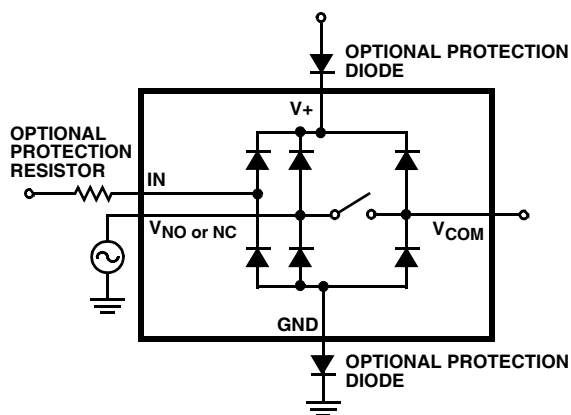


FIGURE 6. OVERVOLTAGE PROTECTION

Power-Supply Considerations

The ISL4311X construction is typical of most CMOS analog switches, except that there are only two supply pins: V+ and GND. Unlike switches with a 13V maximum supply voltage, the ISL4311X 15V maximum supply voltage provides plenty of room for the 10% tolerance of 12V supplies, as well as room for overshoot and noise spikes.

The minimum recommended supply voltage is 2.4V. It is important to note that the input signal range, switching times, and on-resistance degrade at lower supply voltages. Refer

to the electrical specification tables and *Typical Performance Curves* for details.

V+ and GND power the internal CMOS switches and set their analog voltage limits. These supplies also power the internal logic and level shifters. The level shifters convert the input logic levels to switched V+ and GND signals to drive the analog switch gate terminals.

This family of switches cannot be operated with bipolar supplies, because the input switching point becomes negative in this configuration. For a ±5V single SPST switch, see the ISL43112/13 data sheet.

Logic-Level Thresholds

This switch family is TTL compatible (0.8V and 2.4V) over a supply range of 3V to 11V, and the full temperature range (see Figure 10). At 12V the low temperature V_{IH} level is about 2.5V. This is still below the TTL guaranteed high output minimum level of 2.8V, but noise margin is reduced. For best results with a 12V supply, use a logic family that provides a V_{OH} greater than 3V.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat to 20MHz, with a -3dB bandwidth exceeding 200MHz (see Figure 15). Figure 15 also illustrates that the frequency

response is very consistent over a wide V+ range, and for varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feedthrough from a switch’s input to its output. Off Isolation is the resistance to this feedthrough. Figure 16 details the high Off Isolation provided by this family. At 10MHz, off isolation is about 50dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease Off Isolation due to the voltage divider action of the switch OFF impedance and the load impedance.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog-signal paths and V+ or GND.

Typical Performance Curves T_A = 25°C, Unless Otherwise Specified

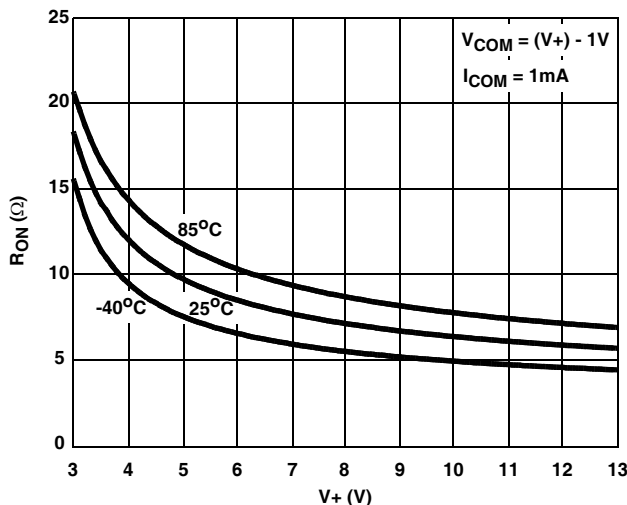


FIGURE 7. ON RESISTANCE vs SUPPLY VOLTAGE

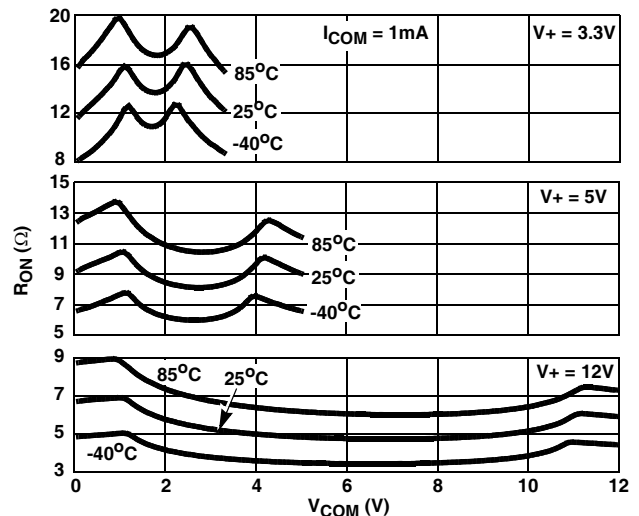


FIGURE 8. ON RESISTANCE vs SWITCH VOLTAGE

Typical Performance Curves $T_A = 25^\circ\text{C}$, Unless Otherwise Specified (Continued)

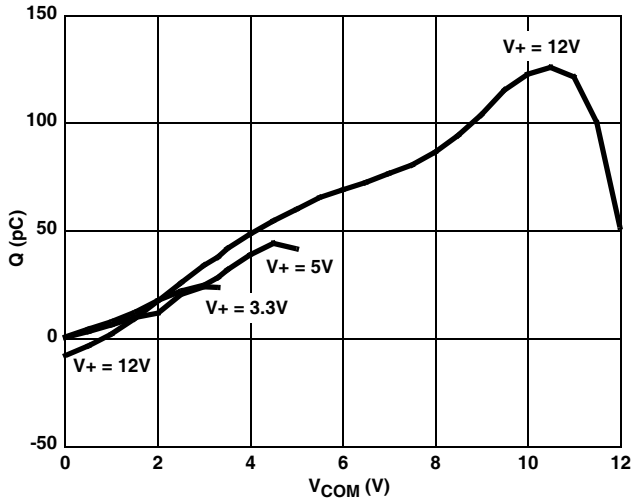


FIGURE 9. CHARGE INJECTION vs SWITCH VOLTAGE

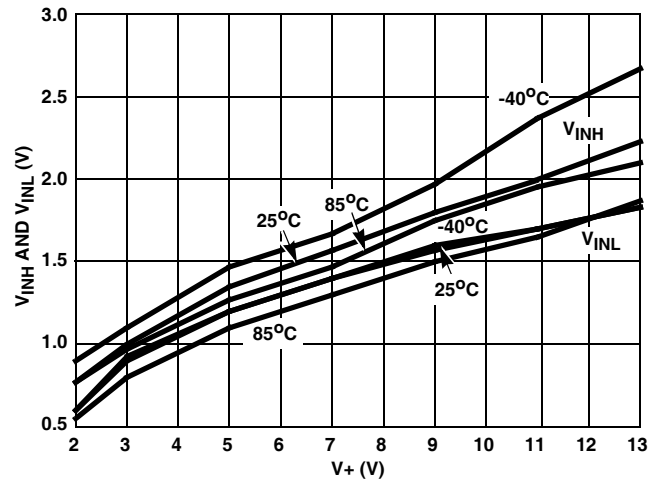


FIGURE 10. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

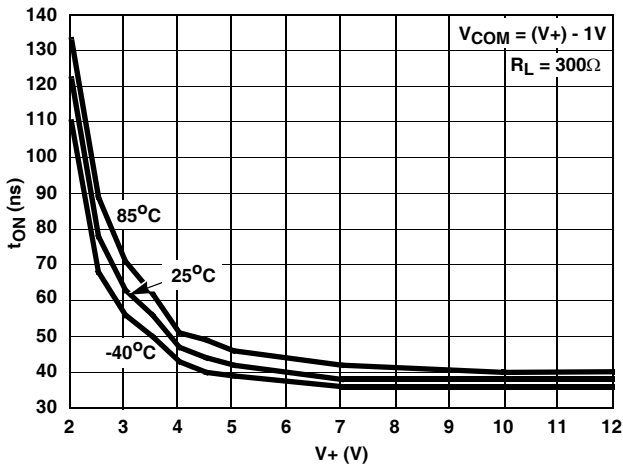


FIGURE 11. TURN - ON TIME vs SUPPLY VOLTAGE

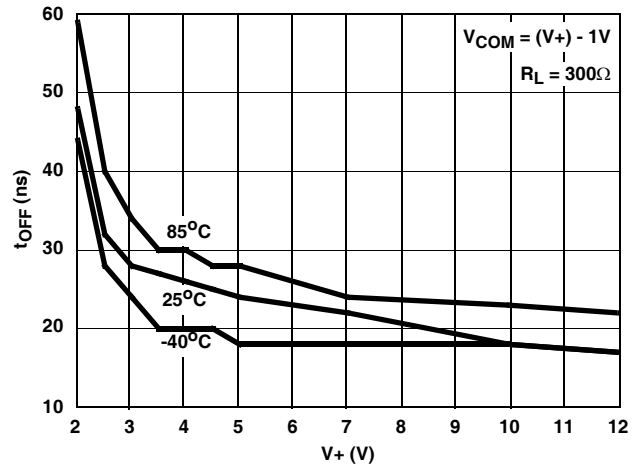


FIGURE 12. TURN - OFF TIME vs SUPPLY VOLTAGE

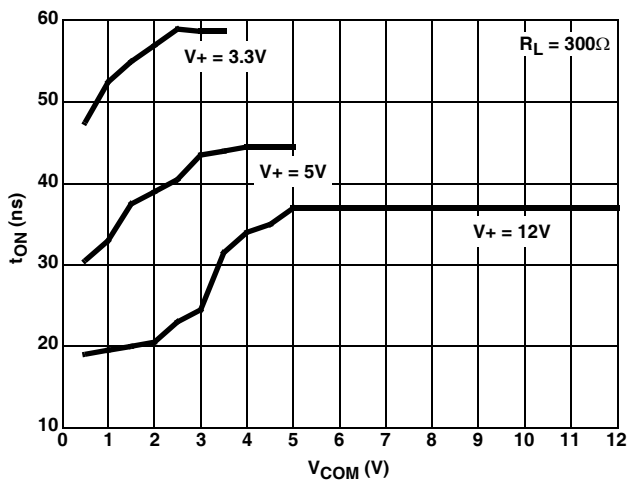


FIGURE 13. TURN - ON TIME vs SWITCH VOLTAGE

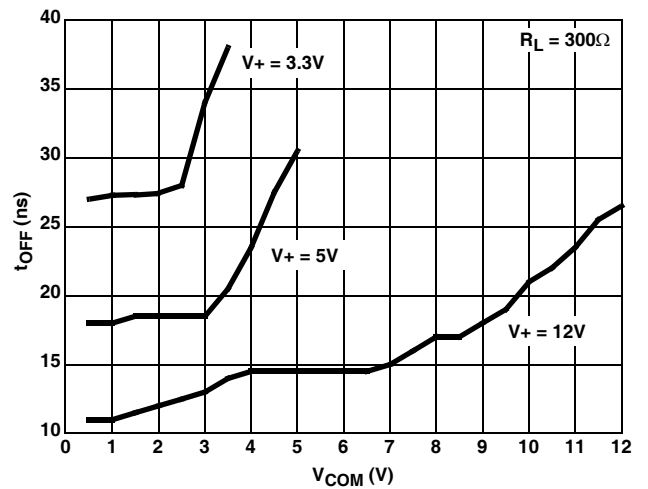


FIGURE 14. TURN - OFF TIME vs SWITCH VOLTAGE

Typical Performance Curves $T_A = 25^\circ\text{C}$, Unless Otherwise Specified (Continued)

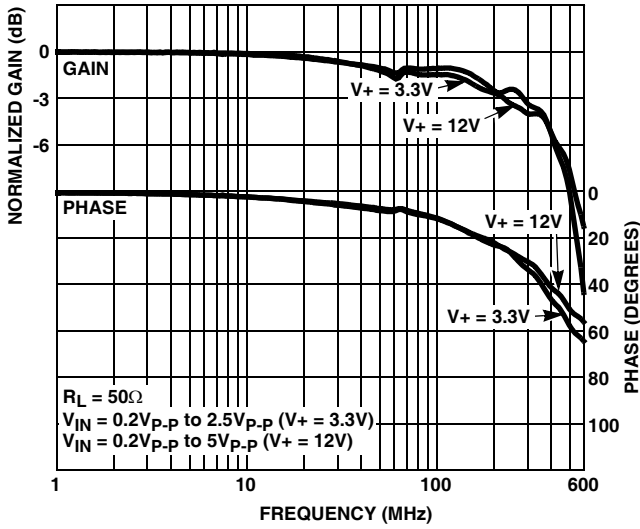


FIGURE 15. FREQUENCY RESPONSE

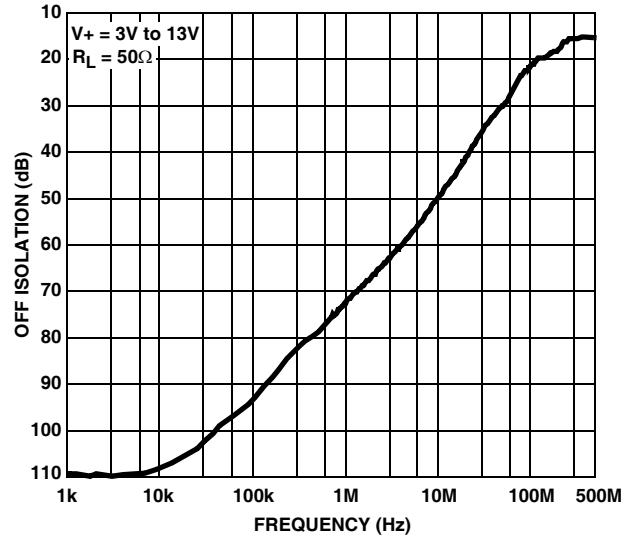


FIGURE 16. OFF ISOLATION

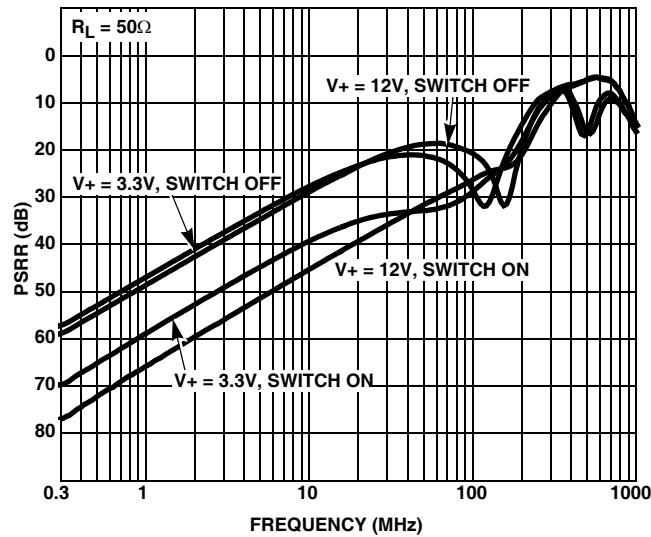


FIGURE 17. PSRR vs FREQUENCY

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

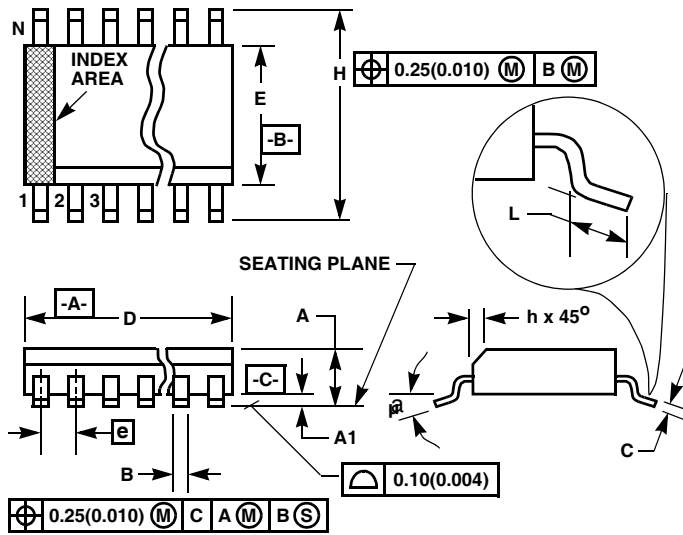
ISL43110: 40

ISL43111: 40

PROCESS:

Si Gate CMOS

Small Outline Plastic Packages (SOIC)



NOTES:

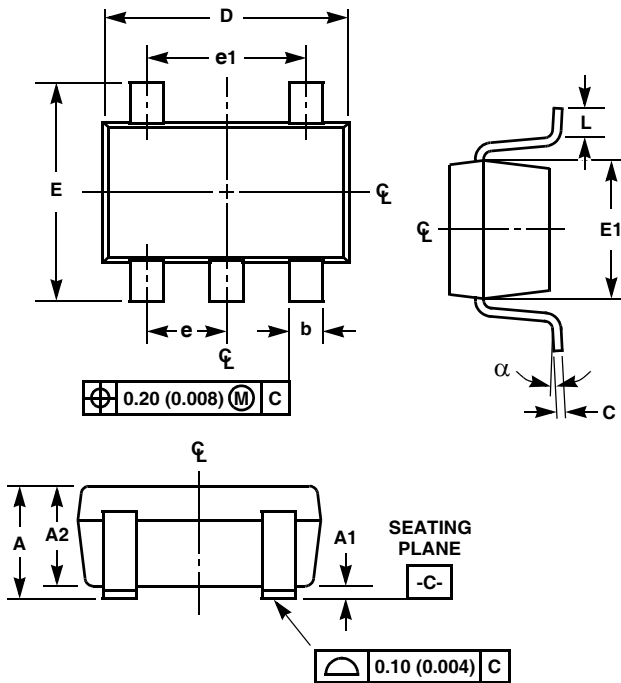
7. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
10. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
11. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
12. "L" is the length of terminal for soldering to a substrate.
13. "N" is the number of terminal positions.
14. Terminal numbers are shown for reference only.
15. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
16. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

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Small Outline Transistor Plastic Packages (SOT23-5)



P5.064

5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.036	0.057	0.90	1.45	-
A1	0.000	0.0059	0.00	0.15	-
A2	0.036	0.051	0.90	1.30	-
b	0.0138	0.0196	0.35	0.50	-
C	0.0036	0.0078	0.09	0.20	-
D	0.111	0.118	2.80	3.00	3
E	0.103	0.118	2.60	3.00	-
E1	0.060	0.068	1.50	1.75	3
e	0.0374 Ref		0.95 Ref		-
e1	0.0748 Ref		1.90 Ref		-
L	0.004	0.023	0.10	0.60	4, 5
N	5		5		6
α	0°	10°	0°	10°	-

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NOTES:

17. Dimensioning and tolerances per ANSI 14.5M-1982.
18. Package conforms to EIAJ SC-74A (1992).
19. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
20. Footlength L measured at reference to seating plane.
21. "L" is the length of flat foot surface for soldering to substrate.
22. "N" is the number of terminal positions.
23. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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