SOTINY™ Low-Voltage, Single-Supply, 1-Ohm SPST CMOS Analog Switches

Features

- 1-ohm max. On-Resistance
- 0.15-ohm max. On-Resistance Flatness at +25°C
- Fast Switching
  t_{ON} = 50ns max.
  t_{OFF} = 50ns max.
- +1.8V to +5.5V Single-Supply Operation
- TTL/CMOS-Logic Compatible
- –57dB Off-Isolation at 1MHz
- 4nA max. Off-Leakage at +25°C
- Packaging:
  - 5-Pin SOT-23 (T)

Description

PI5A4626/PI5A4629, single-pole/single-throw (SPST) analog switches that operate from a single +1.8V to +5.5V supply, are normally open (NO). The PI5A4629 pinout is optimized for the highest SOT-23 package off-isolation available.

These switches have 1-ohm max On-resistance (R_{ON}), with 0.12-ohm max R_{ON} flatness over the analog signal range when powered from a +5V supply. Leakage currents are 0.5nA and fast switching times are less than 50ns. They are packaged in a compact 5-pin SOT-23 package.

Applications

- Cellular Phones • Communications Circuits
- Battery-Operated Equipment • DSL Modems
- Audio and Video Signal Routing • PCMCIA Cards

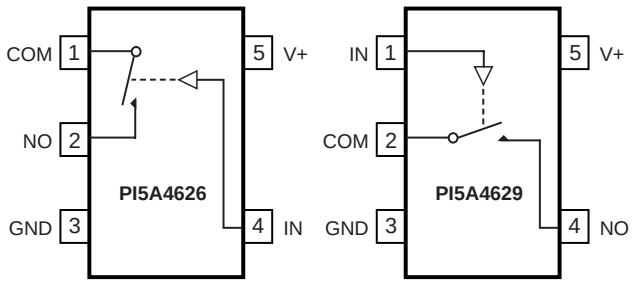
Pin Description

Pin		Name	Function
4626	4629		
1	2	COM	Analog Switch, Common
2	4	NO	Analog Switch, Normally Open
3	3	GND	Ground
4	1	IN	Digital Control Input
5	5	V+	Positive Supply Voltage

Note:
NO, NC, and COM pins are identical and interchangeable. Any pin may be considered as an input or an output; signals pass

Functional Block Diagrams/Pin Configurations

Top Views



Switches shown for Logic “0” input.

Truth Table

Input	Switch State
	PI5A4626 / PI5A4629
LOW	OFF
HIGH	ON

Absolute Maximum Ratings

Voltages Referenced to GND
V+ ..... –0.5V to +5.5V

V_{IN}, V_{COM}, V_{NC}, V_{NO} (Note 1) ..... –0.5V to V_+ +0.3V
or 30mA, whichever occurs first

Current (any terminal) ..... ±200mA

Peak Current, COM, NO, NC
(Pulsed at 1ms, 10% duty cycle) ..... ±400mA

Thermal Information

Continuous Power Dissipation

SOT-23 (derate 7.1mW/ºC above +70ºC) 0.5W

Storage Temperature ..... –65ºC to +150ºC

Lead Temperature (soldering, 10s) ..... +300ºC

Note:
1. Signals on NC, NO, COM, or IN exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to 30mA.

***Caution**: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.*

Electrical Specifications - Single +5V Supply

(V+ = +5V ± 10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Paramenter	Description	Test Conditions	Temp.(°C)	Min.(1)	Typ.(2)	Max.(1)	Units
Analog Switch							
Analog Signal Range(3)	V_{ANALOG}		Full	0		V+	V
On Resistance	R_{ON}	V+ 4.5V, I_{COM} = –30mA, V_{NO} or V_{NC} = –2.5V	25		0.5	0.9	Ohm
			Full			1.1	
On-Resistance Match Between Channels (4)	ΔR_{ON}		25		0.03	0.05	
			Full			0.10	
On-Resistance Flatness(5)	$R_{FLAT(ON)}$	V+ =5V, I_{COM} = –30mA, V_{NO} or V_{NC} =1V, –2.5V, 4V	25		0.08	0.12	
			Full			0.15	
NO or NC Off Leakage Current(6)	$I_{COM(OFF)}$ or $I_{NC(OFF)}$	V+ =5.5V, V_{COM} = 0V, V_{NO} or V_{NC} = 4.5V	25	2	0.01	2	nA
			Full	–20		20	
COM On Leakage Current(6)	$I_{COM(ON)}$	V+ =5.5V, V_{COM} = +4.5 V_{NO} or V_{NC} =+ 4.5V	25	–4		4	
			Full	–40	0.3	40	

Electrical Specifications - Single +5V Supply (continued)

(V+ = + 5V ± 10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp(°C)	Min.(1)	Typ.(2)	Max.(1)	Units
Logic Input							
Input High Voltage	V_{IH}	Guaranteed logic High Level	Full	2.4			V
Input Low Voltage	V_{IL}	Guaranteed logic Low Level				0.8	
Input Current with Voltage High	I_{INH}	V_{IN} = 2.4V, all others = 0.8V		–1	0.005	1	µA
Input Current with Voltage Low	I_{INL}	V_{IN} = 0.8V, all others = 2.4V		–1	0.005	1	
Dynamic							
Turn-On Time	t_{ON}	V+= 5V, V_{NO} or V_{NC} = 2.5V, Figure 1	25		20	35	ns
			Full			40	
Turn-Off Time	t_{OFF}		25		15	20	
			Full			35	
Charge Injection(3)	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0 Ohm, Figure 2	25		40		pC
Off Isolation	OIRR	R_L = 50 Ohms, f = 1MHz, Figure 3			–57		dB
Crosstalk(8)	X_{TALK}	R_L = 50 Ohms, f = 1MHz, Figure 4			–57		
NC or NO Capacitance	$C_{(OFF)}$	f = 1MHz, Figure 5			83		pF
COM Off Capacitance	$C_{COM(OFF)}$				83		
COM On Capacitance	$C_{COM(ON)}$	f = 1MHz, Figure 6			170		
Supply							
Power-Supply Range	V+		Full	1.8		5.5	V
Positve Supply Current	I+	V_{CC} = 5.5V, V_{IN} = 0V or V+			0.5	1	µA

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON}$ max. - R_{ON} min.
5. Flatness is defined as the difference between the maximum and minimum value of On-resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.
7. Off Isolation = $20\log_{10}$ [V_{COM} / (V_{NO} or V_{NC})]. See Figure 3.
8. Between any two switches. See Figure 4.

Electrical Specifications - Single +3.3V Supply

(V+ = +3.3V ± 10%, GND = 0V, V_{INH} = 2.0V, V_{INL} = 0.6V)

Paramenter	Description	Test Conditions	Temp.(°C)	Min.(1)	Typ.(2)	Max.(1)	Units
Analog Switch							
Analog Signal Range(3)	V_{ANALOG}			0		V+	V
On Resistance	R_{ON}	V+=3V, I_{COM} = –24mA, V_{NO} or V_{NC} = 2.0V	25		1.0	1.8	Ohm
			Full			2.2	
On-Resistance Match Between Channels (4)	ΔR_{ON}	V+=3.3V, I_{COM} = –24mA, V_{NO} or V_{NC} = 0.8V, 2.0V	25		0.04	0.5	
			Full		0.11		
On-Resistance Flatness(3,5)	$R_{FLAT(ON)}$		25		0.17	0.2	
			Full		0.25		
Dynamic							
Turn-On Time	t_{ON}	V+=3.3V, V_{NO} or V_{NC} = 2.0V, Figure 1	25		30	40	ns
			Full			55	
Turn-Off Time	t_{OFF}		25		20	25	
			Full			40	
Charge Injection(3)	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0V, Figure 2	25		30		pC
Supply							
Positive Supply Current	I+	V+=3.6V, V_{IN} = 0V or V+ All channels on or off	Full		0.5	1	µA
Logic Input							
Input HIGH Voltage	V_{IH}	Guaranteed logic high level	Full	2			V
Input LOW Voltage	V_{IL}	Guaranteed logic Low level	Full			0.6	
Input HIGH Current	I_{INH}	V_{IN} =2.4V, all others = 0.8V	Full	–1		1	µA
Input HIGH Current	I_{INL}	V_{IN} =0.8V, all others =2.4V	Full	–1		1	

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON}$ max. - R_{ON} min.
5. Flatness is defined as the difference between the maximum and minimum value of On-resistance measured.

Electrical Specifications - Single +2.5V Supply

(V+ = +2.5V ± 10%, GND = 0V, V_{INH} = 1.8V, V_{INL} = 0.6V)

Paramenter	Description	Test Conditions	Temp.(°C)	Min.(1)	Typ.(2)	Max.(1)	Units
Analog Switch							
Analog Signal Range(3)	V_{ANALOG}			0		V+	V
On Resistance	R_{ON}	V+=2.5V, I_{COM} = –8mA, V_{NO} or V_{NC} = 1.8V	25		1.5	2	Ohm
			Full			2.7	
On-Resistance Match Between Channels (4)	ΔR_{ON}	V+=2.5V, I_{COM} = –8mA, V_{NO} or V_{NC} = 0.8V,1.8V	25		0.13	0.16	
			Full		0.2		
On-Resistance Flatness(3,5)	$R_{FLAT(ON)}$		25		0.25	0.3	
			Full		0.45		
Dynamic							
Turn-On Time	t_{ON}	V+=2.5V, V_{NO} or V_{NC} = 1.8V, Figure 1	25		40	55	ns
			Full			70	
Turn-Off Time	t_{OFF}		25		30	40	
			Full			55	
Charge Injection(3)	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0V, Figure 2	25		20		pC
Supply							
Positive Supply Current	I+	V+=2.75V, V_{IN} = 0V or V+ All channels on or off	Full		0.5	1	µA
Logic Input							
Input HIGH Voltage	V_{IH}	Guaranteed logic high level	Full	1.8			V
Input LOW Voltage	V_{IL}	Guaranteed logic Low level	Full			0.6	
Input HIGH Current	I_{INH}	V_{IN} =2.0V, all others = 0.8V	Full	–1		1	µA
Input HIGH Current	I_{INL}	V_{IN} =0.8V, all others =2.0V	Full	–1		1	

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON}$ max. - R_{ON} min.
5. Flatness is defined as the difference between the maximum and minimum value of On-resistance measured.

Electrical Specifications - Single +1.8V Supply

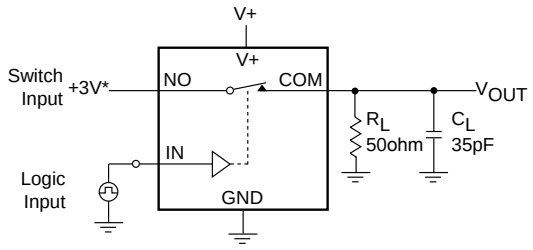
(V+ = +1.8V ± 10%, GND = 0V, V_{INH} = 1.5V, V_{INL} = 0.6V)

Paramenter	Description	Test Conditions	Temp.(°C)	Min.(1)	Typ.(2)	Max.(1)	Units
Analog Switch							
Analog Signal Range(3)	V_{ANALOG}			0		V+	V
On Resistance	R_{ON}	V+=1.8V, I_{COM} = –2mA, V_{NO} or V_{NC} = 1.5V	25		2.0	4	Ohm
			Full			5	
On-Resistance Match Between Channels (4)	ΔR_{ON}	V+=1.8V, I_{COM} = –2mA, V_{NO} or V_{NC} = 0.6V,1.5V	25		0.44	0.6	
			Full		0.7		
On-Resistance Flatness(3,5)	$R_{FLAT(ON)}$		25		0.5	0.6	
			Full		0.9		
Dynamic							
Turn-On Time	t_{ON}	V+=1.8V, V_{NO} or V_{NC} = 1.5V, Figure 1	25		65	70	ns
			Full			95	
Turn-Off Time	t_{OFF}		25		40	55	
			Full			70	
Charge Injection(3)	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0V, Figure 2	25		10		pC
Supply							
Positive Supply Current	I+	V+=2.0V, V_{IN} = 0V or V+ All channels on or off	Full		0.5	1	µA
Logic Input							
Input HIGH Voltage	V_{IH}	Guaranteed logic high level	Full	1.5			V
Input LOW Voltage	V_{IL}	Guaranteed logic Low level	Full			0.6	
Input HIGH Current	I_{INH}	V_{IN} =1.5V, all others = 0.8V	Full	–1		1	µA
Input HIGH Current	I_{INL}	V_{IN} =0.8V, all others =1.5V	Full	–1		1	

Notes:

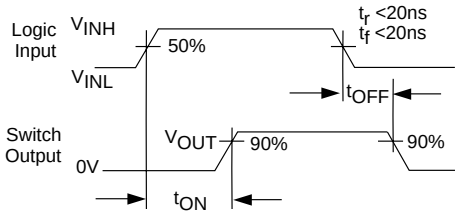
1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON}$ max. - R_{ON} min.
5. Flatness is defined as the difference between the maximum and minimum value of On-resistance measured.

Test Circuits/Timing Diagrams



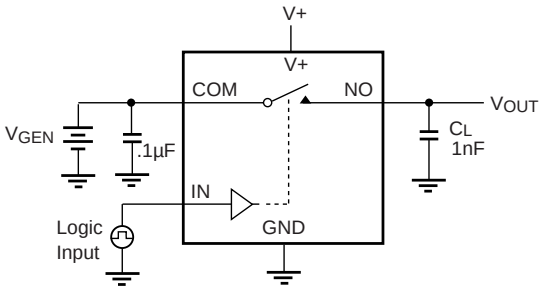
C_L INCLUDES FIXTURE AND STRAY CAPACITANCE

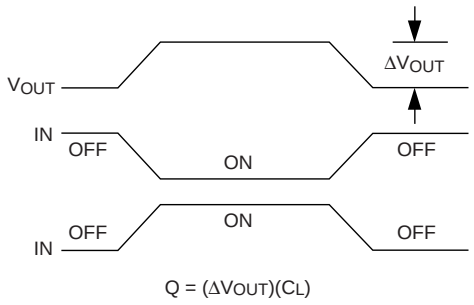
$$V_{OUT} = V_{NO}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



LOGIC INPUT WAVEFORMS INVERTED FOR SWITCHES THAT HAVE OPPOSITE LOGIC
* 1.5V FOR 3.3V SUPPLY

Figure 1. Switching Time





Q = (ΔVOUT)(CL)

Figure 2. Charge Injection

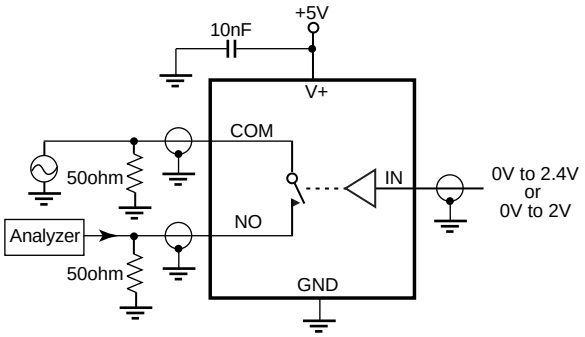


Figure 3. Off Isolation/On-Channel Bandwidth

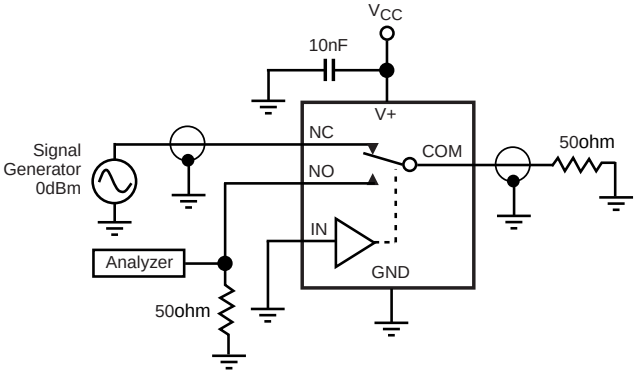


Figure 4. Crosstalk

Test Circuits/Timing Diagrams (continued)

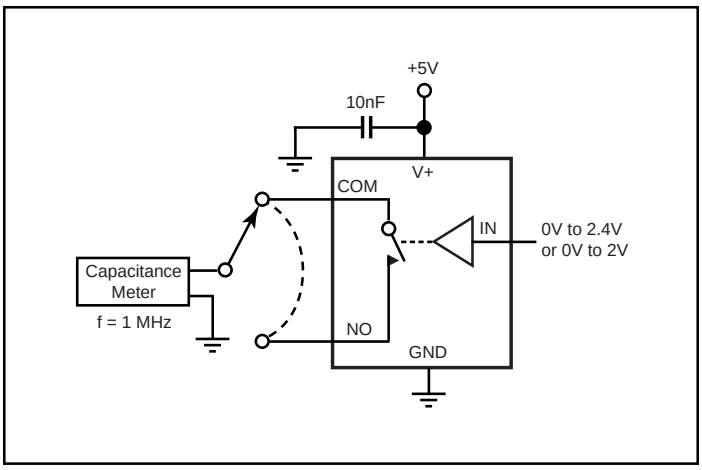


Figure 5. Channel On/Off Capacitance

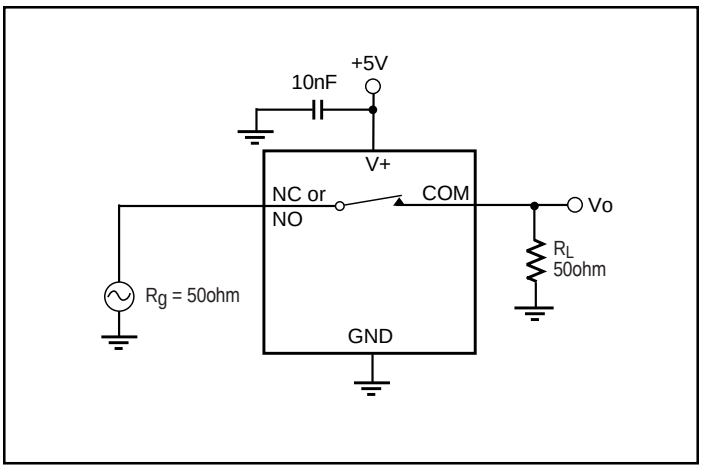
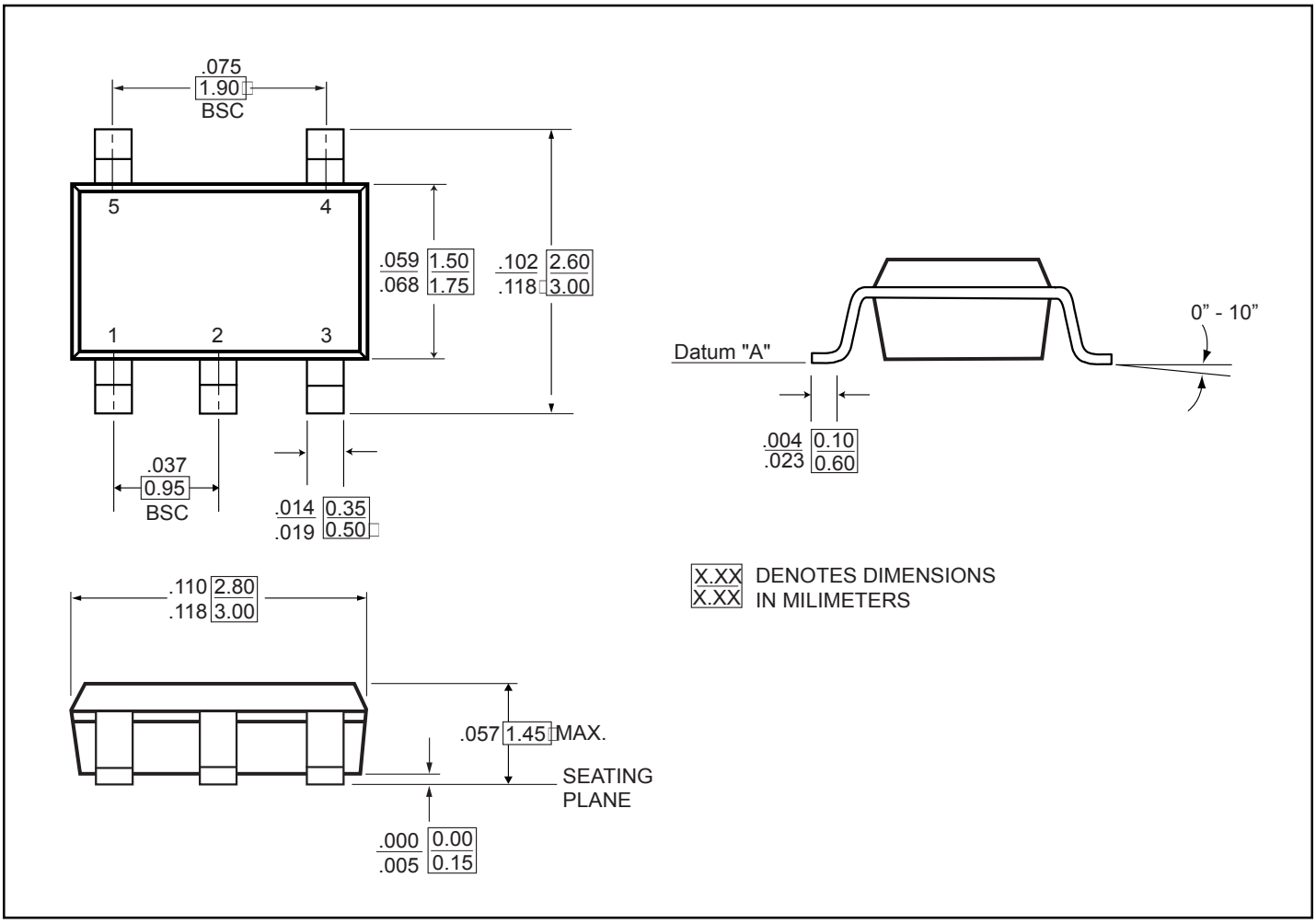


Figure 6. Bandwidth

Packaging Mechanical: 5-Pin SOT-23 (T)



Ordering Information

Ordering Code	Package Code	Package Description	Top Marking
PI5A4626TX	T	5-pin SOT-23	ZI
PI5A4629TX	T	5-pin SOT-23	ZH

Notes:
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. X = Tape and reel
3. Number of transistors: 604 (both devices)