

MC74HCT541A

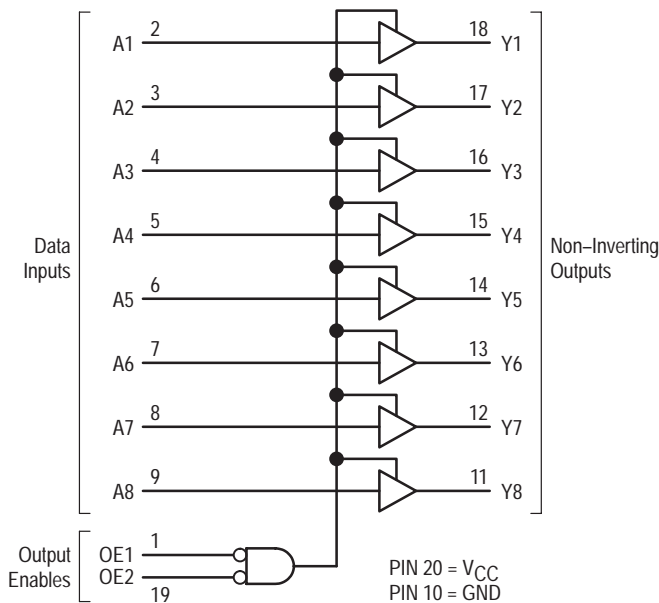
Octal 3-State Non-Inverting Buffer/Line Driver/ Line Receiver With LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS

The MC74HCT541A is identical in pinout to the LS541. This device may be used as a level converter for interfacing TTL or NMOS outputs to high speed CMOS inputs.

The HCT541A is an octal non-inverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. This device features inputs and outputs on opposite sides of the package and two ANDed active-low output enables.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5V
- Low Input Current: 1µA
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 134 FETs or 33.5 Equivalent Gates

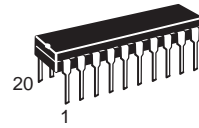
LOGIC DIAGRAM



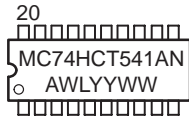
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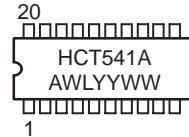
MARKING DIAGRAMS



PDIP-20
N SUFFIX
CASE 738



SOIC WIDE-20
DW SUFFIX
CASE 751D



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

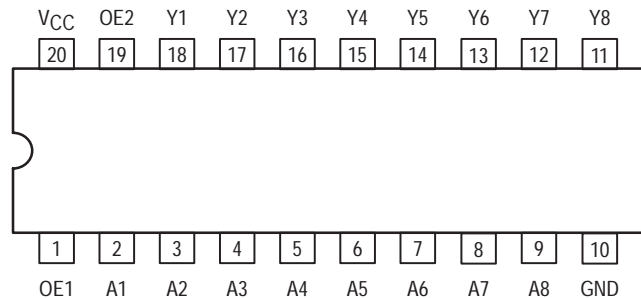
Device	Package	Shipping
MC74HCT541AN	PDIP-20	1440 / Box
MC74HCT541ADW	SOIC-WIDE	38 / Rail
MC74HCT541ADWR2	SOIC-WIDE	1000 / Reel

FUNCTION TABLE

Inputs			Output Y
OE1	OE2	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Z = High Impedance
X = Don't Care

Pinout: 20-Lead Packages (Top View)



MC74HCT541A

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Current, per Pin	± 35	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 75	mA
P _D	Power Dissipation in Still Air Plastic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature Range	- 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP or SOIC Package	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature Range, All Package Types	- 55	+ 125	°C
t _r , t _f	Input Rise/Fall Time (Figure 1)	0	500	ns

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V _{CC} V	Guaranteed Limit			Unit
				-55 to 25°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1V or V _{CC} - 0.1V I _{out} ≤ 20μA	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1V or V _{CC} - 0.1V I _{out} ≤ 20μA	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20μA	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20μA	4.5	0.1	0.1	0.1	V
			5.5	0.1	0.1	0.1	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6.0mA	4.5	3.98	3.84	3.70	μA
			5.5	0.26	0.33	0.40	
I _{OZ}	Maximum Three-State Leakage Current	Output in High Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	5.5	±0.5	±5.0	±10.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0μA	5.5	4	40	160	μA
ΔI _{CC}	Additional Quiescent Supply Current	V _{in} = 2.4V, Any One Input V _{in} = V _{CC} or GND, Other Inputs I _{out} = 0μA	5.5	≥ -55°C	25 to 125°C		mA
				2.9	2.4		

- Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).
- Total Supply Current = I_{CC} + ΣΔI_{CC}.

MC74HCT541A

AC CHARACTERISTICS ($V_{CC} = 5.0V$, $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	Guaranteed Limit			Unit
		-55 to 25°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	23	28	32	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	30	34	38	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	30	34	38	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High Impedance State)	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

C_{PD}	Power Dissipation Capacitance (Per Buffer)*	Typical @ 25°C, $V_{CC} = 5.0$ V		pF
		55		

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

SWITCHING WAVEFORMS

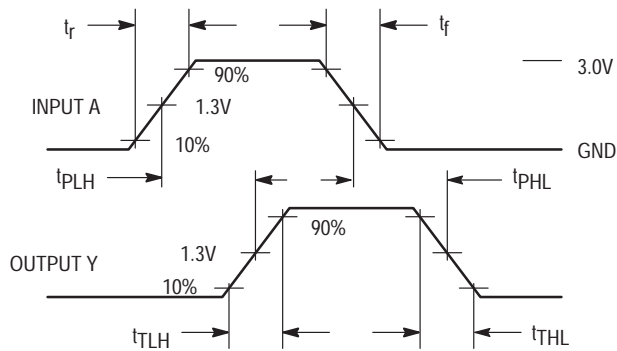


Figure 1.

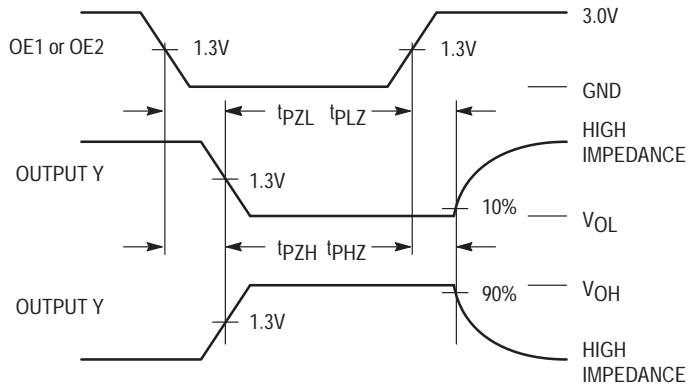
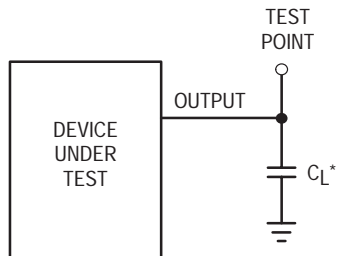


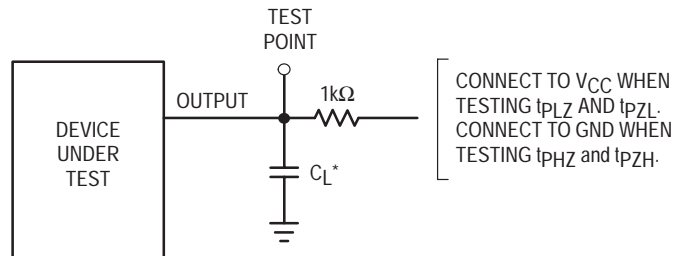
Figure 2.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 3.



*Includes all probe and jig capacitance

Figure 4.

MC74HCT541A

PIN DESCRIPTIONS

INPUTS

A1, A2, A3, A4, A5, A6, A7, A8 (PINS 2, 3, 4, 5, 6, 7, 8, 9) — Data input pins. Data on these pins appear in non-inverted form on the corresponding Y outputs, when the outputs are enabled.

CONTROLS

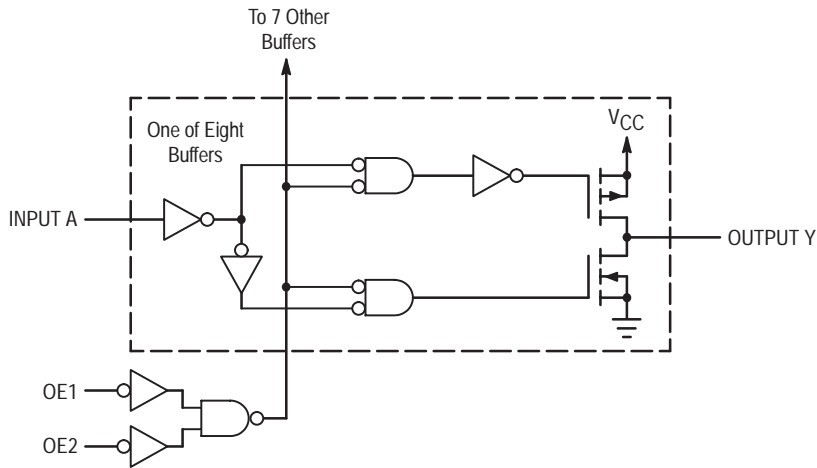
OE1, OE2 (PINS 1, 19) — Output enables (active-low). When a low voltage is applied to both of these pins, the

outputs are enabled and the device functions as a non-inverting buffer. When a high voltage is applied to either input, the outputs assume the high impedance state.

OUTPUTS

Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8 (PINS 18, 17, 16, 15, 14, 13, 12, 11) — Device outputs. Depending upon the state of the output enable pins, these outputs are either non-inverting outputs or high-impedance outputs.

LOGIC DETAIL



Notes

Notes

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