Data Sheet June 1999 File Number 4237.4

400MHz Quadrature Modulator and AGC

The HFA3763 is a highly integrated baseband converter for quadrature modulation applications. The HFA3763 400MHz quadrature modulator and AGC is one of the seven chips in the PRISM® full duplex chip set (see Typical Application Diagram). It features all the necessary blocks for baseband modulation of I and Q signals. An output AGC and Baseband shaping filters are integrated in the design. Four filter bandwidths are programmable via a two bit digital control interface. In addition, these filters are continuously tunable over a ±20% frequency range via one external resistor. The modulator channel receives digital or analog I and Q data for processing. To achieve broadband operation, the Local Oscillator frequency input is required to be twice the desired frequency of modulation. A selectable buffered divide by 2 LO output and a stable reference voltage are provided for convenience of the user.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HFA3763IN	-40 to 85	80 Ld TQFP	Q80.14x14

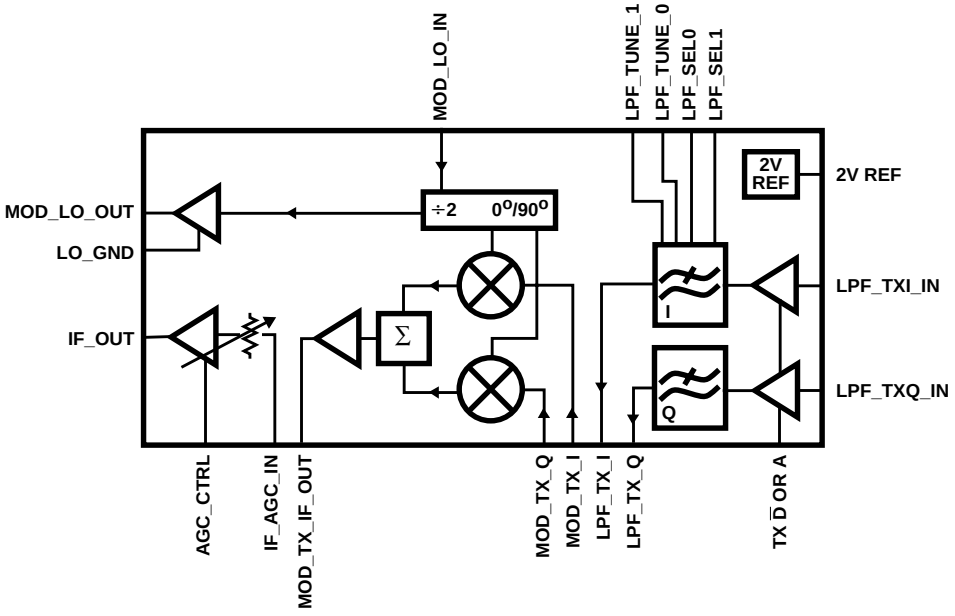
Features

- Integrates all IF Transmit Functions
- Broad Frequency Range . . . . . 10MHz to 400MHz
- I/Q Amplitude and Phase Balance . . . . . 0.2dB, 2^{o}
- 5th Order Programmable Low Pass Filter. . . . . 2.2MHz - 17.6MHz
- 400MHz Output AGC Amplifier/Attenuator 45dB
- Selectable Digital or Analog TX Baseband Inputs
- Low LO Drive Level . . . . . -15dBm
- Fast Transmit-on Switching 1µs
- Power Management/Standby Mode
- Single Supply 2.7V to 5.5V Operation

Applications

- Wireless Local Loop Systems
- Wireless Local Area Networks
- PCMCIA Wireless Duplex Transceivers
- ISM Systems
- TDMA Packet Protocol Radios
- PCS/Wireless PBX

Simplified Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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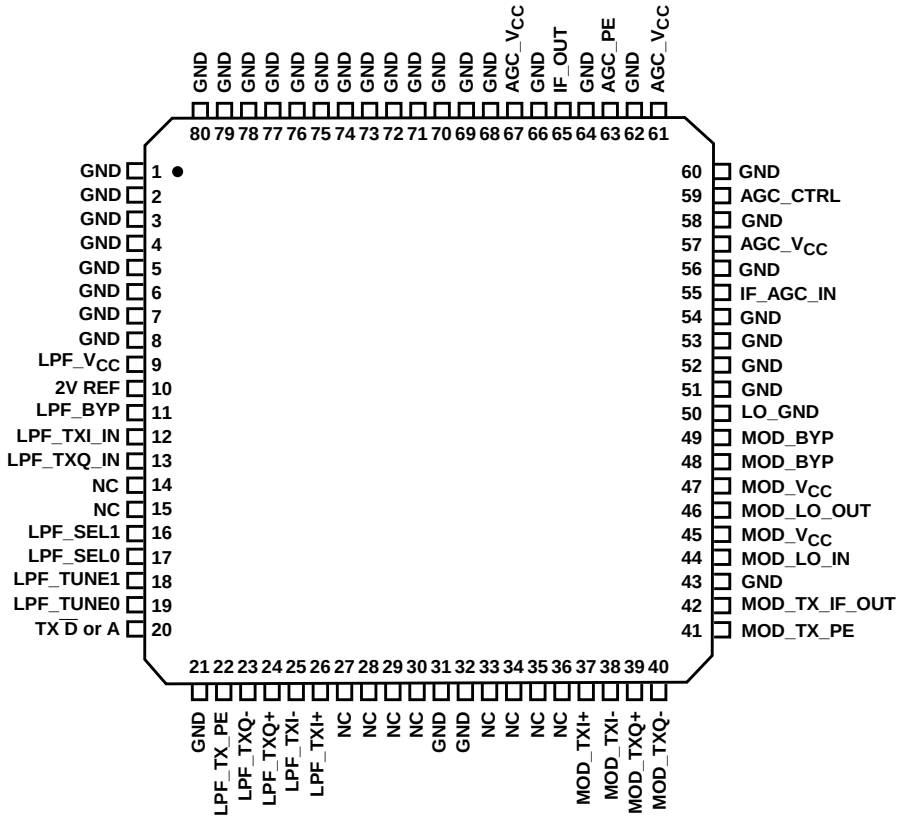
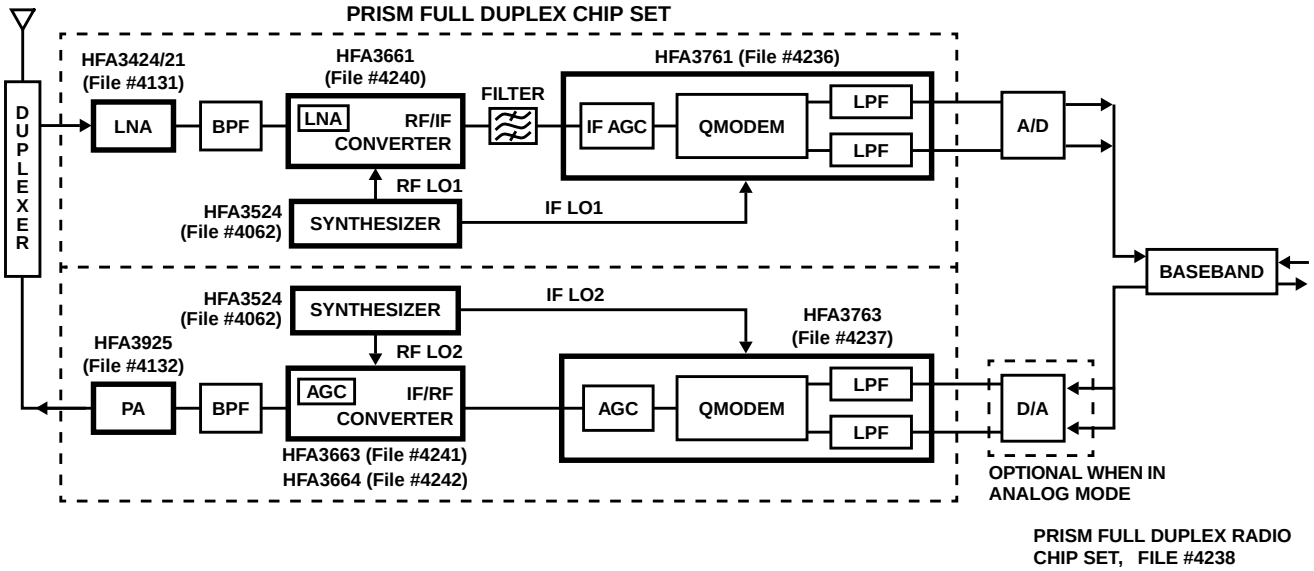
Pinout

80 LEAD TQFP
TOP VIEW

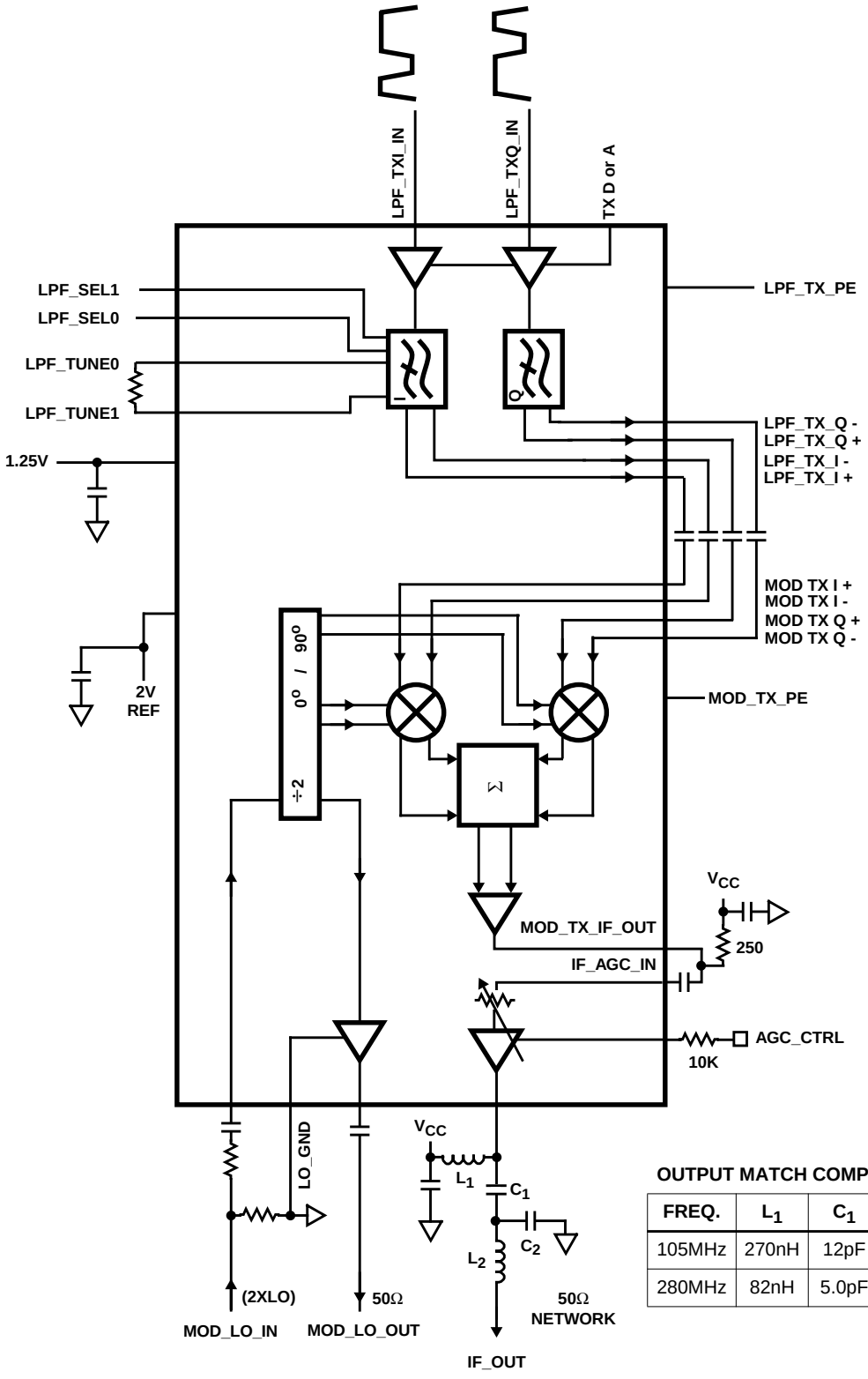


Typical Application Diagram



PRISM FULL DUPLEX RADIO
CHIP SET, FILE #4238

Block Diagram



OUTPUT MATCH COMPONENTS TABLE

FREQ.	L_1	C_1	L_2	C_2
105MHz	270nH	12pF	82nH	15pF
280MHz	82nH	5.0pF	33nH	6.0pF

NOTE: V_{CC}, GND and Bypass capacitors not shown.

Pin Descriptions

PIN	SYMBOL	DESCRIPTION
9	LPF_V_{CC}	Supply pin for the Low pass filter. Use high quality decoupling capacitors right at the pin.
10	2V REF	Stable 2V reference voltage output for external applications. Loading must be higher than 10kΩ. A bypass capacitor of at least 0.1µF is required.
11	LPF_BYP	Internal reference bypass pin. This is the common voltage (V_{CM}) used for the LPF digital thresholds. Requires 0.1µF decoupling capacitor.
12	LPF_TXI_In	Low pass filter in phase (I) channel transmit input. Conventional or attenuated direct coupling is required for digital inputs. AC couple for analog input.
13	LPF_TXQ_In	Low pass filter quadrature (Q) channel transmit input. Conventional or attenuated direct coupling is required for digital inputs. AC couple for analog input.
14	NC	Connected internally for test purpose. Leave this pin floating.
15	NC	Connected internally for test purpose. Leave this pin floating.
16	LPF_Sel1	Digital control input pins. Selects four programmed cut off frequencies for the transmit channel. Tuning speed from one cutoff to another is less than 1µs. **SEL1 SEL0 CUTOFF FREQUENCY SEL1 SEL0 CUTOFF FREQUENCY** LO LO 2.2MHz HI LO 8.8MHz LO HI 4.4MHz HI HI 17.6MHz
17	LPF_Sel0	
18	LPF_Tune1	These two pins are used to fine tune the Low pass filter cutoff frequency. A resistor connected between the two pins (R_{TUNE}) will fine tune the transmit filters. Refer to the tuning equation in the LPF AC specifications.
19	LPF_Tune0	
20	TX $\overline{D}$ or A	Selects the configuration of the Transmit baseband input for either Digital or Analog (500mV_{P-P} max). Tie to a High for Analog and Ground for Digital inputs. Requires decoupling capacitor for analog and a simple direct coupled attenuator for digital inputs.
22	LPF_TX_PE	Digital input control pin to enable the LPF transmit mode of operation. Enable logic level is High.
23	LPF_TXQ-	Negative output of the transmit Low pass filter, quadrature channel. AC coupling is required. Normally connects to the inverting input of the quadrature Modulator (Mod_TXQ-), pin 40.
24	LPF_TXQ+	Positive output of the transmit Low pass filter, quadrature channel. AC coupling is required. Normally connects to the non inverting input of the quadrature Modulator (Mod_TXQ+), pin 39.
25	LPF_TXI-	Negative output of the transmit Low pass filter, in phase channel. AC coupling is required. Normally connects to the inverting input of the in phase Modulator (Mod_TXI-), pin 38.
26	LPF_TXI+	Positive output of the transmit Low pass filter, in phase channel. AC coupling is required. Normally connects to the non inverting input of the in phase Modulator (Mod_TXI+), pin 37.
27	NC	Connected internally for test purpose. Leave this pin floating.
28	NC	Connected internally for test purpose. Leave this pin floating.
29	NC	Connected internally for test purpose. Leave this pin floating.
30	NC	Connected internally for test purpose. Leave this pin floating.
33	NC	Connected internally for test purpose. Leave this pin floating.
34	NC	Connected internally for test purpose. Leave this pin floating.
35	NC	Connected internally for test purpose. Leave this pin floating.
36	NC	Connected internally for test purpose. Leave this pin floating.
37	Mod_TXI+	In phase modulator non inverting input. AC coupling is required. This input is normally coupled to the Low pass filter positive output (LPF_TXI+), pin 26.
38	Mod_TXI-	In phase modulator inverting input. AC coupling is required. This input is normally coupled to the Low pass filter negative output (LPF_TXI-), pin 25.
39	Mod_TXQ+	Quadrature modulator non inverting input. AC coupling is required. This input is normally coupled to the Low pass filter positive output (LPF_TXQ+), pin 24.
40	Mod_TXQ-	Quadrature modulator inverting input. AC coupling is required. This input is normally coupled to the Low pass filter negative output (LPF_TXQ-), pin 23.

Pin Descriptions (Continued)

PIN	SYMBOL	DESCRIPTION
41	Mod_TX_PE	Digital input control to enable the Modulator section. Enable logic level is High for transmit.
42	Mod_TX_IF_Out	Modulator open collector output, single ended. Termination resistor to V_{CC} with a typical value of 250Ω.
44	Mod_LO_In (2XLO)	Single ended local oscillator current input. Frequency of input signal must be twice the required modulator carrier LO frequency. Input current is optimum at 200μA_{RMS}. Input matching networks and filters can be designed for a wide range of power and impedances at this port. Typical input impedance is 130Ω.This pin requires AC coupling. NOTE: High second harmonic content input waveforms may degrade I/Q phase accuracy.
45	Mod_V_{CC}	Modulator supply pin. Use high quality decoupling capacitors right at the pin.
46	Mod_LO_Out	Divide by 2 buffered output reference from “Mod_LO_in” input. Used for external applications where the modulating and demodulating carrier reference frequency is required. 50Ω single end driving capability. AC coupling is required. This output can be disabled by shorting to V_{CC} or floating pin 50.
47	Mod_V_{CC}	Modulator supply pin. Use high quality decoupling capacitors right at the pin.
48	MOD_BYP	This pin must be connected to pin 49 and decoupled to gnd. (Note 1)
49	MOD_BYP	This pin must be connected to pin 48. (Note 1)
50	LO_GND	When grounded, this pin enables the LO buffer (Mod_LO_Out). When open (NC) it disables the LO buffer.
55	IF_AGC_IN	AC coupled input to the AGC amplifier.
57	AGC_V_{CC}	AGC supply pin supply pin. Use high quality decoupling capacitors right at the pin.
59	AGC_CTRL	AGC control DC control voltage input requires external resistor to set scale factor. 10K for optimum temp. co. May require decoupling filtering capacitor.
61	AGC_V_{CC}	AGC supply pin supply pin. Use high quality decoupling capacitors right at the pin.
63	AGC_PE	Digital input control for the AGC amplifier. Enable logic level is High.
65	AGC_IF_OUT	AGC amplifier output. Output impedance of 250Ω. Need to be connected to V_{CC} by an inductor with reactance well above 250Ω.
67	AGC_V_{CC}	AGC supply pin supply pin. Use high quality decoupling capacitors right at the pin.
See Pinout	GND	All remaining pins not listed above must be connected to a solid ground plane.

NOTE:

1. If pin 50 is grounded, otherwise float.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage . . . . . -0.3V to +6.0V
Voltage on Any Other Pin. . . . . -0.3V to V_{CC} +0.3V

Operating Conditions

Supply Voltage Range . . . . . +2.7V to +5.5V
Operating Temperature Range . . . . . $-40^oC \le T_A \le 85^oC$

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
TQFP Package	75

Package Power Dissipation at 70^oC
Plastic TQFP Package 1.1W
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . $-65 \le T_A \le 150$
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(TQFP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Cascaded DC Electrical Specifications V_{CC} = 4.5V to 5.5V, Unless Otherwise Specified

PARAMETER	(NOTE 2) TEST LEVEL	TEMP (^oC)	MIN	TYP	MAX	UNITS
Total Supply Current, TX Mode at 5.5V	A	Full	-	80	106	mA
Shutdown Current at 5.5V	A	Full	-	0.8	1.0	mA
All Digital Inputs V_{IH} (TTL Threshold for All V_{CC})	A	Full	2.0	-	V_{CC}	V
All Digital Inputs V_{IL} (TTL Threshold for All V_{CC})	A	Full	-0.2	-	0.8	V
High Level Input Current at 5.5V V_{CC} for pin 16 with V_{IN} = 2.4V	A	Full	-200	-65	0	µA
High Level Input Current at 5.5V V_{CC} for pin 16 with V_{IN} = 4.0V	A	Full	-150	-30	0	µA
Low Level Input Current at 5.5V V_{CC} for pin 16 with V_{IN} = 0.8V	A	Full	-300	-95	0	µA
High Level Input Current at 5.5V V_{CC} for pins 17, 20, and 22 with V_{IN} = 2.4V	A	Full	0	50	200	µA
High Level Input Current at 5.5V V_{CC} for pins 17, 20, and 22 with V_{IN} = 4.0V	A	Full	0	80	300	µA
Low Level Input Current at 5.5V V_{CC} for pins 17, 20, and 22 with V_{IN} = 0.8V	A	Full	0	15	150	µA
High Level Input Current at 5.5V V_{CC} for pins 41 and 63 with V_{IN} = 2.4V	A	Full	-20	1	20	µA
High Level Input Current at 5.5V V_{CC} for pin 41 with V_{IN} = 4.0V	A	Full	0	110	300	µA
High Level Input Current at 5.5V V_{CC} for pin 63 with V_{IN} = 4.0V	A	Full	-20	1.5	20	µA
Low Level Input Current at 5.5V V_{CC} for pins 41 and 63 with V_{IN} = 0.8V	A	Full	-20	.1	20	µA
Power Down/Up Switching Speed	C	25	-	10	-	µs
Reference Voltage	A	Full	1.85	2.0	2.15	V
Reference Voltage Variation Over Temperature	B	Full	-	800	-	$\mu V/^oC$
Reference Voltage Variation Over Supply Voltage	B	25	-	1.6	-	mV/V
Reference Voltage Minimum Load Resistance	C	25	10	-	-	kΩ

NOTE:

2. A = Production Tested, B = Based on Characterization, C = By Design

Cascaded AC Electrical Specifications, Modulator Performance V_{CC} = 4.5V to 5.5V

PARAMETER	(NOTE 3) TEST LEVEL	TEMP (^oC)	MIN	TYP	MAX	UNITS
IF Modulator Output Power (Note 6)	A	25	-4	1	6	dBm
IF Modulator I/Q Amplitude Balance (Note 4)	B	Full	-1.0	0	+1.0	dB
IF Modulator I/Q Phase Balance (Note 4)	B	Full	-4.0	0	+4.0	Degrees

Cascaded AC Electrical Specifications, Modulator Performance V_{CC} = 4.5V to 5.5V (Continued)

PARAMETER	(NOTE 3) TEST LEVEL	TEMP (^oC)	MIN	TYP	MAX	UNITS
IF Modulator Side Band Suppression at 105MHz (Note 5)	A	Full	25	41	-	dBc
	A	25	33	41	-	dBc
IF Modulator Side Band Suppression at 400MHz	C	25	28	-	-	dBc
IF Mod Carrier Suppression (LO Buffer Enabled) (Note 5)	C	25	28	30	-	dBc
IF Mod Carrier Suppression (LO Buffer Disabled) (Note 5)	A	25	28	38	-	dBc
IF Modulator I/Q 3dB Cutoff SEL0/1 = 2.2MHz	B	25	1.98	2.2	2.42	MHz
IF Modulator I/Q 3dB Cutoff SEL0/1 = 4.4MHz	B	25	3.96	4.4	4.84	MHz
IF Modulator I/Q 3dB Cutoff SEL0/1 = 8.8MHz	B	25	7.92	8.8	9.68	MHz
IF Modulator I/Q 3dB Cutoff SEL0/1 = 17.6MHz	B	25	15.84	17.6	19.36	MHz

NOTES:

3. A = Production Tested, B = Based on Characterization, C = By Design
4. Data is characterized by DC levels applied to MOD TXI and Q pins for 4 quadrants with LO output as reference or indirectly by the SSB characteristics.
5. Analog mode with an input frequency of 1MHz and an input amplitude of 400mV_{P-P} and a 2.2MHz lowpass filter cutoff with V_{AGC} = 1.25V.
6. Data is characterized with V_{AGC} = 1V with an input of 400mV_{P-P} at LPF_TXI_IN and LPF_TXQ_IN.

DC/AC Electrical Specifications AGC/Attenuator, Individual Performance V_{CC} = 4.5V to 5.5V Unless Otherwise Specified

PARAMETER	(NOTE 7) TEST LEVEL	TEMP (^oC)	MIN	TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS AGC ATTENUATOR INDIVIDUAL PERFORMANCE						
AGC Scale Factor at 100MHz at 3dB	A	25	36	45	54	dB/V
AGC Linearity: Max-to-Min Scale Factor at 0dB to 45dB AGC with External 10kΩ	A	25	0.9:1	2:1	3:1	-
AGC Control Input for 45dB Max Attenuation with External 10kΩ	A	25	1.7	2.0	2.5	V
AGC Control Input for -3 dB from Minimum Attenuation (Gain Approx. = 6dB) with External 10kΩ	A	25	1.0	1.2	1.4	V
AGC Input Bias Current with External 10kΩ at -45 dB	A	Full	-	-	120	µA
AC ELECTRICAL SPECIFICATIONS AGC ATTENUATOR INDIVIDUAL PERFORMANCE						
Frequency Range	B	25	10	-	400	MHz
Power Gain at min AGC at 100MHz V_{AGC} = 1.0V	C	25	-	9.0	-	dB
Power Gain Temperature Coefficient V_{AGC} = 1.0V	B	25	-	+0.013	-	dB/deg
Output P1dB at Minimum AGC, 100MHz V_{AGC} = 1.0V	B	25	-	8.0	-	dBm
Output IP3 at Minimum AGC, 100MHz V_{AGC} = 1.0V	B	25	-	17.5	-	dBm
AGC/Attenuator Range	A	25	42	45	-	dB
AGC Settling Time to 1dB, 0dB to -40dB	C	25	-	-	10	µs
Output Impedance	C	25	-	250	-	Ω
Input Impedance	C	25	-	250	-	Ω
Gain Flatness, 20MHz Bandwidth	C	25	-	0.02	-	dB
Phase Shift vs AGC at 100MHz	C	25	-	-0.045	-	deg/dB
Power Down/Up Switching Speed (Note 3)	C	25	-	-	10	µs

NOTE:

7. A = Production Tested, B = Based on Characterization, C = By Design

AC Electrical Specifications, I/Q Up Converter and LO Individual Performance

V_{CC} = 4.5V to 5.5V Unless Otherwise Specified

PARAMETER	(NOTE 8) TEST LEVEL	TEMP (^oC)	MIN	TYP	MAX	UNITS
2XLO Input Frequency Range (2 X Input Range)	B	25	20	-	800	MHz
2XLO Input Current Range	C	25	50	200	300	μA_{RMS}
2XLO Input Impedance	C	25	-	130	-	Ω
Buffered LO Output Voltage, Single Ended	A	25	80	100	-	mV_{P-P}
Buffered LO Output Impedance	C	25	-	50	-	Ω
Quadrature IF Modulator Output Frequency Range	B	25	10	-	400	MHz
IF Modulator I/Q Input Frequency Range	C	25	-	-	30	MHz
IF Modulator Differential I/Q Max Input Voltage	C	25	-	2.25	-	V_{P-P}
IF Modulator Differential I/Q Input Impedance	C	25	-	4	-	kΩ
IF Modulator Differential Input Capacitance	C	25	-	0.5	-	pF
IF Modulator I/Q Amplitude Balance	B	Full	-1.0	-	1.0	dB
IF Modulator I/Q Phase Balance at 105MHz	B	Full	-4	-	4	Degrees
IF Modulator I/Q Phase Balance at 400MHz	C	25	-4	-	4	Degrees
IF Modulator Carrier Suppression (LO Buffer Enabled)	C	25	28	30	-	dBc
IF Modulator Carrier Suppression (LO Buffer Disabled)	A	25	28	38	-	dBc
IF Modulator SSB Sideband Suppression at 105MHz	A	Full	25	41	-	dBc
	A	25	33	41	-	dBc
IF Modulator SSB Sideband Suppression at 400MHz	C	25	28	-	-	dBc
IF Output Level Compression Point	C	25	-	1.0	-	V_{P-P}
IF Modulator Intermodulation Suppression	B	25	26	-	-	dBc

NOTE:

8. A = Production Tested, B = Based on Characterization, C = By Design

AC Electrical Specifications, TX Buffer Individual Performance V_{CC} = 4.5V to 5.5V Unless Otherwise Specified

PARAMETER	(NOTE 9) TEST LEVEL	TEMP (^oC)	MIN	TYP	MAX	UNITS
TX LPF Buffer Analog Input Range	A	25	-	500	-	mV_{P-P}
TX LPF Buffer Analog/Digital Input Impedance	C	25	10	12.5	-	kΩ

NOTE:

9. A = Production Tested, B = Based on Characterization, C = By Design

AC Electrical Specifications, RX/TX 5TH Order LPF Individual Performance

V_{CC} = 4.5V to 5.5V Unless Otherwise Specified

PARAMETER	(NOTE 10) TEST LEVEL	TEMP (^oC)	MIN	TYP	MAX	UNITS
TX LPF 3dB Bandwidth, Sel0 = 0, Sel1 = 0	B	25	1.98	2.20	2.42	MHz
TX LPF 3dB Bandwidth, Sel0 = 1, Sel1 = 0	B	25	3.96	4.40	4.84	MHz
TX LPF 3dB Bandwidth, Sel0 = 0, Sel1 = 1	B	25	7.92	8.80	9.68	MHz
TX LPF 3dB Bandwidth, Sel0 = 1, Sel1 = 1	B	25	15.84	17.60	19.36	MHz
TX LPF Sel0, Sel1 Tuning Speed	B	25	-	-	1	µs

AC Electrical Specifications, RX/TX 5TH Order LPF Individual Performance

V_{CC} = 4.5V to 5.5V Unless Otherwise Specified **(Continued)**

PARAMETER	(NOTE 10) TEST LEVEL	TEMP (^{o}C)	MIN	TYP	MAX	UNITS
TX LPF 3dB Bandwidth Tuning	B	25	-20	-	+20	%
LPF Tune Nominal Resistance	B	25	-	787	-	Ω
TX/RX LPF Total Harmonic Distortion	B	25	-	1	-	%
LPF Output Impedance, Single Ended	C	25	-	50	-	Ω

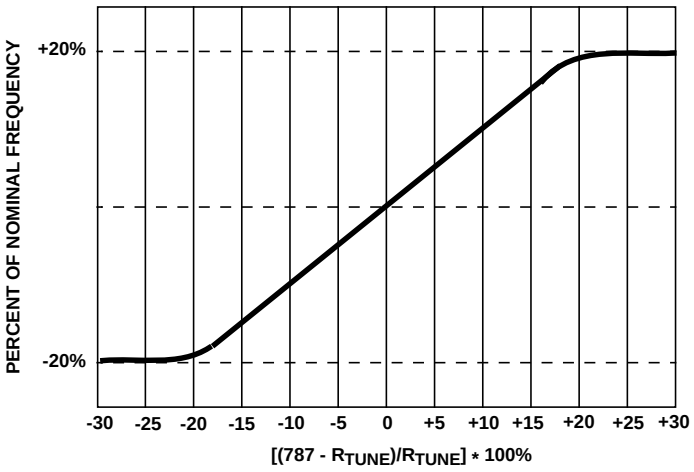
NOTE:

10. A = Production Tested, B = Based on Characterization, C = By Design

TABLE 1. LOW PASS FILTER PROGRAMING AND TUNING INFORMATION

MODE	LPF SEL1	LPF SEL0	f_{3dB} (NOMINAL R_{TUNE})
BW0	0	0	2.2MHz
BW1	0	1	4.4MHz
BW2	1	0	8.8MHz
BW3	1	1	17.6MHz

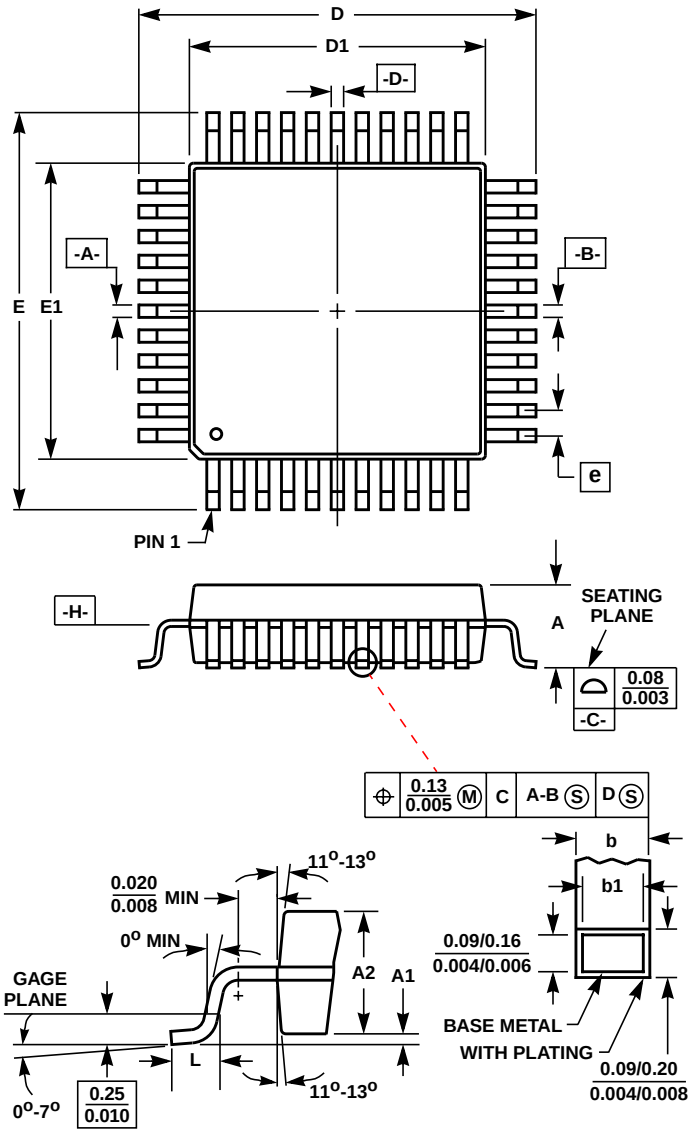
$$f_{TUNED}3dB = \frac{f_{3dBNOMINAL} * 787}{R_{TUNE}}$$



FREQUENCY	R_{TUNE}
20% Low	984Ω
Nominal	787Ω
20% High	656Ω

FIGURE 1. TYPICAL f_{3dB} vs R_{TUNE}

Thin Plastic Quad Flatpack Packages (LQFP)



Q80.14x14 (JEDEC MS-026BEC ISSUE C)
80 LEAD THIN PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.062	-	1.60	-
A1	0.002	0.005	0.05	0.15	-
A2	0.054	0.057	1.35	1.45	-
b	0.009	0.014	0.22	0.38	6
b1	0.009	0.012	0.22	0.33	-
D	0.626	0.634	15.90	16.10	3
D1	0.547	0.555	13.90	14.10	4, 5
E	0.626	0.634	15.90	16.10	3
E1	0.547	0.555	13.90	14.10	4, 5
L	0.018	0.029	0.45	0.75	-
N	80		80		7
e	0.026 BSC		0.65 BSC		-

Rev. 2 4/99

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm (0.003 inch).
7. “N” is the number of terminal positions.

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