DATA SHEET

TDA10085HT
Single chip DVB-S/DSS channel receiver

Product specification
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File under Integrated Circuits, IC02

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Philips
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CONTENTS

Single chip DVB-S/DSS channel receiver TDA10085HT

1 FEATURES

- DSS and DVB-S compliant single chip demodulator and forward error correction
- Dual 6-bit Analog-to-Digital Converter (ADC) on-chip
- PLL that allows using a low-cost crystal (typically 4 MHz)
- DiSEqC 1.X from 1 to 8 byte-long sequences with modulated or unmodulated output
- DSS dish control
- Digital cancellation of ADC offset
- Simultaneous parallel and serial output interfaces
- Variable rate BPSK/QPSK coherent demodulator
- Modulation rate variable from 1 to 49 Mbauds
- Automatic gain control output
- Digital symbol timing recovery:
  - Acquisition range up to 960 ppm
- Carrier offset cancellation up to one half of the sampling frequency
- Digital carrier recovery:
  - Acquisition range up to 12% of the symbol rate
- Half-Nyquist filters: roll-off = 0.35 for DVB and 0.2 for DSS
- Interpolating and anti-aliasing filters to handle variable symbol rates
- Channel quality estimation
- Spectral inversion ambiguity resolution
- Viterbi decoder:
  - Supported rates from 1/2 to 8/9
  - Constraint length K = 7 with G1 = 171_8 and G2 = 133_8
  - Viterbi output BER measurement
  - Automatic code rate search within $^1/_2$, $^2/_3$ and $^6/_7$ in DSS mode
  - Automatic code rate search within $^1/_2$, $^2/_3$, $^3/_4$, $^5/_6$ and $^7/_8$ in DVB-S mode
- Convolutional de-interleaver and Reed Solomon decoder according to DVB and DSS specifications
- Automatic frame synchronization
- Selectable DVB-S descrambling
- I²C-bus interface
- 64-pin TQFP package
- CMOS technology (0.2 μm, 1.8 V to 3.3 V).

2 APPLICATIONS

- DVB-S receivers (ETS 300-421)
- DSS receivers.

3 GENERAL DESCRIPTION

The TDA10085 is a single-chip channel receiver for satellite television reception matching both DSS and DVB-S standards. The device contains a dual 6-bit flash ADC, variable rate BPSK/QPSK coherent demodulator and forward error correction functions. The ADC interfaces directly with I and Q analog baseband signals.
After analog-to-digital conversion, the TDA10085 implements a bank of cascadable filters as well as anti-alias and half-Nyquist filters. An analog AGC signal is generated using an amplitude estimation function. The TDA10085 performs clock recovery at twice the baud rate and achieves coherent demodulation without any feedback to the local oscillator. Forward error correction is built around two error-correcting codes: a Reed-Solomon (outer code) and a Viterbi decoder (inner code). The Reed-Solomon decoder corrects up to 8 erroneous bytes among the N (204) bytes of one data packet.
A convolutional de-interleaver is located between the Viterbi output and the Reed-Solomon decoder input. The de-interleaver and Reed-Solomon decoder are automatically synchronized according to a frame synchronization algorithm that uses the sync pattern present in each packet. The TDA10085 is controlled via an I²C-bus interface. The circuit operates at sampling frequencies up to 100 MHz, can process variable modulation rates and achieves transmission rates up to 45 Mbaud. Furthermore, for dish control applications, hardware supports DiSEqc 1.x with control access via the I²C-bus.

An interrupt line that can be programmed to activate on events or on timing information is provided.

Designed in 20 micron CMOS technology and housed in a TQFP64 package, the TDA10085 operates over the commercial temperature range.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		VERSION
	NAME	DESCRIPTION	
TDA10085HT	TQFP64	plastic thin quad flat package; 64 leads; body 10 × 10 × 1.0 mm	SOT357-1

5 BLOCK DIAGRAM

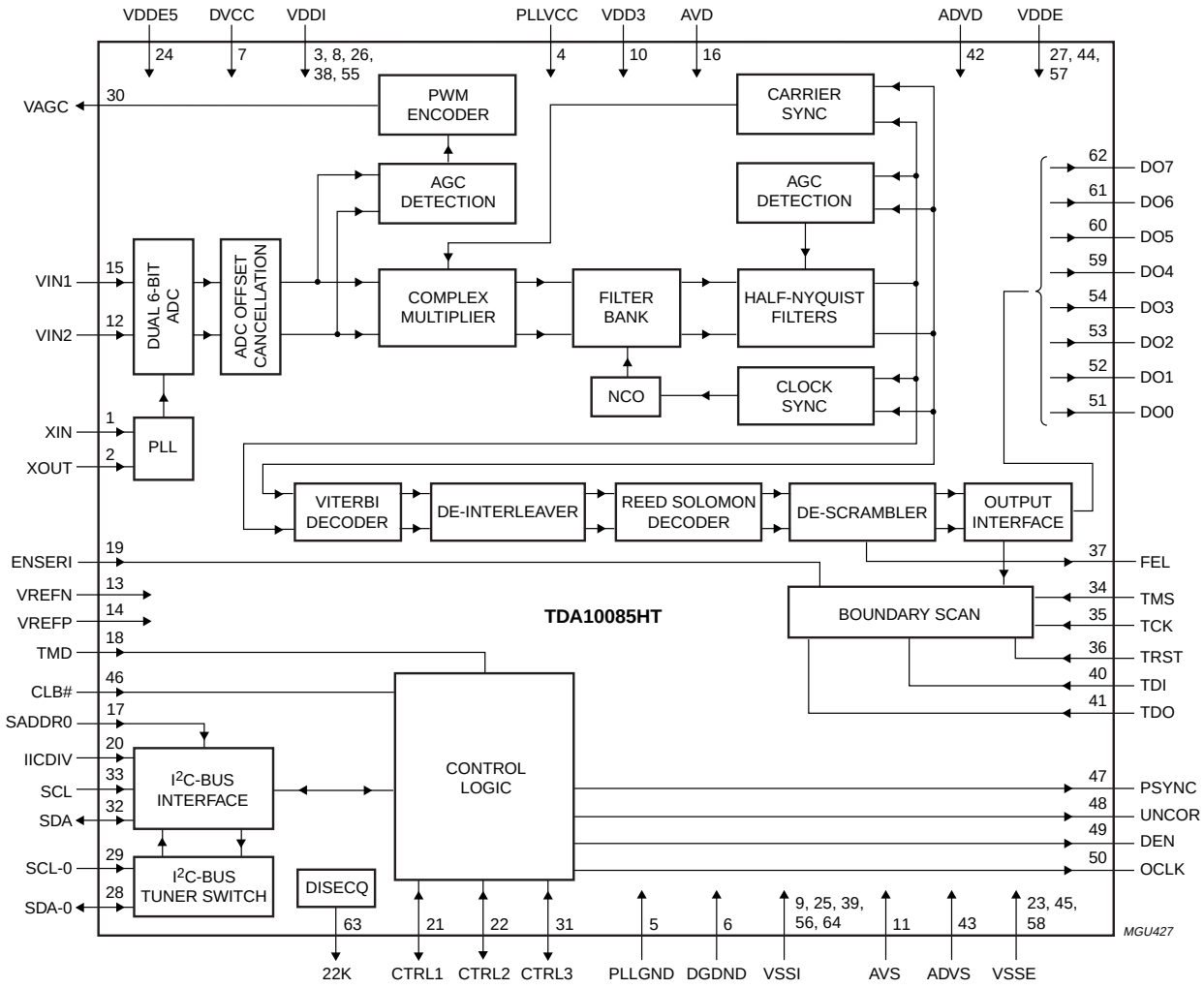


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
XIN	1	I	crystal oscillator input and output pins; in a typical application, a fundamental oscillator crystal is connected between pins XIN and XOUT; see note 1
XOUT	2	I	
VDDI	3	supply	digital core supply voltage (typically 1.8 V)
PLLVCC	4	supply	analog supply voltage for the PLL (typically 3.3 V)
PLLGND	5	ground	analog ground for the PLL
DGND	6	ground	digital PLL core ground voltage; see note 2
DVCC	7	supply	digital PLL core supply voltage (typically 1.8 V)
VDDI	8	supply	digital ADC supply voltage (typically 1.8 V)
VSSI	9	ground	digital ADC ground voltage; see note 2
VDD3	10	supply	analog ADC supply voltage (typically 3.3 V)
AVS	11	ground	analog ground voltage
VIN2	12	I	analog signal input for channel Q; see note 1
VREFN	13	O	negative analog voltage reference output (typically 1.25 V); a decoupling capacitor (typically 0.1 μF) must be placed as close as possible between VREFN and GND
VREFP	14	O	positive analog voltage reference output (typically 2 V); a decoupling capacitor (typically 0.1 μF) must be placed as closed as possible between VREFP and GND
VIN1	15	I	analog signal input for channel I; see note 1
AVD	16	supply	analog supply voltage (typically 3.3 V); a 0.1 μF decoupling capacitor must be placed between AVD and AVS
SADDR0	17	I	SADDR0 input signal is the LSB of the I^2C-bus address of the TDA10085; other bits of the address are set internally to 000111, therefore the complete I^2C-bus address is (MSB to LSB): 0, 0, 0, 1, 1, 1 plus the SADDR0 bit; see note 1
TMD	18	I	test input; must be connected to ground for normal operation; see note 1
ENSERI	19	I	enable serial interface input; when HIGH, the serial transport stream is present on the boundary scan pins (TRST, TDO, TCK, TDI and TMS); when LOW, the boundary scan pins are available; note 1
IICDIV	20	I	input to select the I^2C-bus internal system clock frequency (depends on the crystal frequency); internal I^2C-bus clock is XIN when IICDIV = 0 and XIN/4 if IICDIV = 1; see note 1
CTRL1	21	OD	control line output 1; this pin function is directly programmable through the I^2C-bus interface; default value is logic 1; open-drain output requiring an external pull-up resistor to 3.3 V or to 5 V
CTRL2	22	OD	control line output 2; this pin function is directly programmable through the I^2C-bus interface; default value is logic 1; open-drain output requiring an external pull-up resistor to 3.3 V or to 5 V
VSSE	23	ground	digital ground voltage; see note 2
VDDE5	24	supply	digital 5 V supply voltage; required for the 5 V tolerance of inputs
VSSI	25	ground	digital core ground voltage; see note 2

SYMBOL	PIN	TYPE	DESCRIPTION
VDDI	26	supply	digital core supply voltage (typically 1.8 V)
VDDE	27	supply	digital supply voltage (typically 3.3 V)
SDA_0	28	I/OD	I^2C-bus bidirectional serial input/ open drain output; equivalent to SDA but with a high-impedance state programmable via the I^2C-bus; a pull-up resistor must be connected between this pin and DVCC
SCL_0	29	OD	I^2C-bus clock output; equivalent to SCL but with a high-impedance state programmable via the I^2C-bus; open drain output requiring an external pull-up resistor to 5 V
VAGC	30	O or OD	PWM encoded output signal for AGC; the refresh frequency of AGC information is the sampling frequency divided by 2048, the maximum signal frequency on the VAGC output is $^1/_4 \times$ AGC sampling clock; the VAGC output can be selected by I^2C-bus to be open-drain or have 3.3 V capability (typically, output VAGC is fed to the AGC amplifier through a single RC network)
CTRL3	31	I/OD	control line 3 input/open drain output; this pin function is directly programmable through the I^2C-bus interface and is an input by default; it requires a pull-up resistor to 3.3 or 5 V, or a pull-down resistor to GND
SDA	32	I/OD	I^2C-bus bidirectional serial data input/output; the open-drain output requires a pull-up resistor (typically 2.2 kΩ) to be connected between SDA and 5 V for proper operation
SCL	33	I	I^2C-bus clock input; nominally a square wave with a maximum frequency of 400 kHz generated by the system I^2C-bus master; see note 1
TMS	34	I/O	boundary scan mode: test mode select input/output; provides the logic levels needed to change the TAP controller from state to state serial mode enabled (ENSERI = 1): serial TS uncorrectable output; when not in serial mode, TMS must be set to VSS
TCK	35	I/O	boundary scan mode: test clock input/output; TCK is an independant clock used to drive the TAP controller serial mode enabled (ENSERI = 1): TCK is the serial TS clock output; when not in serial mode, TCK must be set to VSS
TRST	36	I/O	boundary scan mode: test reset input/output; TRST is an active-LOW reset input to the TAP controller serial mode enabled (ENSERI = 1): test reset input/output; TRST is the serial TS PSYNC output; when not in serial mode, TRST must be set to VSS
FEL	37	OD	front-end locked output signal that goes HIGH when demodulator, Viterbi decoder and de-interleaver are all synchronized; open-drain output requiring an external pull-up resistor to 3.3 or 5 V; can be set via the I^2C-bus to be an interrupt pin
VDDI	38	supply	digital core supply voltage (typically 1.8 V)
VSSI	39	ground	digital core ground voltage; see note 2
TDI	40	I/O	boundary scan mode: test data and instruction serial input serial mode enabled (ENSERI = 1): serial TS data output; must be set to VSS when not in serial mode

SYMBOL	PIN	TYPE	DESCRIPTION
TDO	41	I/O	boundary scan mode: test data serial output; output provided on the falling edge of TCK serial mode enabled (ENSERI = 1): serial TS enable input; must be set to VSS when not in serial mode
ADVD	42	supply	analog supply voltage for the 2nd PLL (typically 1.8 V)
ADVS	43	ground	analog ground voltage for the 2nd PLL
VDDE	44	supply	digital supply voltage (typically 3.3 V)
VSSE	45	ground	digital ground voltage; see note 2
CLB#	46	I	asynchronous, active LOW input that clears the TDA10085; when CLB# goes LOW the circuit immediately enters its RESET mode and normal operation resumes three XIN rising edges later after CLB# returns HIGH; at RESET, the I^2C-bus register contents are all initialized to their default values; the minimum width of CLB# LOW level is three XIN clock periods; pin CLB# is not TTL, 5 V tolerant
PSYNC	47	O	packet sync output signal goes HIGH on a rising edge of OCLK each time the first byte of a packet is provided
UNCOR	48	O	uncorrectable packet output signal goes HIGH on a rising edge of OCLK when the packet provided is uncorrectable
DEN	49	O	data enable; this output signal is HIGH when there is valid data on bus DO[7:0]
OCLK	50	O	output clock for the parallel DO[7:0] outputs; OCLK is generated internally and depends on which interface type is selected
DO0	51	O	transport stream data output bits; part of the 8-bit parallel data output after demodulation, Viterbi decoding, de-interleaving, RS decoding and de-scrambling; possible output interfaces are three parallel and two serial
DO1	52	O	
DO2	53	O	
DO3	54	O	
VDDI	55	supply	digital core supply voltage (typically 1.8 V)
VSSI	56	ground	digital core ground voltage; see note 2
VDDE	57	supply	digital supply voltage (typically 3.3 V)
VSSE	58	ground	digital ground voltage; see note 2
DO4	59	O	transport stream data output bits; part of the 8-bit parallel data output after demodulation, Viterbi decoding, de-interleaving, RS decoding and de-scrambling; possible output interfaces are three parallel and two serial
DO5	60	O	
DO6	61	O	
DO7	62	O	
22K	63	O	22 kHz output used to control the antenna LNB (output is controlled via the I^2C-bus interface)
VSSI	64	ground	digital core ground voltage; see note 2

Notes

1. TTL, 5 V tolerant input (if VDDE5 is connected to 5 V).
2. DGND, VSSI and VSSE can be connected to the same ground plane.

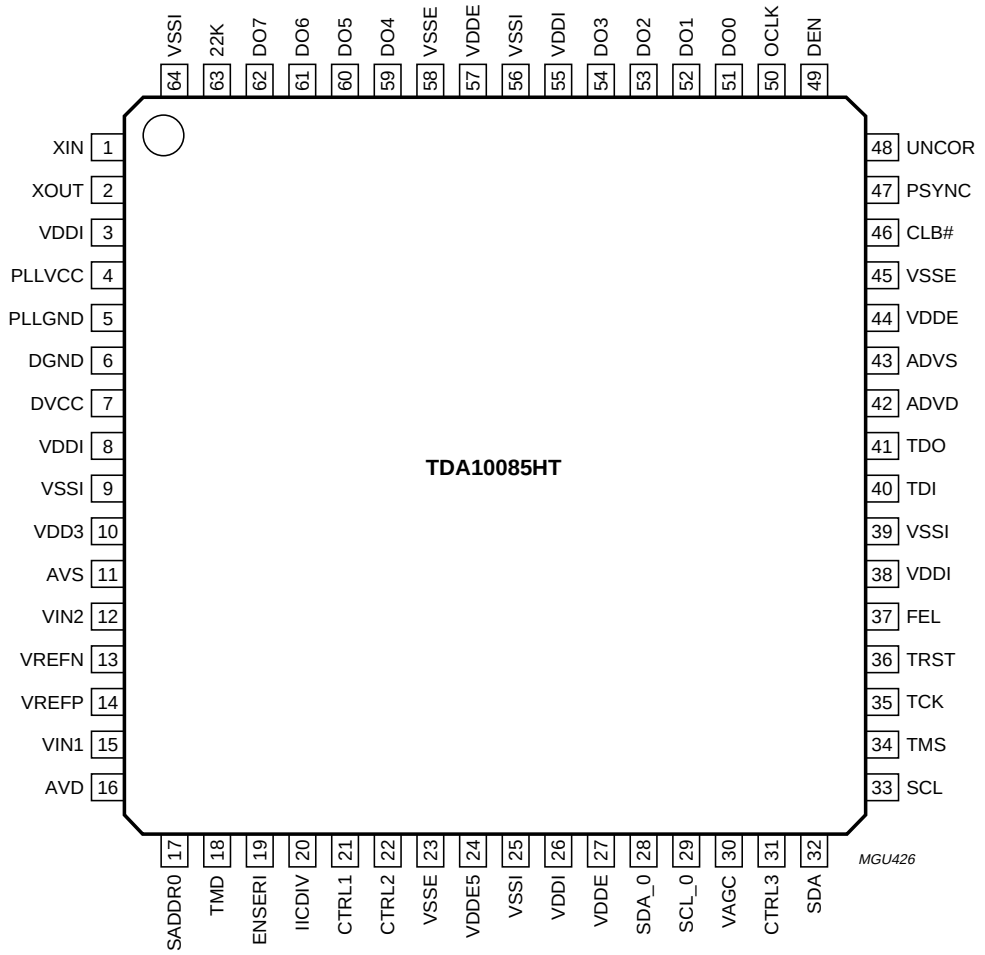


Fig.2 Pin configuration.

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); note 1

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{VDDE}	DC supply voltage	–0.5	+4.1	V
V_{VDDI}	DC core supply voltage	–0.5	+2.2	V
V_I	DC input voltage	–0.5	V_{VDDE} + 0.5	V
T_{amb}	ambient temperature	0	70	°C
T_j	junction temperature	–	150	°C
T_{sp}	solder point temperature	–	300	°C

Note

1. Stresses above the Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.

8 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	45	K/W

9 CHARACTERISTICS

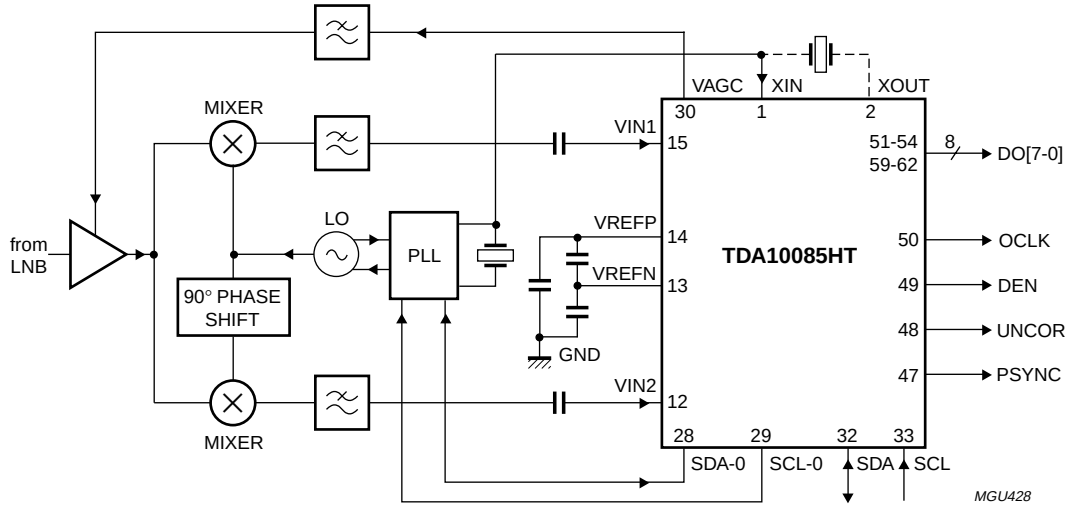
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{VDDE}	digital supply voltage		3.0	3.3	3.6	V
V_{VDDI}	digital core supply voltage		1.6	1.8	2.0	V
V_{VDDE5}	digital 5 V supply voltage	for 5 V tolerance of inputs	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	TTL input; note 1	2.0	–	V_{VDDE} + 0.3	V
V_{IL}	LOW-level input voltage	TTL input	–0.5	–	+0.8	V
V_{OH}	HIGH-level output voltage	I_{OH} = –0.8 mA	V_{VDDE} – 0.1	–	–	V
		$I_{OH} = -I_{O(max)}$; note 4	2.4	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 0.8 mA	–	–	0.1	V
		$I_{OL} = I_{O(max)}$; note 4	–	–	0.4	V
I_{VDDE}	supply current for V_{VDDE}	f_s = 96 MHz	68	–	78	mA
I_{VDDI}	supply current for V_{VDDI}	symbol rate				
		1 Mbaud	–	38	–	mA
		27.5 Mbauds	–	93	–	mA
		45 Mbauds	–	–	139	mA
C_i	input capacitance		–	10	–	pF
XIN						
f_{XIN}	crystal frequency		–	4	–	MHz
V_{IH}	HIGH-level input voltage		$0.7V_{VDDE}$	–	V_{VDDE}	V
V_{IL}	LOW-level input voltage		0	–	$0.3V_{VDDE}$	V
PLL						
V_{DVCC}	digital PLL supply voltage		1.6	1.8	2.0	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{PLLVCC}	analog PLL supply voltage		3.0	3.3	3.6	V
ADC						
V_{VDD3}	3 V ADC digital supply voltage		3.0	3.3	3.6	V
V_{AVD}	analog supply voltage		3.0	3.3	3.6	V
V_{VIN1}, V_{VIN2}	analog input voltage DC component AC component		 V_{VREFN} –	 – 750	 V_{VREFP} –	 V mV
C_i	analog input capacitance		–	–	16	pF
V_{VREFP}	top voltage reference		–	2.475	–	V
V_{VREFN}	bottom voltage reference		–	1.725	–	V
SINAD	ADC signal to noise and distortion ratio	note 2	–	34	–	dB
THD	total harmonic distortion	note 3	–	35	–	dB

Notes

1. All inputs except pin CLB# are 5 V tolerant.
2. Signal-to-noise plus distortion ratio (SINAD): ratio between the RMS magnitude of the fundamental input frequency to the RMS magnitude of all other ADC output signals.
3. Total Harmonic Distortion (THD): ratio of the RMS sum of all harmonics of the input signal (below one half of the sampling frequency) to the RMS value at the fundamental frequency.
4. $I_{O(max)}$ = 8 mA for pins OCLK and TCK
   $I_{O(max)}$ = 4 mA for pins DO[7:0], DEN, PSYNC, UNCOR, TDI, TDO, TRST, TMS, SDA, SCL_O and SDA_O
   $I_{O(max)}$ = 2 mA for pins CTRL1, CTRL2, CTRL3, VAGC and FEL, 22K.

10 APPLICATION INFORMATION



The TDA10085 can receive a 4 MHz clock signal delivered by the PLL synthesizer, or can generate the sampling clock from a crystal connected between XIN and XOUT.

Bypass capacitors (0.1 μF) should be placed close to ADC voltage references VREFP and VREFN.

Fig.3 Front-end receiver schematic.

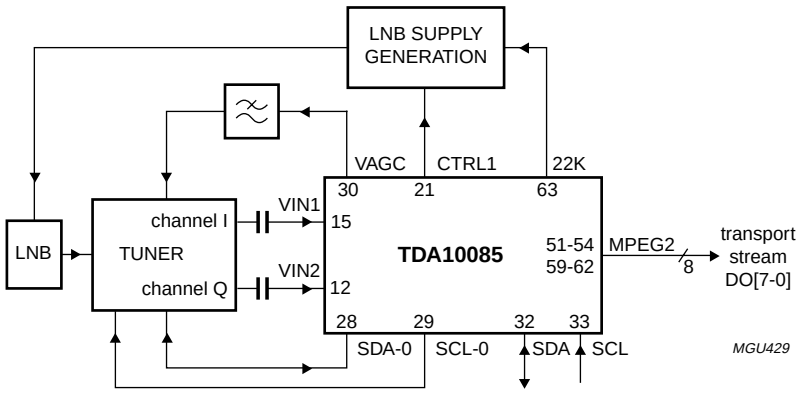
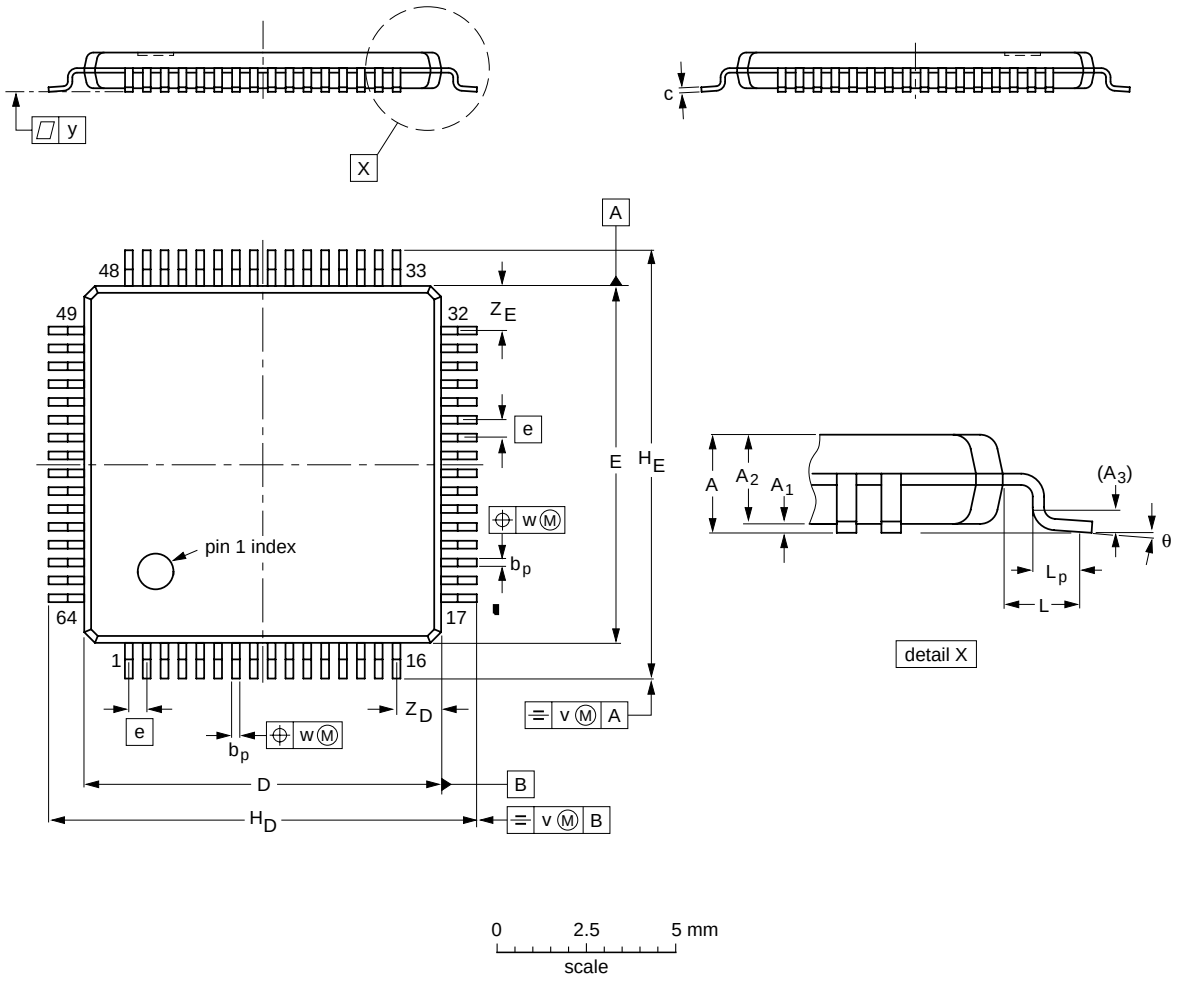


Fig.4 Typical use of CTRL1 and 22K outputs.

11 PACKAGE OUTLINE

TQFP64: plastic thin quad flat package; 64 leads; body 10 x 10 x 1.0 mm **SOT357-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.2	0.08	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT357-1	137E10	MS-026				~~99-12-27~~ 00-01-19

12 SOLDERING

12.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

12.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

12.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

12.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

12.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

13 DATA SHEET STATUS

DATA SHEET STATUS(1)	PRODUCT STATUS(2)	DEFINITIONS
Objective specification	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary specification	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product specification	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

14 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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