19-1832; Rev 0a; 1/01

MAXIM

-48V Simple Swapper Hot-Swap Switches

General Description

The MAX5911/MAX5912 are fully integrated hot-swap switches for negative supply rails. These devices allow the safe insertion and removal of circuit cards into live backplanes or ports without causing problematic glitches on the negative power-supply rail. They also monitor various circuit parameters and disconnect the load if a fault condition occurs, alerting the host with a logic-level $\overline{\text{FAULT}}$ output. The MAX5911/MAX5912 operate over a voltage range of -16V to -65V and are designed to permit hot plugging of an IP phone into a hub, but are not limited to that operation.

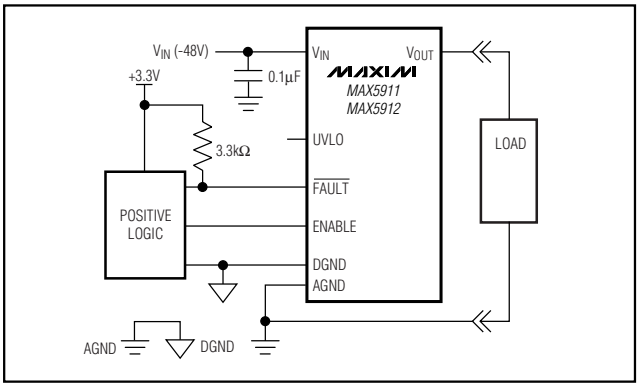
During startup, an internal power FET regulates the current between the backplane power source and the load to 280mA for MAX5911 and 415mA for MAX5912. After startup, the FET is fully enhanced to reduce its on-resistance. To ensure robust operation, the MAX5911/MAX5912 contain built-in safety features that prevent damage to the internal FET. They include an enable input, which responds to positive logic signals (+3.3V or +5V), allowing the host system to disconnect the load. ENABLE is also used to reset the device after a latching fault condition occurs.

The MAX5911/MAX5912 Simple Swapper™ hot-swap ICs monitor four parameters for these fault conditions: undervoltage lockout (UVLO), power-not-good, zero-current detection, and thermal shutdown. These devices are available in the extended temperature range, -40°C to +85°C. The MAX5911 and MAX5912 come in 8-pin and 16-pin SOIC packages, respectively.

Applications

IP Phones
Network Routers
Network Switches
Internet Appliances
Power-Over-LAN

Typical Operating Circuit



Features

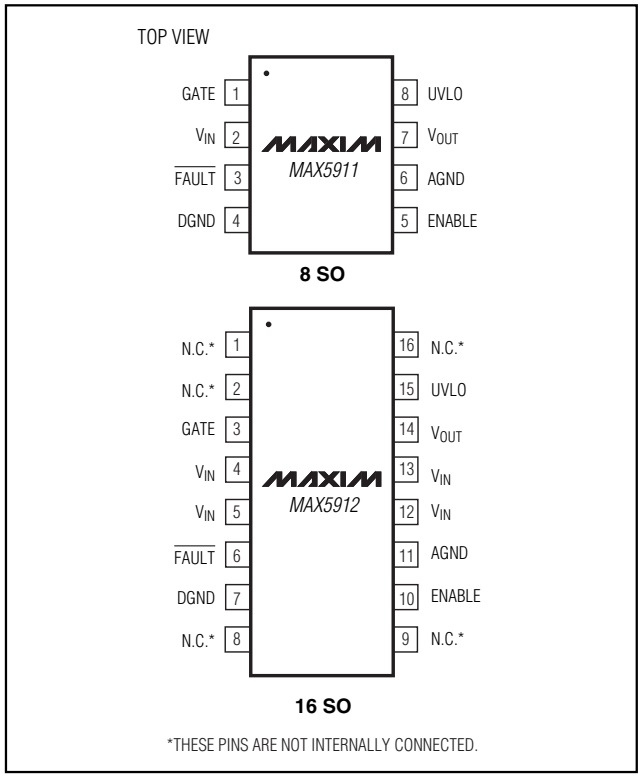
- **Provides Safe Hot Swap for -16V to -65V Power Supplies**
- **280mA Current Limit for MAX5911**
- **415mA Current Limit for MAX5912**
- **Zero-Current Load Disconnect**
- **Integrated Power FET**
- **Status Output Reports Fault Condition**
- **Internal Switch-Protection Circuitry**
- **Built-In Thermal Shutdown**
- **DGND Can Vary Up to ±5V with Respect to AGND**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX5911ESA	-40°C to +85°C	8 SO
MAX5912ESE	-40°C to +85°C	16 SO

Simple Swapper is a trademark of Maxim Integrated Products, Inc.

Pin Configurations



-48V Simple Swapper Hot-Swap Switches

ABSOLUTE MAXIMUM RATINGS

Voltages are with respect to AGND, unless otherwise noted.

V_{IN} .....+0.3V to -70V
V_{OUT} .....+0.3V to (V_{IN} - 0.3V)
ENABLE to DGND .....-0.3V to +11V
ENABLE to V_{IN} .....-0.3V to +70V
$\overline{FAULT}$ to DGND .....-0.3V to +11V
UVLO to V_{IN}.....-0.3V to +11V
DGND .....-5V to +5V
DGND to V_{IN}.....-0.3V to +70V
$\overline{FAULT}$ Sink Current 10mA
Continuous Output Current .....Internally Limited
Continuous Power Dissipation (T_A = +70°C)
8-Pin SO (derate 5.9mW/°C above +70°C).....470mW
16-Pin SO (derate 12.9mW/°C above +70°C).....1039mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL SPECIFICATIONS

(V_{IN} = -48V, AGND = DGND = 0, UVLO = open circuit, V_{ENABLE} = +3.3V, and T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}			-65		-16	V
Supply Current	I_{IN}	Measured at AGND at the end of output voltage slew			1.5	2.5	mA
Maximum V_{OUT} Current	$I_{OUT(MAX)}$	V_{OUT} = V_{IN} + 5V	MAX5911	-310	-280	-250	mA
			MAX5912	-457	-415	-373	
DMOS On-Resistance	$R_{DS(ON)}$	MAX5911 I_{OUT} = -225mA, MAX5912 I_{OUT} = -350mA			2.5	4	Ω
V_{OUT} Leakage Current		Measured on V_{OUT} when internal DMOS is shut off				10	µA
ENABLE Low Voltage	V_{IL}	Referenced to DGND				0.8	V
ENABLE High Voltage	V_{IH}	Referenced to DGND		2.0			V
ENABLE High Input Current	I_{IH}	V_{ENABLE} = +3.3V			140	300	µA
ENABLE Low Pulse Width (Note 1)	t_{EPW}			200			ns
$\overline{FAULT}$ Output Low Voltage	V_{OL}	$I_{\overline{FAULT}}$ = 3mA				0.4	V
$\overline{FAULT}$ Output Leakage Current	I_{OH}	$V_{\overline{FAULT}}$ = +3.3V				10	µA
Zero-Current Detection Threshold	IF_{TH}	Decreasing load current		-12	-8	-4	mA
Zero-Current Detection Threshold Hysteresis	IF_{HY}				1.5		mA
Zero-Current Detection Delay (Note 2)	IF_{DEL}			280	350	520	ms
Current-Limit Delay (Note 3)	t_{LIMIT}	V_{OUT} shorted to AGND			10	20	µs
Power-Good Threshold	V_{PG}	$\lvert V_{IN} - V_{OUT} \rvert$, $\lvert V_{IN} - V_{OUT} \rvert$ decreasing		1.95	2.15	2.35	V
Power-Good Hysteresis	PG_{HYS}	% of V_{PG}			5		%

ELECTRICAL SPECIFICATIONS (continued)

(V_{IN} = -48V, AGND = DGND = 0, UVLO = open circuit, V_{ENABLE} = +3.3V, and T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

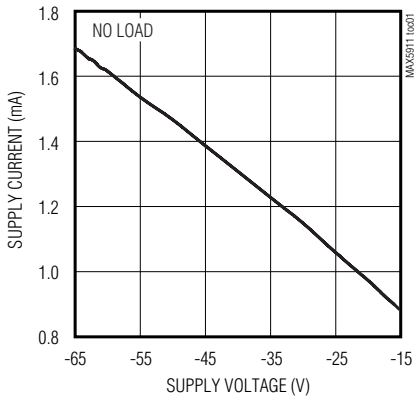
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Not-Good Output Delay (Note 4)	PG_{DEL}	After $\|V_{IN} - V_{OUT}\|$ increases above (V_{PG} + PG_{HYS})	8	14	20	ms
Thermal Shutdown Temperature (Note 5)	T_J			140		°C
Default UVLO		UVLO open circuit, $\|V_{IN}\|$ increasing	-30	-28	-26	V
UVLO Hysteresis		UVLO open circuit, percentage of UVLO threshold		12		%
UVLO Comparator Threshold		Referenced to V_{IN}, UVLO open circuit, $\|V_{IN}\|$ increasing		+1.258		V
UVLO Input Resistance	R_{UVLO}			95		kΩ

Note 1: Minimum ENABLE low pulse width required to unlatch fault condition.
Note 2: The delay from I_{OUT} falling below the zero-current threshold until $\overline{FAULT}$ is latched low and V_{OUT} is disabled.
Note 3: The time from an output overcurrent or short-circuit condition until the output goes into current limit.
Note 4: The time from V_{OUT} falling until $\overline{FAULT}$ is asserted low. $\overline{FAULT}$ is not latched for Power-Not-Good condition.
Note 5: When the device goes into thermal shutdown, the output is disabled and $\overline{FAULT}$ is latched low.

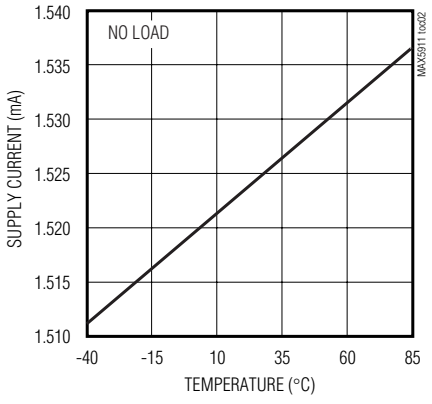
Typical Operating Characteristics

(V_{IN} = -48V, AGND = DGND = 0, UVLO = open circuit, V_{ENABLE} = +3.3V, R_{LOAD} = 1.8kΩ, T_A = +25°C, unless otherwise noted.)

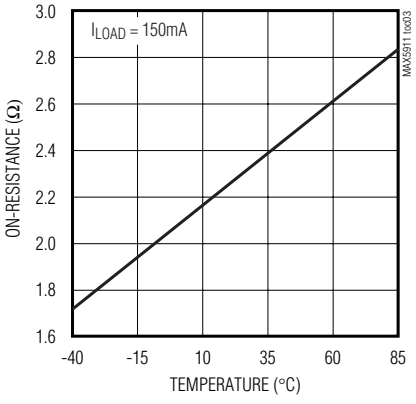
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. AMBIENT TEMPERATURE



ON-RESISTANCE vs. AMBIENT TEMPERATURE

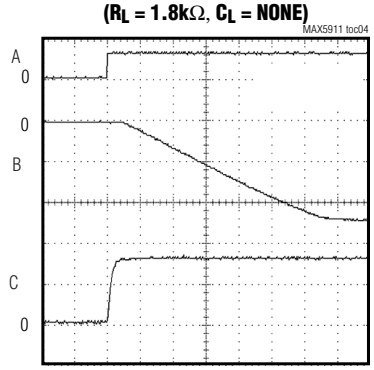


-48V Simple Swapper Hot-Swap Switches

Typical Operating Characteristics (continued)

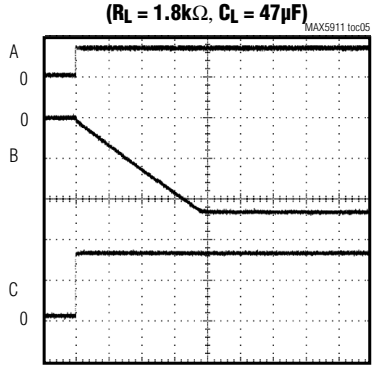
(V_{IN} = -48V, AGND = DGND = 0, UVLO = open circuit, V_{ENABLE} = +3.3V, R_{LOAD} = 1.8kΩ, T_A = +25°C, unless otherwise noted.)

MAX5911 TURN-ON WAVEFORMS
(R_L = 1.8kΩ, C_L = NONE)



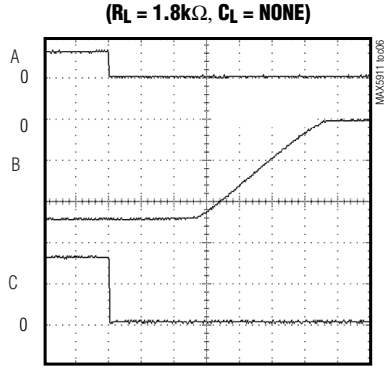
t = 10µs/div
A: ENABLE, 5V/div
C: $\overline{FAULT}$, 2V/div
B: V_{OUT}, 20V/div

MAX5911 TURN-ON WAVEFORMS
(R_L = 1.8kΩ, C_L = 47µF)



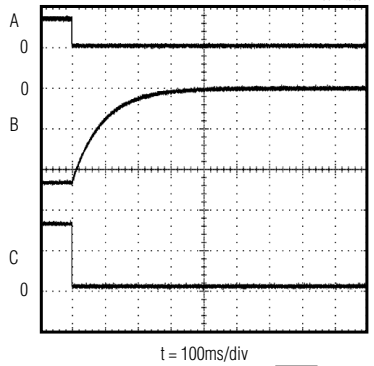
t = 2ms/div
A: ENABLE, 5V/div
C: $\overline{FAULT}$, 2V/div
B: V_{OUT}, 20V/div

MAX5911 TURN-OFF WAVEFORMS
(R_L = 1.8kΩ, C_L = NONE)



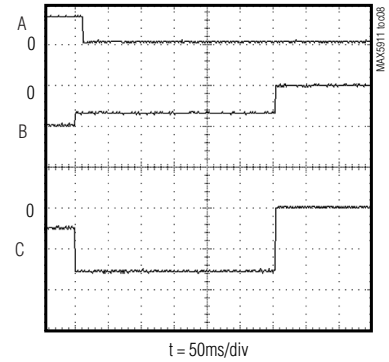
t = 10µs/div
A: ENABLE, 5V/div
C: $\overline{FAULT}$, 2V/div
B: V_{OUT}, 20V/div

MAX5911 TURN-OFF WAVEFORMS
(R_L = 1.8kΩ, C_L = 47µF)



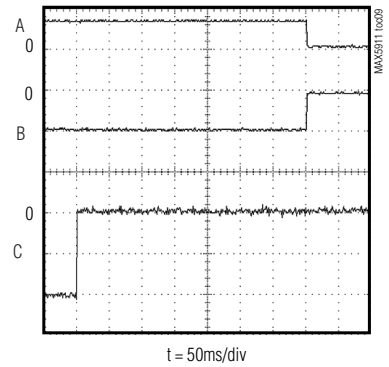
t = 100ms/div
A: ENABLE, 5V/div
C: $\overline{FAULT}$, 2V/div
B: V_{OUT}, 20V/div

MAX5911
OVERCURRENT RESPONSE



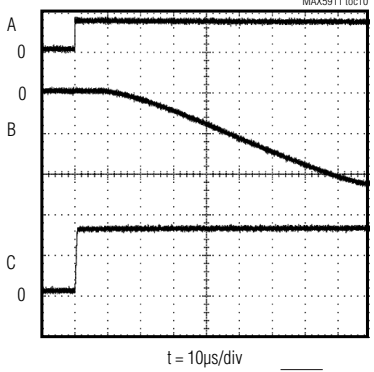
t = 50ms/div
A: $\overline{FAULT}$, 5V/div
C: I_{OUT}, 200mA/div
B: V_{OUT}, 50V/div

MAX5911
ZERO-CURRENT RESPONSE



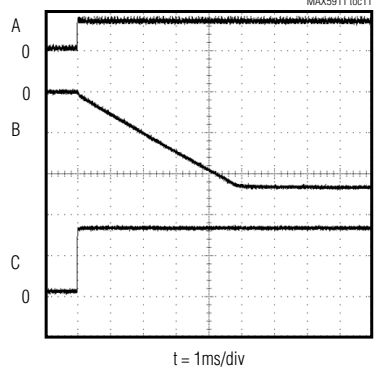
t = 50ms/div
A: $\overline{FAULT}$, 5V/div
C: I_{OUT}, 50mA/div
B: V_{OUT}, 50V/div

MAX5912 TURN-ON WAVEFORMS
(R_L = 1.8kΩ, C_L = NONE)



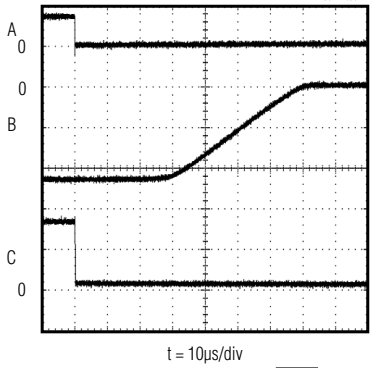
t = 10µs/div
A: ENABLE, 5V/div
C: $\overline{FAULT}$, 2V/div
B: V_{OUT}, 20V/div

MAX5912 TURN-ON WAVEFORMS
(R_L = 1.8kΩ, C_L = 47µF)



t = 1ms/div
A: ENABLE, 5V/div
C: $\overline{FAULT}$, 2V/div
B: V_{OUT}, 20V/div

MAX5912 TURN-OFF WAVEFORMS
(R_L = 1.8kΩ, C_L = NONE)

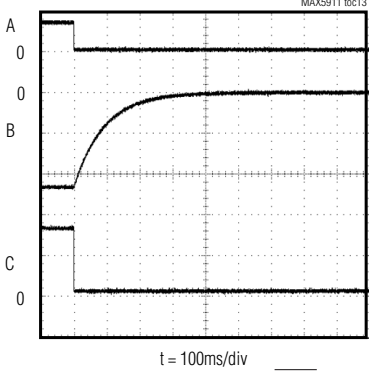


t = 10µs/div
A: ENABLE, 5V/div
C: $\overline{FAULT}$, 2V/div
B: V_{OUT}, 20V/div

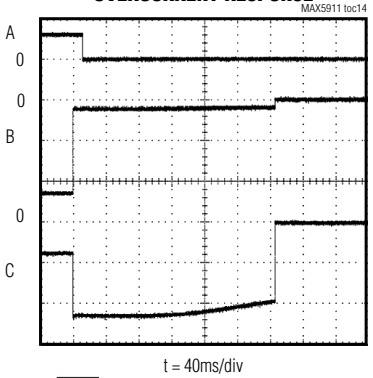
Typical Operating Characteristics (continued)

(V_{IN} = -48V, AGND = DGND = 0, UVLO = open circuit, V_{ENABLE} = +3.3V, R_{LOAD} = 1.8kΩ, T_A = +25°C, unless otherwise noted.)

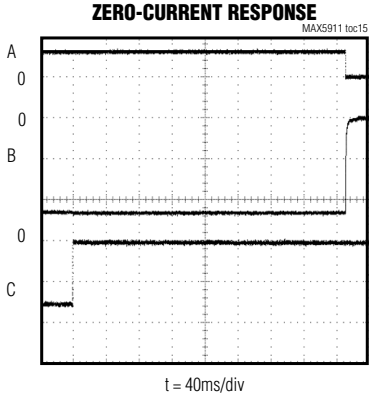
MAX5912 TURN-OFF WAVEFORMS (R_L = 1.8kΩ, C_L = 47µF)



MAX5912 OVERCURRENT RESPONSE



MAX5912 ZERO-CURRENT RESPONSE



Pin Description

PIN		NAME	FUNCTION
MAX5911	MAX5912		
1	3	GATE	Gate of the Internal Power MOSFET. Normally leave open circuit. To slow down the output voltage ramp, connect two capacitors, one to V_{IN} and one to V_{OUT}. See *GATE Connections* for details.
2	4, 5, 12, 13	V_{IN}	Voltage Input Terminal. Bypass V_{IN}, to AGND with a 0.1µF capacitor to improve noise immunity.
3	6	$\overline{FAULT}$	Fault Logic Output, open-drain. Tie $\overline{FAULT}$ to the positive logic supply with a 3.3kΩ resistor. Referenced to DGND.
4	7	DGND	Digital Ground. Ground reference level for the external positive logic, $\overline{FAULT}$, and ENABLE. DGND can vary up to ±5V with respect to AGND to accommodate differential ground voltages in large systems.
5	10	ENABLE	ENABLE Input. Turns on and off the internal FET. ENABLE is a positive logic-level input referenced to DGND. Drive ENABLE high to enable V_{OUT}. Drive ENABLE low to disable V_{OUT}. Pulse ENABLE low to reset the MAX5911/ MAX5912 after a latched fault condition occurs.
6	11	AGND	Analog Ground. Ground reference level for V_{IN}, V_{OUT}, and UVLO.
7	14	V_{OUT}	Voltage Output Terminal
8	15	UVLO	Undervoltage Lockout Input. Leave UVLO open circuit for default setting of -28V. Alternatively, UVLO can be connected to a resistive divider to set the lockout voltage (see the *Changing the Undervoltage Lockout Setting* section). The comparator threshold level is +1.258V with respect to V_{IN}.
—	1, 2, 8, 9, 16	N.C.	No Connection. No internal connection.

-48V Simple Swapper Hot-Swap Switches

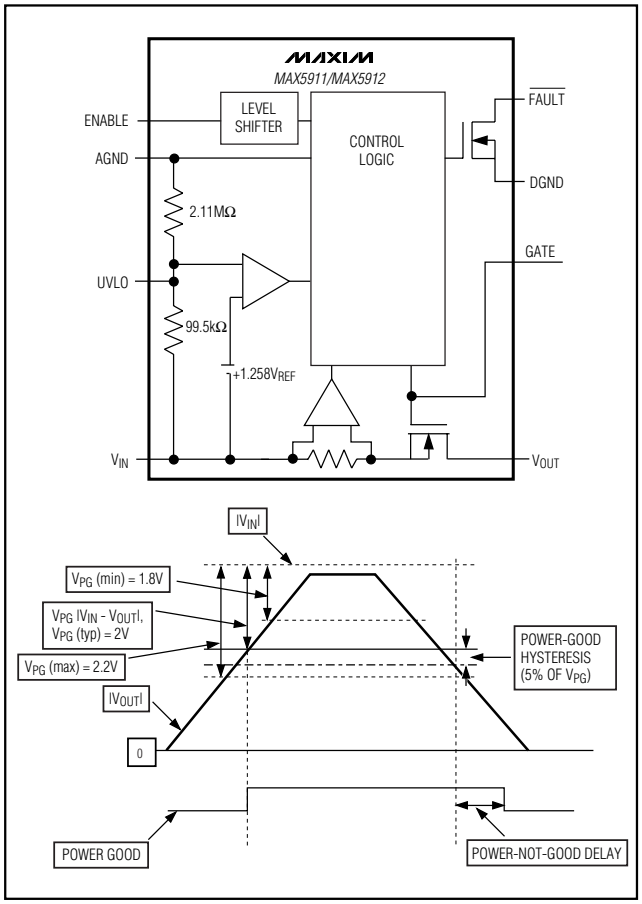


Figure 1. Functional Block Diagram

Detailed Description

Figure 1 shows a functional block diagram. The MAX5911/MAX5912 are hot-swap switches for negative supply rails. The devices allow the safe insertion and removal of circuit cards into live backplanes or ports without causing undue glitches on the negative power-supply rail. They operate over the -16V to -65V voltage range. The devices act as a current regulator, using their on-board FET to limit the amount of current drawn from the backplane to 280mA for MAX5911 and 415mA for MAX5912. If the load current exceeds that current limit, the internal switch behaves like a constant current source.

The MAX5911/MAX5912 monitor the input voltage, the output voltage, the output current, and the die temperature. They assert their $\overline{FAULT}$ output if they detect an error condition.

A zero-current load disconnect feature activates if the load current drops below 8mA for over 350ms. They also include an enable input that responds to positive logic, allowing the host system to turn the FET switch on or off. The enable input is also used to reset the devices after an error condition has latched the output FET off.

Normal Operation

Startup

When power is first applied with ENABLE high, or when ENABLE is asserted, the MAX5911/MAX5912 limit the current to the load to 280mA/415mA. If the output voltage has not reached the power-good threshold within the 14ms power-good delay, $\overline{FAULT}$ is pulled low. $\overline{FAULT}$ stays low until the output voltage exceeds the power-good threshold, at which time it is released and becomes high impedance.

Undervoltage Lockout Fault

If $|V_{IN}| \le |UVLO|$, where UVLO is the desired voltage at which the UVLO fault occurs, $\overline{FAULT}$ is pulled low and the internal FET is turned off. If the condition persists for over 350ms (IF_{DEL}), the FET is latched off. The default UVLO voltage is -28V, but it can be adjusted using an external resistive divider (see the *Changing the Undervoltage Lockout Setting* section). Once the FET is latched off, ENABLE must be pulsed low then brought back high to release $\overline{FAULT}$ and enable V_{OUT}.

Thermal Shutdown Fault

The MAX5911/MAX5912 monitor their internal die temperatures. If the temperature of the die exceeds +140°C, $\overline{FAULT}$ is pulled low and the internal FET is latched off. ENABLE must be pulsed low and then brought high again to reset the FET latch, and release $\overline{FAULT}$, provided the die is below the thermal shutdown temperature by 5°C (typ).

Power-Not-Good Fault

If $|V_{IN} - V_{OUT}|$ is more than the power-good threshold for over 14ms, $\overline{FAULT}$ is pulled low. When the output voltage exceeds the power-good threshold, $\overline{FAULT}$ is released. $\overline{FAULT}$ output is not latched during a power-not-good fault.

Zero-Current Detection

If the load current drops below 8mA for over 350ms, $\overline{FAULT}$ is pulled low and the FET is latched off. ENABLE must be pulsed low and then brought high again to release $\overline{FAULT}$ and enable V_{OUT}.

Applications Information

Chosing A Device

The MAX5911 will output up to 280mA (typ) and the MAX5912 up to 415mA (typ). In applications where high heat is expected, use the MAX5912 for its superior

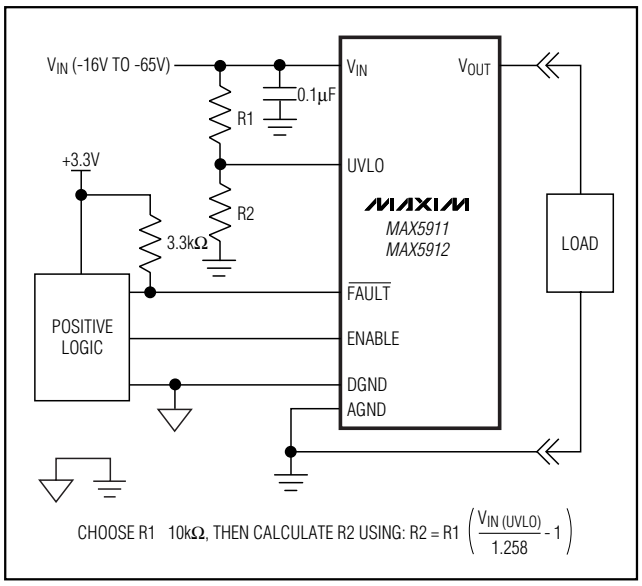


Figure 2. UVLO Voltage Set by an External Resistive Divider

heat dissipation properties, and always solder all of its V_{IN} pins to a large section of circuit board copper.

Logic Control

The enable input responds to +3.3V logic signals and will force the internal FET off if it is pulled low. This feature allows the host to disconnect the load from the power bus if required. Additionally, all fault conditions that latch the internal FET off must be cleared by pulsing ENABLE low for at least 200ns, then reasserting ENABLE before normal operation can resume.

GATE Connections

GATE connects to the gate of the internal N-channel power MOSFET. Normally this pin should be left open circuit. To slow down the voltage ramp at V_{OUT}, connect capacitors from GATE to V_{OUT} and V_{IN}. Size the capacitors so that the GATE to V_{IN} capacitor is ten times the size of the GATE to V_{OUT} capacitor. This technique to slow down the output voltage ramp will also cause the output discharge time to increase if the capacitor values exceed about 1nF. Additionally, this technique will cause the time delay for a power-not-good fault to increase.

$\overline{FAULT}$ Output

The $\overline{FAULT}$ output is open-drain and is pulled low if the MAX5911/MAX5912 detect an undervoltage fault, a thermal fault, a power-not-good fault, or a zero-current fault. See the *Normal Operation* section for specific details of fault operation. Connect $\overline{FAULT}$ to the logic supply with a pullup resistor; 3.3kΩ is sufficient in most cases.

Changing the Undervoltage Lockout Setting

The UVLO value defaults to -28V if the UVLO pin is left open circuit. The lockout voltage can be changed with a resistive divider. Connect the divider from V_{IN} to AGND, and connect the center node of the divider to the UVLO pin. Figure 2 shows an example circuit. Use R1 ≤ 10kΩ, then calculate R2 using:

$$R2 = R1 \times \left(\frac{V_{IN(UVLO)}}{1.258} - 1 \right)$$

where $V_{IN(UVLO)}$ is the desired lockout voltage.

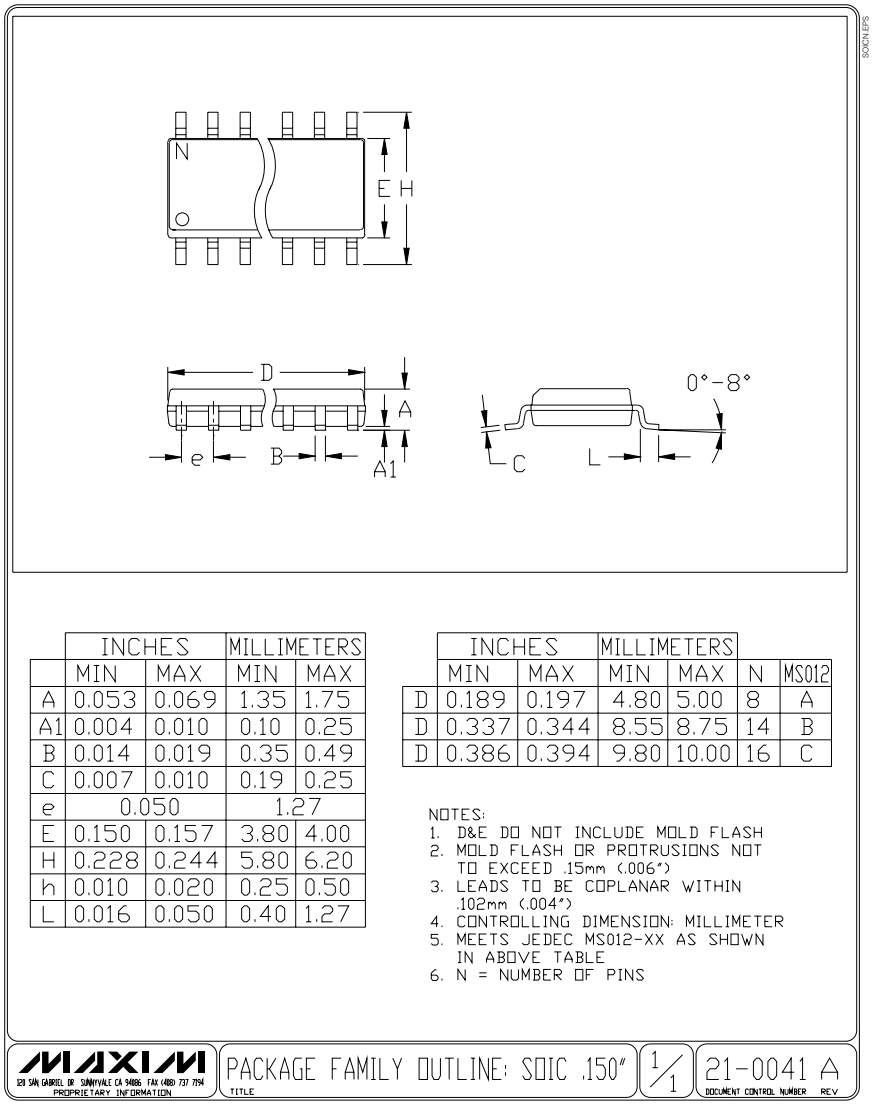
Chip Information

TRANSISTOR COUNT: 1021

PROCESS: BiCMOS

-48V Simple Swapper Hot-Swap Switches

Package Information



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION

PACKAGE FAMILY OUTLINE: SOIC .150" TITLE

1/1

21-0041 A DOCUMENT CONTROL NUMBER REV.