

M61533FP

4ch Electronic Volume with AGC

REJ03F0059-0100Z

Rev.1.0

Sep.19.2003

Features

| Function | Feature |
|---------------------|---|
| Electric Volume | <ul style="list-style-type: none"> 0 to -87dB, $-\infty/1\text{dBstep}$ 4ch SL/SR/C/SW independent Electric Volume Controlled by trim volume data + master volume data. |
| AGC | $V_c=1.8V_{rms}<SWch>$ |
| LPF | Can be set externally <SWch> |
| Output Gain Control | 0, +6, +9, +12dB 4step <SWch> |
| MUC I/F | Controlled by serial data from microcomputer |

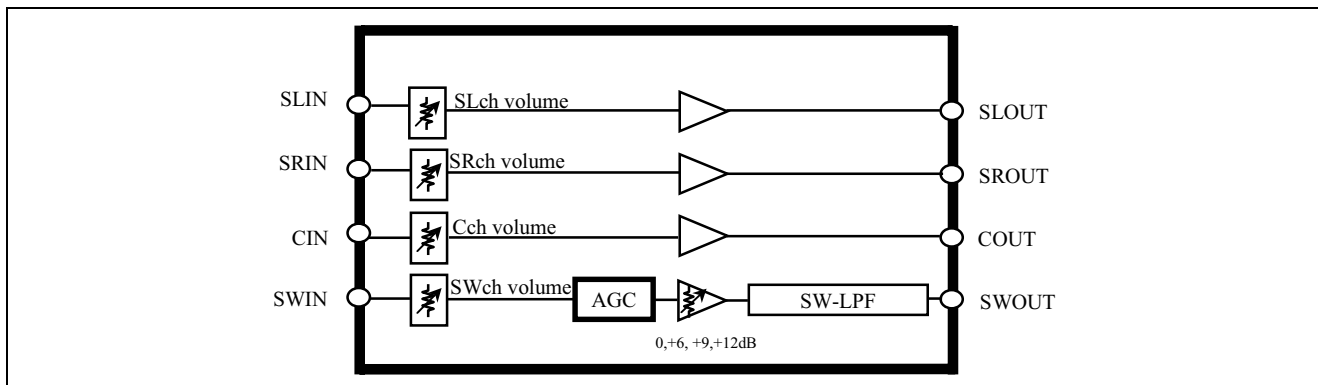
Application

Mini Stereo etc.

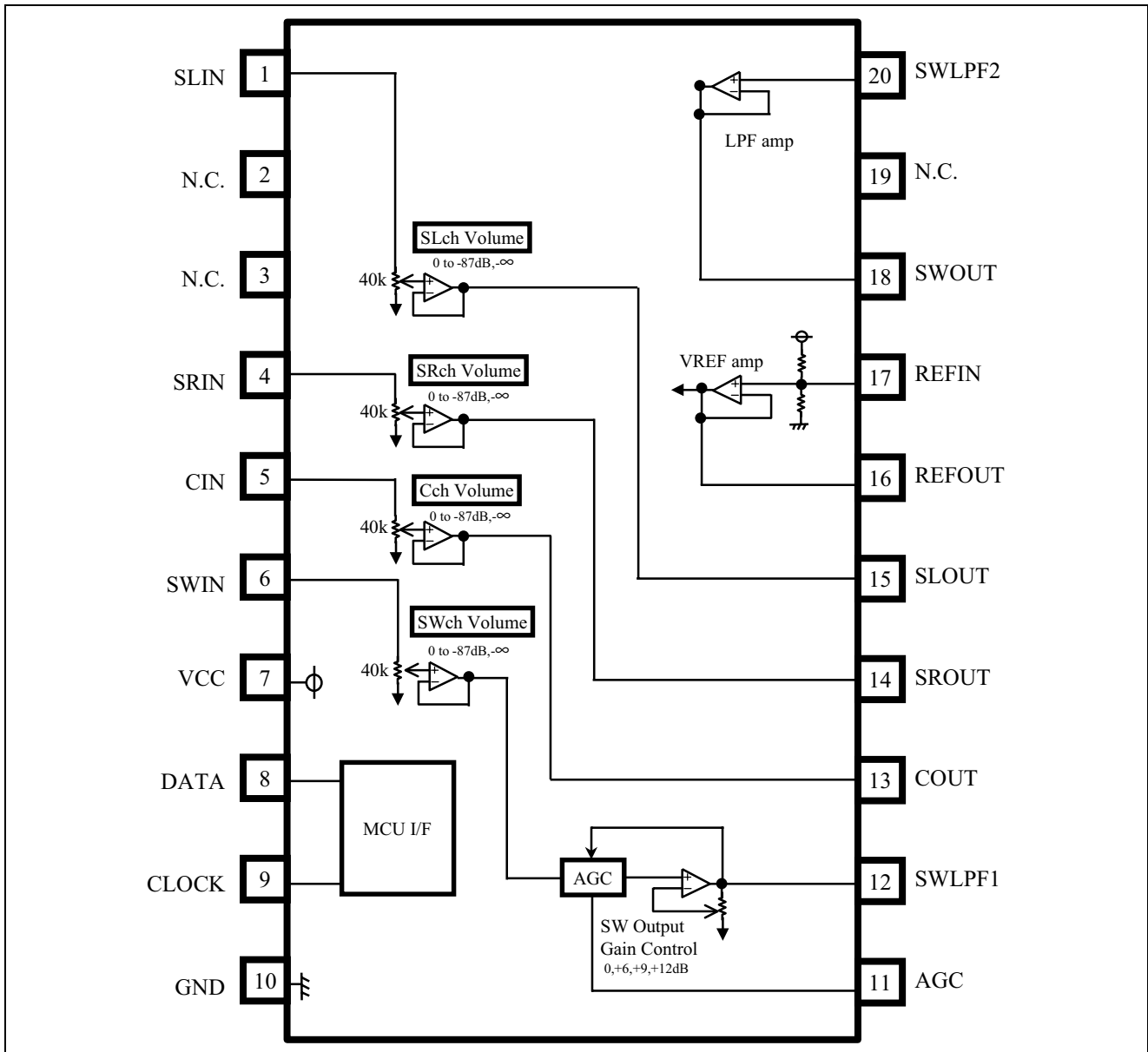
Recommended Operating Condition

Supply Voltage Range VCC= 8 to 10V Typ:VCC=9V

System Block Diagram



Block Diagram and Pin Configuration (Top view)



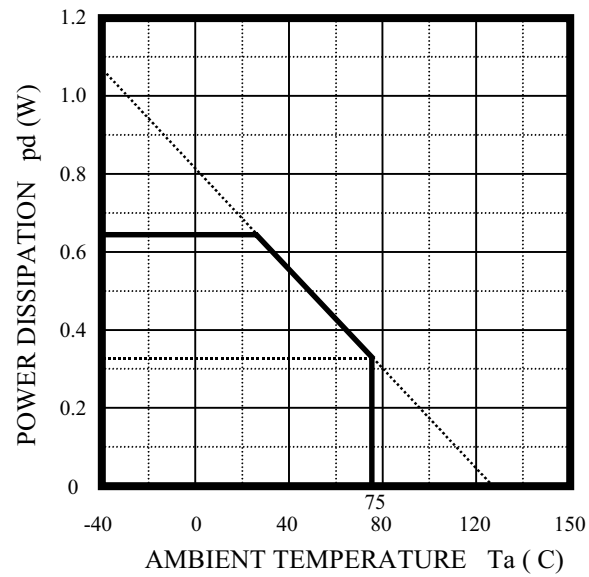
Pin Description

| Pin No. | Name | Function |
|----------------|-------------|--|
| 1 | SLIN | SLch volume input pin |
| 2 | N.C. | N.C. |
| 3 | N.C. | N.C. |
| 4 | SRIN | SRch volume input pin |
| 5 | CIN | Cch volume input pin |
| 6 | SWIN | SWch volume input pin |
| 7 | VCC | Power supply (Typ:9V) |
| 8 | DATA | Input pin of Control data |
| 9 | CLOCK | Input pin of Control clock |
| 10 | GND | Ground |
| 11 | AGC | Attack/Recovery time control pin (by capacitor) |
| 12 | SWLPF1 | SWch LPF (connected with resistance and capacitor) |
| 13 | COUT | Cch output pin |
| 14 | SROUT | SRch output pin |
| 15 | SLOUT | SLch output pin |
| 16 | REFOUT | Vref output pin |
| 17 | REFIN | Vref input pin |
| 18 | SWOUT | SWch output pin |
| 19 | N.C. | N.C. |
| 20 | SWLPF2 | SWch LPF (connected with resistance and capacitor) |

Absolute Maximum Ratings

| Parameter | Symbol | Ratings | Unit | Condition |
|-----------------------|---------------|----------------|-------------|------------------|
| Power Supply | Vcc | 10.5 | V | |
| Power dissipation | Pd | 648 | mW | Ta ≤ 25°C |
| Thermal derating | Kθ | 6.48 | mW/°C | Ta > 25°C |
| Operating temperature | Topr | -20 to 75 | °C | |
| Storage temperature | Tstg | -40 to 125 | °C | |

THERMAL DERATINGS
(MAXIMUM RATING)

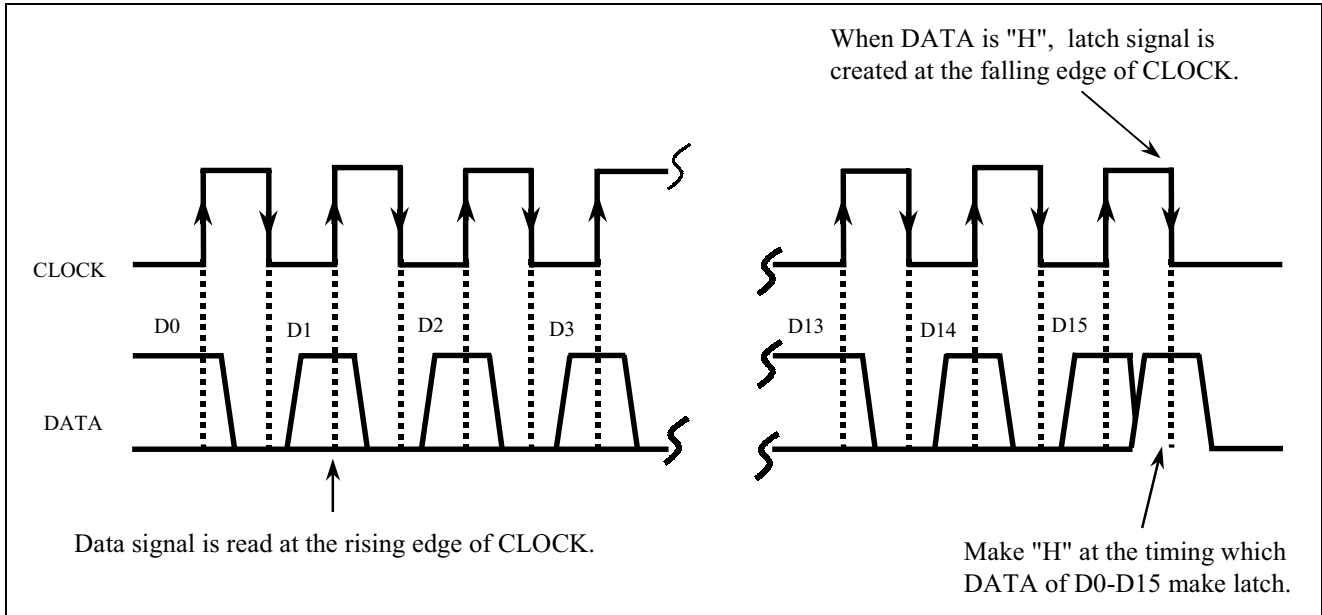


Recommended Conditions

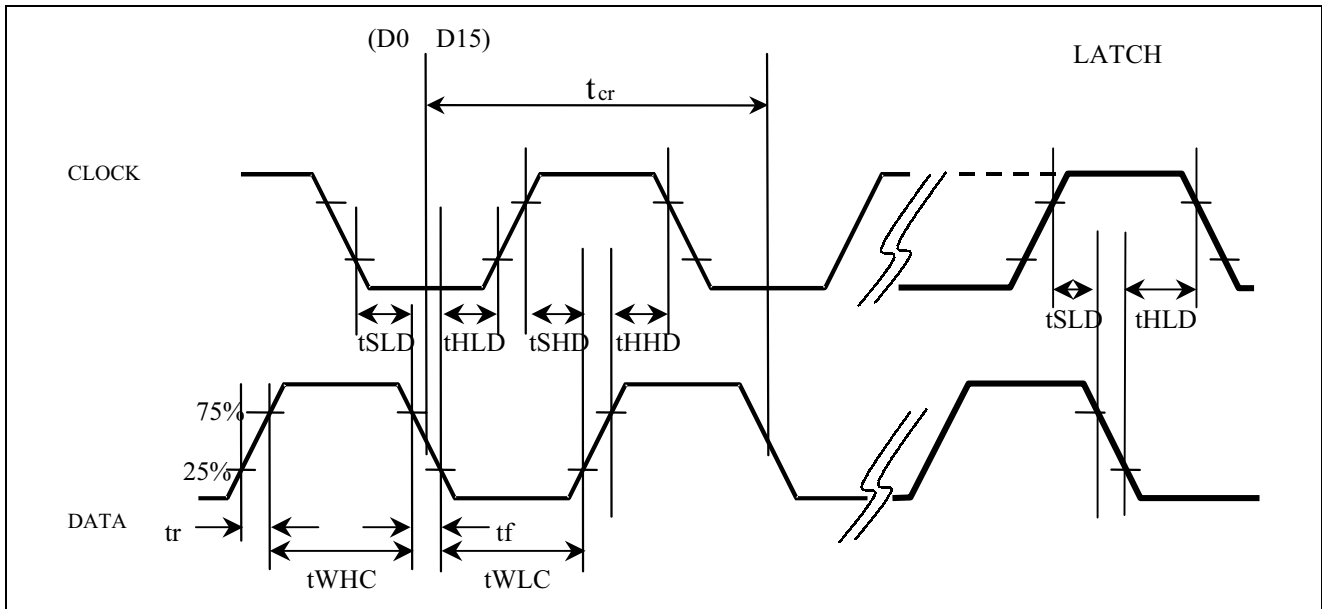
($T_a=25^\circ\text{C}$, Unless otherwise noted)

| Parameter | Symbol | Limits | | | Unit | Conditions |
|-------------------------------|-----------------|--------|------|------|------|--------------------------------------|
| | | Min. | Typ. | Max. | | |
| Power supply | V _{CC} | 8 | 9 | 10 | V | |
| Logic "H" level input voltage | V _{IH} | 2.2 | — | 5.5 | V | V _{CC} =9V GND reference |
| Logic "L" level input voltage | V _{IL} | 0 | — | 0.6 | V | V _{CC} =9V GND reference |

Relationship Between Data and Clock



Clock and Data Timings



Timing Definition of Digital Block

| Parameter | Symbol | Limits | | | Unit |
|---|--------|--------|------|------|------|
| | | Min. | Typ. | Max. | |
| CLOCK cycle time | tcr | 4 | — | — | μs |
| CLOCK pulse width("H" level) | tWHC | 1.6 | — | — | |
| CLOCK pulse width ("L" level) | tWLC | 1.6 | — | — | |
| Rising time of clock and data | tr | — | — | 0.4 | |
| Falling time of clock and data | tf | — | — | 0.4 | |
| DATA setup time (Rising time of clock) | tSHD | 0.8 | — | — | |
| DATA setup time (Falling time of clock) | tSLD | 0.8 | — | — | |
| DATA hold time("H" level) | tHHD | 0.8 | — | — | |
| DATA hold time("L" level) | tHLD | 0.8 | — | — | |

Data Control Specification

Four types of input format can be selected by changing the D14/D15 slot setting status.

(Initialize all data of the 4 formats when power supply(VCC) turn on.)

Note : No guarantee except for these code.

- (1)
- | D0a | D1a | D2a | D3a | D4a | D5a | D6a | D7a | D8a | D9a | D10a | D11a | D12a | D13a | D14 | D15 |
|-----------------------|-----|-----|-----|-----------------------|-----|-----|-----|-----|-----|------|------|------|------|-----|-----|
| ② SLch Trim volume | | | | ② SRch Trim volume | | | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
- (2)
- | D0b | D1b | D2b | D3b | D4b | D5b | D6b | D7b | D8b | D9b | D10b | D11b | D12b | D13b | D14 | D15 |
|----------------------|-----|-----|-----|-----------------------|-----|-----|-----|-----|-------------------------------------|------|------|------|------|-----|-----|
| ② Cch Trim volume | | | | ② SWch Trim volume | | | | 1 | ① SWch Output gain control | 0 | 0 | 0 | 0 | 0 | 1 |
- (3)
- | D0c | D1c | D2c | D3c | D4c | D5c | D6c | D7c | D8c | D9c | D10c | D11c | D12c | D13c | D14 | D15 |
|-------------------------|-----|-----|-----|-------------------------|-----|-----|-----|-----|-----|------|------|------|------|-----|-----|
| ③ SLch Master volume | | | | ③ SRch Master volume | | | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | |
- (4)
- | D0d | D1d | D2d | D3d | D4d | D5d | D6d | D7d | D8d | D9d | D10d | D11d | D12d | D13d | D14 | D15 |
|------------------------|-----|-----|-----|-------------------------|-----|-----|-----|-----|-----|------|------|------|------|-----|-----|
| ③ Cch Master volume | | | | ③ SWch Master volume | | | | 0 | 0 | 0 | 0 | 0 | 1 | 1 | |

Setting Code

It's initial setting when VCC turn on.

① SWch Output gain control

| | D9b | D10b |
|-------|-----|------|
| 0dB | 0 | 0 |
| +6dB | 0 | 1 |
| +9dB | 1 | 0 |
| +12dB | 1 | 1 |

② SL/SR/C/SWch Trim volume

| ATT | SLch | D0a | D1a | D2a | D3a |
|-------|------|-----|-----|-----|-----|
| | SRch | D4a | D5a | D6a | D7a |
| | Cch | D0b | D1b | D2b | D3b |
| | SWch | D4b | D5b | D6b | D7b |
| | | | | | |
| 0dB | 0 | 0 | 0 | 0 | |
| -1dB | 0 | 0 | 0 | 1 | |
| -2dB | 0 | 0 | 1 | 0 | |
| -3dB | 0 | 0 | 1 | 1 | |
| -4dB | 0 | 1 | 0 | 0 | |
| -5dB | 0 | 1 | 0 | 1 | |
| -6dB | 0 | 1 | 1 | 0 | |
| -7dB | 0 | 1 | 1 | 1 | |
| -8dB | 1 | 0 | 0 | 0 | |
| -9dB | 1 | 0 | 0 | 1 | |
| -10dB | 1 | 0 | 1 | 0 | |
| -11dB | 1 | 0 | 1 | 1 | |
| -12dB | 1 | 1 | 0 | 0 | |
| -13dB | 1 | 1 | 0 | 1 | |
| -14dB | 1 | 1 | 1 | 0 | |
| -15dB | 1 | 1 | 1 | 1 | |

③ SL/SR/C/SWch Master volume

| ATT | SLch | D0c | D1c | D2c | D3c | D4c |
|-------|------|-----|-----|-----|-----|-----|
| | SRch | D5c | D6c | D7c | D8c | D9c |
| | Cch | D0d | D1d | D2d | D3d | D4d |
| | SWch | D5d | D6d | D7d | D8d | D9d |
| | | | | | | |
| 0dB | 0 | 0 | 0 | 0 | 0 | |
| -2dB | 0 | 0 | 0 | 0 | 1 | |
| -4dB | 0 | 0 | 0 | 1 | 0 | |
| -6dB | 0 | 0 | 0 | 1 | 1 | |
| -8dB | 0 | 0 | 1 | 0 | 0 | |
| -10dB | 0 | 0 | 1 | 0 | 1 | |
| -12dB | 0 | 0 | 1 | 1 | 0 | |
| -14dB | 0 | 0 | 1 | 1 | 1 | |
| -16dB | 0 | 1 | 0 | 0 | 0 | |
| -18dB | 0 | 1 | 0 | 0 | 1 | |
| -20dB | 0 | 1 | 0 | 1 | 0 | |
| -22dB | 0 | 1 | 0 | 1 | 1 | |
| -24dB | 0 | 1 | 1 | 0 | 0 | |
| -26dB | 0 | 1 | 1 | 0 | 1 | |
| -28dB | 0 | 1 | 1 | 1 | 0 | |
| -30dB | 0 | 1 | 1 | 1 | 1 | |
| -32dB | 1 | 0 | 0 | 0 | 0 | |
| -34dB | 1 | 0 | 0 | 0 | 1 | |
| -36dB | 1 | 0 | 0 | 1 | 0 | |
| -38dB | 1 | 0 | 0 | 1 | 1 | |
| -40dB | 1 | 0 | 1 | 0 | 0 | |
| -42dB | 1 | 0 | 1 | 0 | 1 | |
| -44dB | 1 | 0 | 1 | 1 | 0 | |
| -48dB | 1 | 0 | 1 | 1 | 1 | |
| -52dB | 1 | 1 | 0 | 0 | 0 | |
| -56dB | 1 | 1 | 0 | 0 | 1 | |
| -60dB | 1 | 1 | 0 | 1 | 0 | |
| -64dB | 1 | 1 | 0 | 1 | 1 | |
| -68dB | 1 | 1 | 1 | 0 | 0 | |
| -72dB | 1 | 1 | 1 | 0 | 1 | |
| -76dB | 1 | 1 | 1 | 1 | 0 | |
| -∞ dB | 1 | 1 | 1 | 1 | 1 | |

Note1: Volume ATT controlled by trim volume data + master volume data.

Note2: When trim volume data + master volume data is under -87dB setting, volume ATT keep -87dB.

ex) When trim volume data:-15dB / master volume data -76dB setting, volume ATT keep -87dB.

Electrical characteristics

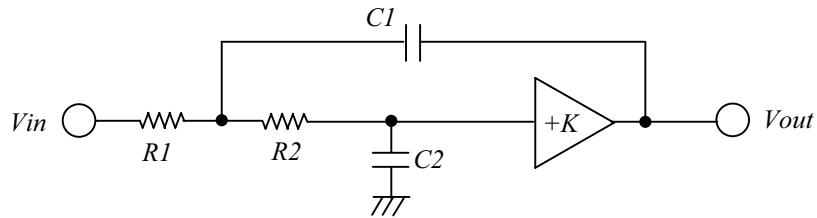
Unless otherwise noted, Ta=25°C, Vcc=9V, f=1kHz, Trim/Master Volume=0dB, Output Gain Control=0dB, SWch LPF fc=300Hz

| Parameter | Symbol | Limits | | | Unit | Test conditions | |
|-----------------------------|--------|--------|-------|------|-------|---|------------------------|
| | | Min. | Typ. | Max. | | | |
| Power circuit current | IACC | — | 15 | 30 | mA | when no signal is provided | |
| Input/output | | | | | | | |
| Maximum input voltage | VIM | — | — | 2.0* | Vrms | (1,4,5,6)PIN input, (13,14,15,18)PIN output, RL=10kΩ, THD=1% | |
| Maximum output voltage | VOM1 | 1.4 | 1.8 | — | Vrms | 6PIN input, 18PIN output, RL=10kΩ, THD=5%, f=100Hz | |
| | VOM2 | 1.6 | 2.0 | — | Vrms | (1,4,5)PIN input, (13,14,15)output, RL=10kΩ, THD=5% | |
| Pass gain | GV | -2 | 0 | +2 | dB | (1,4,5,6)PIN input, (13,14,15,18) output, Vi=0.5Vrms, FLAT | |
| Output noise voltage | Vno1 | — | 1.3 | 4.0 | μVrms | JIS-A, when no signal is provided, (1,4,5)PIN Rg=0 Ω, (13,14,15)PIN output | SL/SR/Cch volume =0dB |
| | | — | 1.3 | 4.0 | μVrms | | SL/SR/Cch volume =-∞dB |
| | Vno2 | — | 8.0 | 16 | μVrms | JIS-A, when no signal is provided, 6PIN Rg=0 Ω, 18PIN output, | SWch volume =0dB |
| | | — | 8.0 | 16 | μVrms | | SWch volume =-∞dB |
| Distortion | THD1 | — | 0.005 | 0.1 | % | (1,4,5)PIN input, (13,14,15)output, BW:400 30kHz, Vo=0.5Vrms, RL=10kΩ | |
| | THD2 | — | 0.05 | 0.2 | % | 6PIN input, 12PIN output, 30kHz L.P.F, f=100Hz, Output Gain Control =0dB, Vi=0.5Vrms(AGC:off), RL=10kΩ | |
| | THD3 | — | 5 | — | % | 6PIN input, 12PIN output, 30kHz L.P.F, f=100Hz, Output Gain Control =+12dB, Vi=0.7Vrms(AGC:on), RL=10kΩ | |
| Maximum attenuation | ATT | — | -92 | -87 | dB | Vo=1Vrms, (12,13,14,15) PIN output, JIS-A, VOL=-∞ | |
| Maximum gain | GVM | +10 | +12 | +14 | dB | 6PIN input, 12PIN output, f=100Hz, Vi=0.1Vrms, FLAT, Output Gain Control =+12dB | |
| Cross talk between channels | CT | — | -70 | -55 | dB | (1,4,5,6)PIN input, (12,13,14,15)PIN output, Vi=0.5Vrms, JIS-A, RL=47kΩ, Rg=0kΩ | |
| AGC | | | | | | | |
| Attack time | TAGCAT | — | 40 | — | ms | 6PIN input, 12PIN output, RL=10kΩ, Output Gain Control =+12dB | |
| Recovery time | TAGCRE | — | 850 | — | ms | 6PIN input, 12PIN output, RL=10kΩ, Output Gain Control =+12dB | |

* Note : The signal can not be inputted to more than 2Vrms. Keep this limit.

LPF

Equivalent circuit of LPF



$$F(s) = \frac{V_{out}}{V_{in}} = \frac{\frac{1}{R_1 R_2 C_1 C_2} K}{s^2 + \left[\frac{1}{R_1 C_1} + \frac{1}{R_2 C_1} + (1-K) \frac{1}{R_2 C_2} \right] s + \frac{1}{R_1 R_2 C_1 C_2}}$$

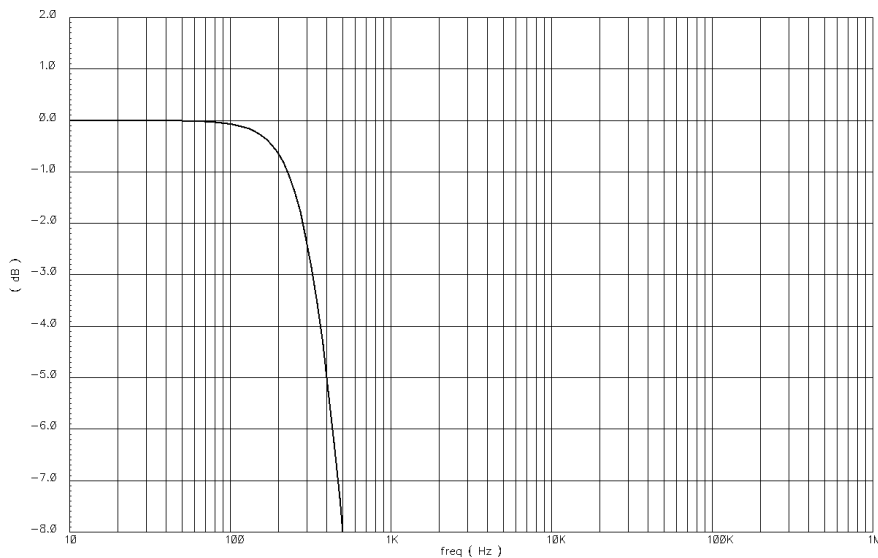
$$\omega_0 = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}} \quad Q = \frac{1}{\sqrt{\frac{R_2 C_2}{R_1 C_1}} + \sqrt{\frac{R_1 C_2}{R_2 C_1}} + (1-K) \sqrt{\frac{R_1 C_1}{R_2 C_2}}}$$

Frequency characteristics (SWch LPF)

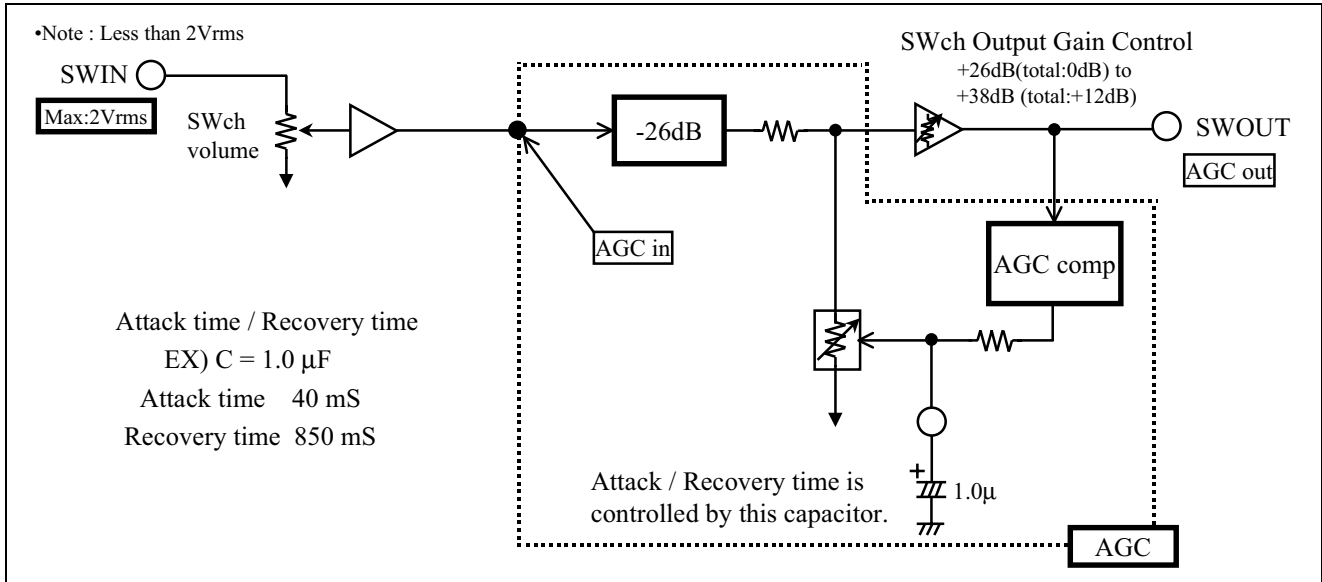
$R_1=2.2\text{k}\Omega$, $R_2=4.7\text{k}\Omega$, $C_1=0.22\mu\text{F}$, $C_2=0.1\mu\text{F}$, $K=1$

$Q \approx 0.68$, $f_c \approx 300\text{Hz}$

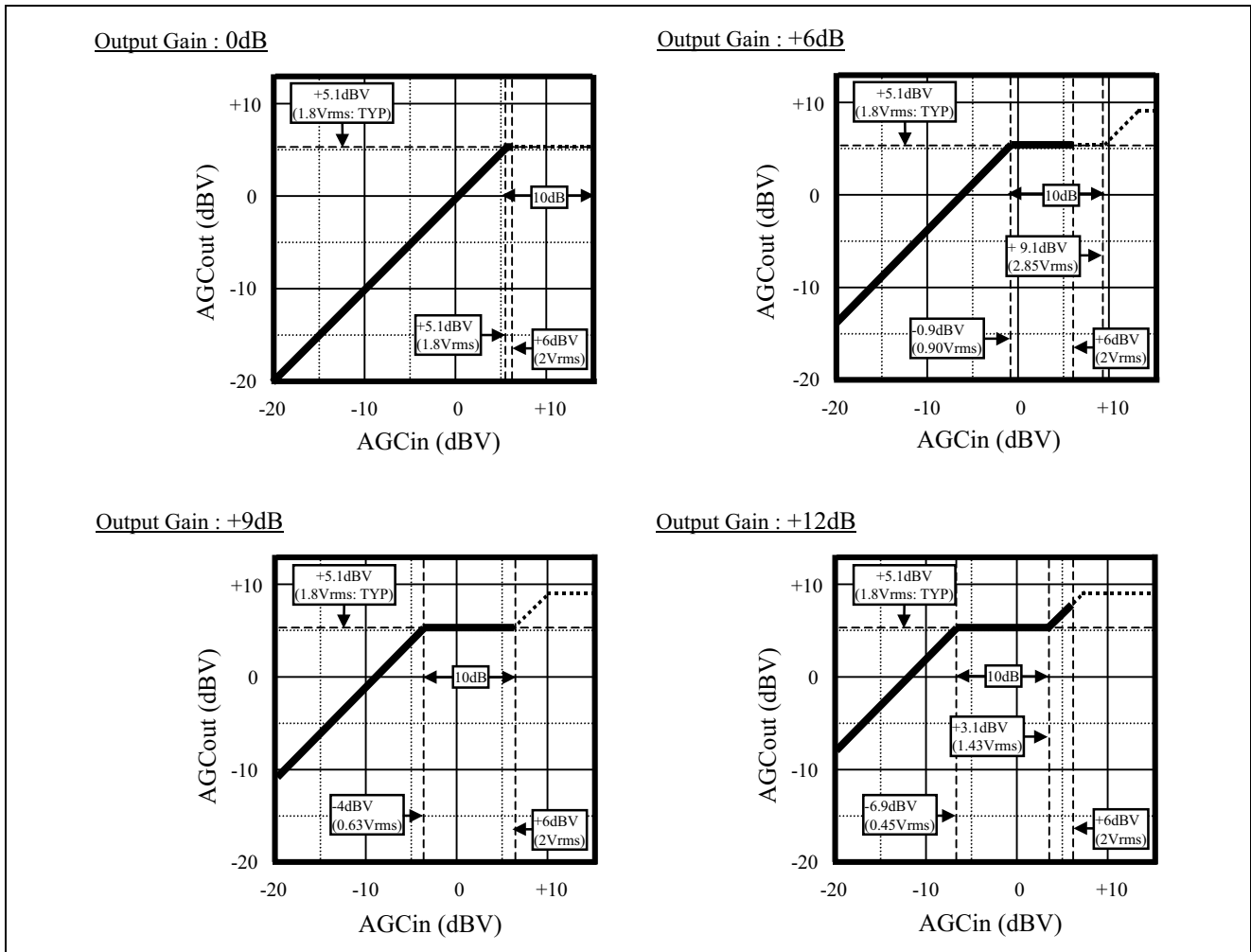
*This frequency response is a simulation result.



AGC

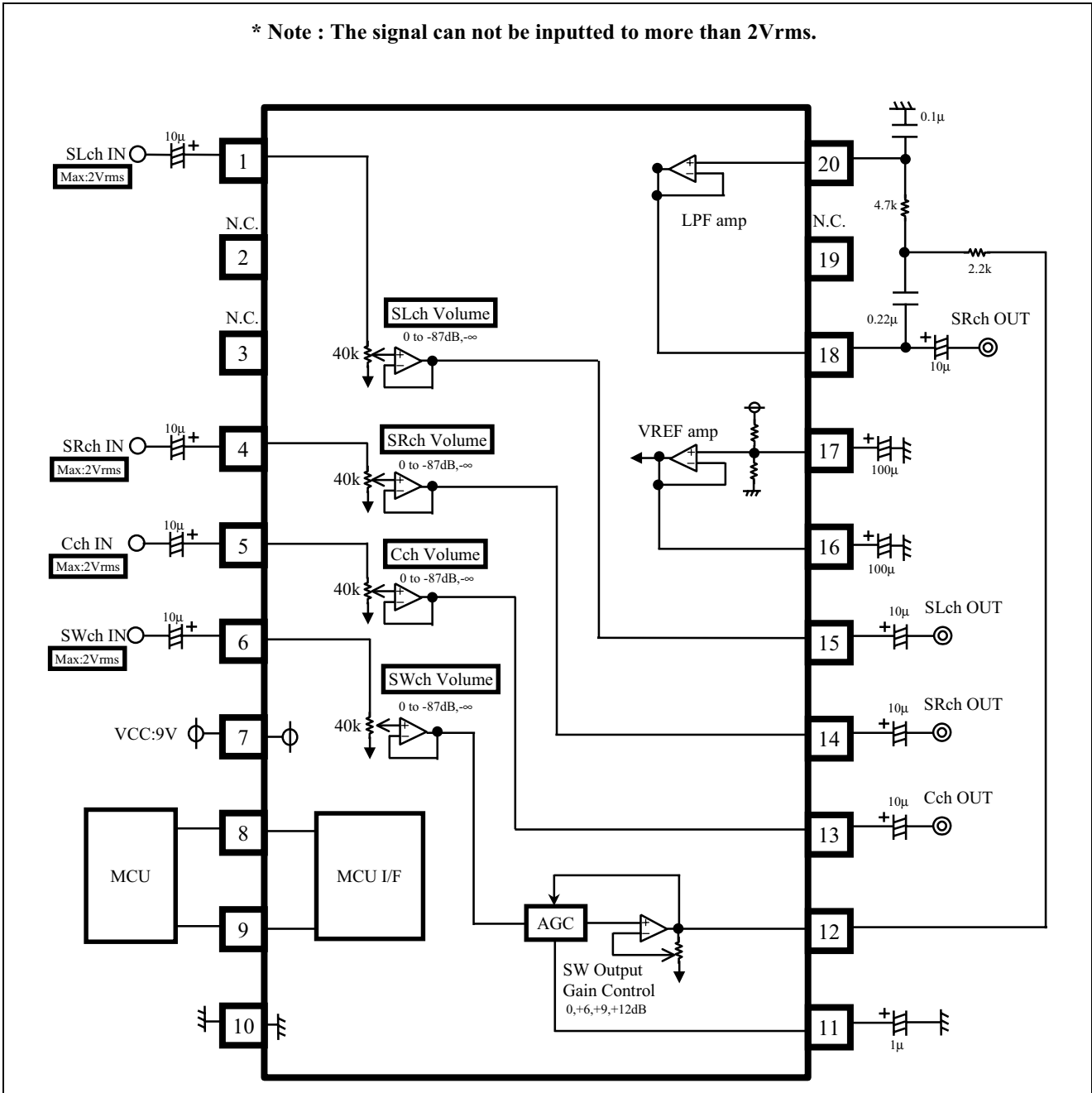


AGC characteristics



Application Example

* Note : The signal can not be inputted to more than 2Vrms.

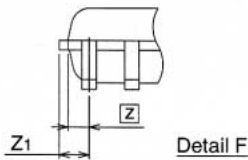
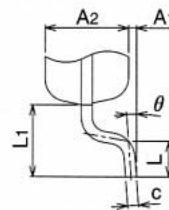
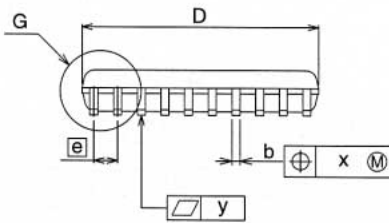
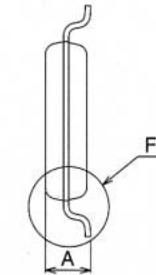
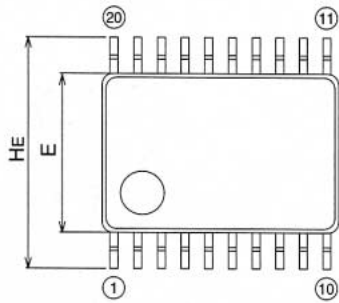


Package Dimensions

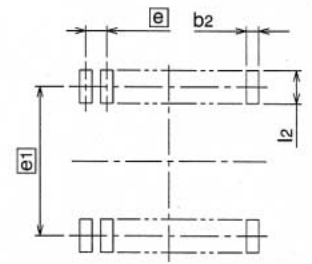
20P2F-A (MMP)

Plastic 20pin 255mil SSOP

| | | | |
|-------------------|------------|-----------|---------------|
| EIAJ Package Code | JEDEC Code | Weight(g) | Lead Material |
| SSOP20-P-255-0.65 | - | - | Cu Alloy |



Detail F



Recommended Mount Pad

| Symbol | Dimension in Millimeters | | |
|--------|--------------------------|-------|-------|
| | Min | Nom | Max |
| A | - | - | 1.45 |
| A1 | 0 | 0.1 | 0.2 |
| A2 | - | 1.15 | - |
| b | 0.17 | 0.22 | 0.32 |
| c | 0.13 | 0.15 | 0.2 |
| D | 6.4 | 6.5 | 6.6 |
| E | 4.3 | 4.4 | 4.5 |
| e | - | 0.65 | - |
| HE | 6.2 | 6.4 | 6.6 |
| L | 0.3 | 0.5 | 0.7 |
| L1 | - | 1.0 | - |
| Z | - | 0.325 | - |
| Z1 | - | - | 0.475 |
| x | - | - | 0.13 |
| y | - | - | 0.1 |
| theta | 0° | - | 10° |
| b2 | - | 0.35 | - |
| e1 | - | 5.8 | - |
| l2 | 1.0 | - | - |

RENESAS Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
 2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
 3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
 4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
 5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
 6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
 7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
 8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.
-



RENESAS SALES OFFICES

<http://www.renesas.com>

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

Renesas Technology Europe Limited.
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

Renesas Technology Europe GmbH
Dornacher Str. 3, D-85622 Feldkirchen, Germany
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

Renesas Technology Hong Kong Ltd.
7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2375-6836

Renesas Technology Taiwan Co., Ltd.
FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001