32-Channel 256 Gray-Shade High Voltage Driver

Ordering Information

Device	Package Option	
	64-Lead 3-Sided Plastic Gullwing	Die
HV62208	HV62208PG	HV62208X

Features

- ❑ HVCMOS® technology
- ❑ 5V CMOS inputs
- ❑ Up to 80V output voltage
- ❑ PWM gray shade conversion
- ❑ Capable of 256 levels of gray shading
- ❑ Balanced shift clock complies with RS-422
- ❑ 8MHz shift and count clock frequency
- ❑ 16MHz data throughput rate
- ❑ 8 bit data bus
- ❑ 32 outputs per device
- ❑ BLANK function

Absolute Maximum Ratings

Supply voltage, V_{DD}	-0.5V to +7.5V
Supply voltage, V_{PP}	-0.5V to +80V
Supply voltage, V_{NN}	-15V to 0V
Logic input levels	-0.5 to V_{DD} + 0.5V
Continuous total power dissipation	1.2W
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C

Notes:
All voltages are referenced to GND.
Maximum V_{PP} to V_{NN} voltage is 90V.
For operation above 25°C ambient derate linearly to 85°C at 20mW/°C.

General Description

Not recommended for new designs. Please use HV632 instead.

The HV622 is a 32-channel gray-shade column driver IC designed for driving electrofluorescent displays. Using Supertex's unique HVCMOS® technology, it is capable of 256 levels of gray shading by PWM conversion.

The shift clock is a balanced clock with electrical characteristics complying with EIA RS-422 standard. Input data, in groups of eight, is latched into a set of data latches on both edges of the shift clock. The data shifted in the first data latch corresponds to $HV_{OUT}1$, the second data latch corresponds to $HV_{OUT}2$, and so on. These data are compared to the contents of the master binary counter which counts on both edges of the count clock. Each time the master counter begins to decrement from 1111 1111, the data in the data latches are compared with the contents of the counter; if they match, the corresponding outputs will go high. The master counter counts down to 0000 0001 and then starts to count up again. The outputs that are at high will stay at high until the contents of the counter match the data in the data latches again. Therefore, the higher the binary data in the data latches, the longer the outputs will stay at high. Thus, different high voltage pulse widths are produced. When the counter reaches its 1111 1111 count while counting up, the device is ready for the next operation cycle. A data value of 0000 0000 produces no pulse; the output stays low.

The BLANK input signal will reset the master counter to all ones (1111 1111) and set all high voltage outputs to low.

Electrical Characteristics

(Over recommended conditions of V_{DD} = 5V, V_{PP} = 70V, V_{NN} = -10V, T_A = 25°C unless otherwise noted)

Low-Voltage DC Characteristics (Digital)

Symbol	Parameter	Min	Max	Units	Conditions
V_{DD}	Low-voltage digital supply voltage	4.5	5.5	V	
I_{DD}	V_{DD} supply current		25	mA	f_{SC} = 8MHz, f_{CC} = 8MHz
I_{DDQ}	Quiescent V_{DD} supply current		100	μA	All V_{IN} = GND, Count Clock = V_{DD}
I_{IH}	High-level input current		10	μA	V_{IN} = V_{DD}
I_{IL}	Low-level input current		-10	μA	V_{IL} = GND
I_{OH}	High-level output current	-1.0		mA	
I_{OL}	Low-level ouptut current	1.0		mA	

Low-Voltage DC Characteristics (Analog)

Symbol	Parameter	Min	Max	Units	Conditions
V_{DD}	Low-voltage analog supply voltage	4.5	5.5	V	
I_{DD}	V_{DD} supply current		100	μA	f_{SC} = 8MHz, f_{CC} = 8MHz
I_{DDQ}	Quiescent V_{DD} supply current		100	μA	All V_{IN} = GND, Count Clock = V_{DD}

High-Voltage DC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
I_{PPQ}	Quiescent V_{PP} supply current		100	μA	All HV_{OUT} low or high
$I_{OUT(p)}$	P-channel output current	-4.0		mA	
$I_{OUT(n)}$	N-channel output current	4.0		mA	

AC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
f_{SC}	Shift clock frequency		8.0	MHz	
f_{CC}	Count clock frequency		8.0	MHz	
f_{DIN}	Data In frequency		16	MHz	
t_{CW}	Chip select pulse width	80		ns	
t_{CSS}	Chip select to shift clock set-up time	15		ns	
t_{CSH}	Chip select to shift clock hold time	45		ns	
t_{SCC}	Shift clock cycle time	125		ns	
t_{DSS}	Data to shift clock set-up time	10		ns	
t_{DSH}	Data to shift clock hold time	52		ns	
t_{DW}	Data In pulse width	62		ns	
t_{LCW}	Load count pulse width	75		ns	
t_{CCW}	Count clock pulse width	62.5		ns	
t_{CCC}	Count clock cycle time	125		ns	
t_{LCD}	Load count to count clock delay	100		ns	
t_{CCD}	Count clock to HV_{OUT} turn-on/turn-off		600	ns	C_L = 15pF
t_{BLW}	BLANK pulse width	700		ns	
t_{BLD}	BLANK to HV_{OUT} delay		500	ns	C_L = 15pF
t_{CDD}	Count clock delay between count down and count up cycles	500		ns	

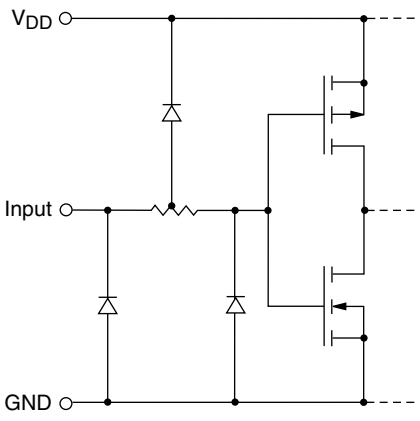
Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units	Conditions
V_{DD}	Logic supply voltage	4.5	5.5	V	
V_{PP}	Positive high-voltage supply	12	70	V	
V_{NN}	Negative high-voltage supply	-8	-10	V	
V_{IL}	Low-level input voltage	0	1	V	
V_{IH}	High-level input voltage	V_{DD}–1	V_{DD}	V	
f_{SC}	Shift clock frequency		8	MHz	
f_{CC}	Count clock frequency		8	MHz	
T_A	Operating temperature	-40	+85	°C	

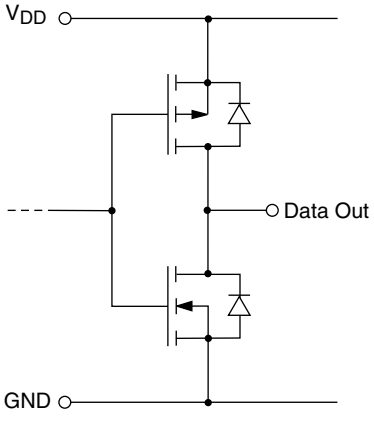
Pin Definitions

Pin #	Name	I/O	Function
27-30 36-29	D1 – D8	I	Inputs for binary-format parallel data (D8 is the most significant bit)
34	Shift Clock	I	Triggers data on both edges
35	$\overline{\text{Shift Clock}}$	I	Triggers data on both edges
31	Count Clock	I	Input to the counter
24	CSI	I	Chip select input to enable the device to accept data
25	CSO	O	Chip select output to enable the next device
33	Load Count	I	Input to initiate the counting
26	Blank	I	Input to reset the counter and HV_{OUT}
4-19 46-61	$HV_{OUT}1$ – $HV_{OUT}32$	O	High-voltage outputs
23,43	V_{PP}	—	Positive high-voltage supply
41	V_{DD} (Analog)	—	Low-voltage analog supply voltage
40	V_{DD} (Digital)	—	Low-voltage digital supply voltage
22,44	V_{NN}	—	Negative high-voltage supply
20-21	GND (Digital)	—	Digital ground
42	GND (Analog)		Analog ground

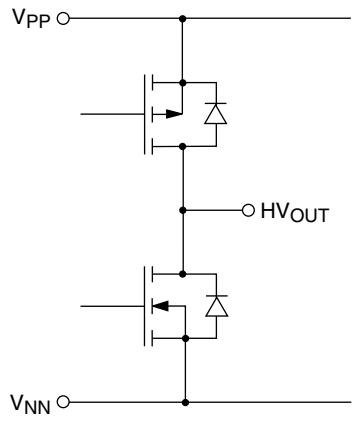
Input and Output Equivalent Circuits



Logic Inputs

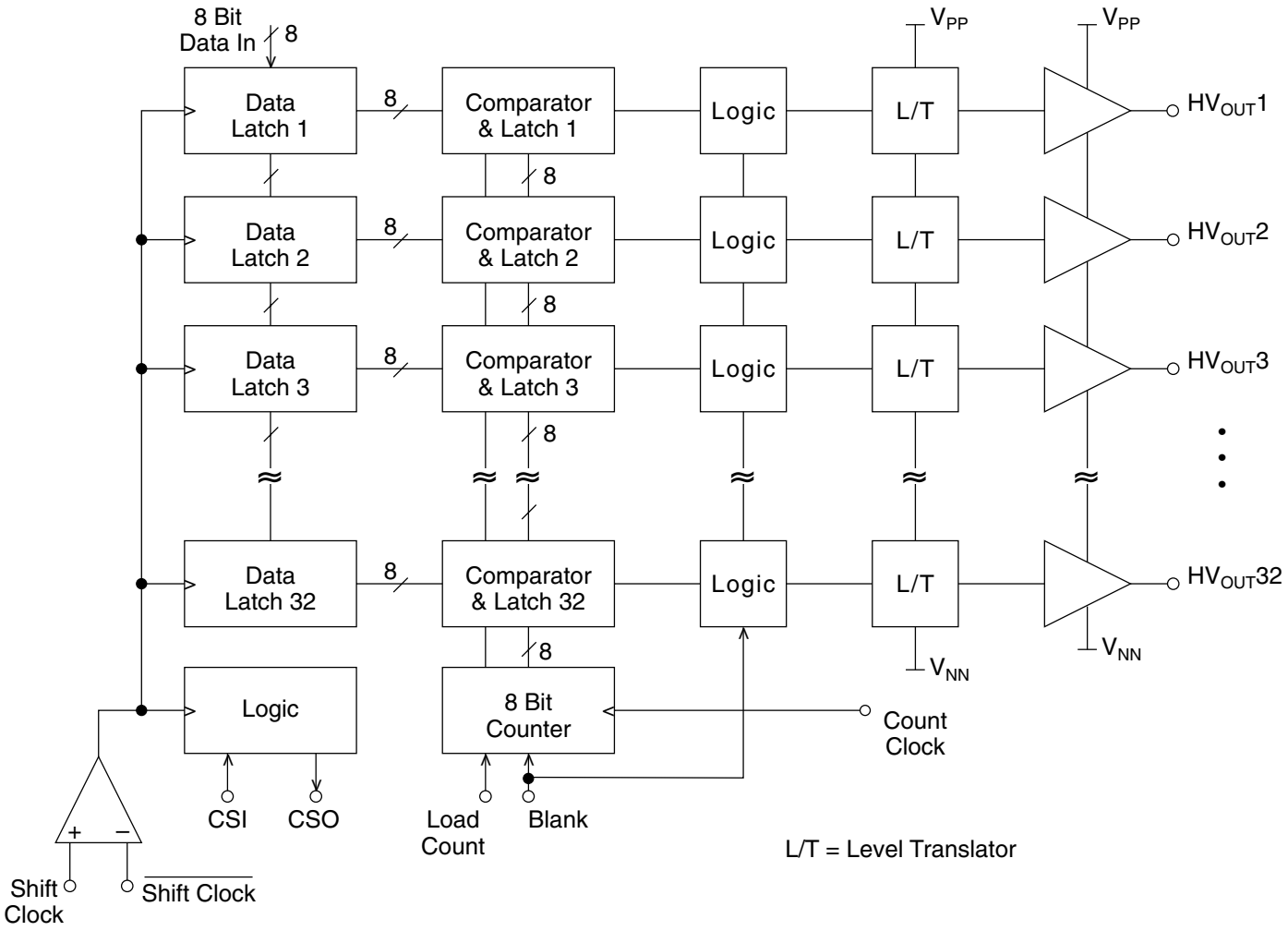


Logic Data Output

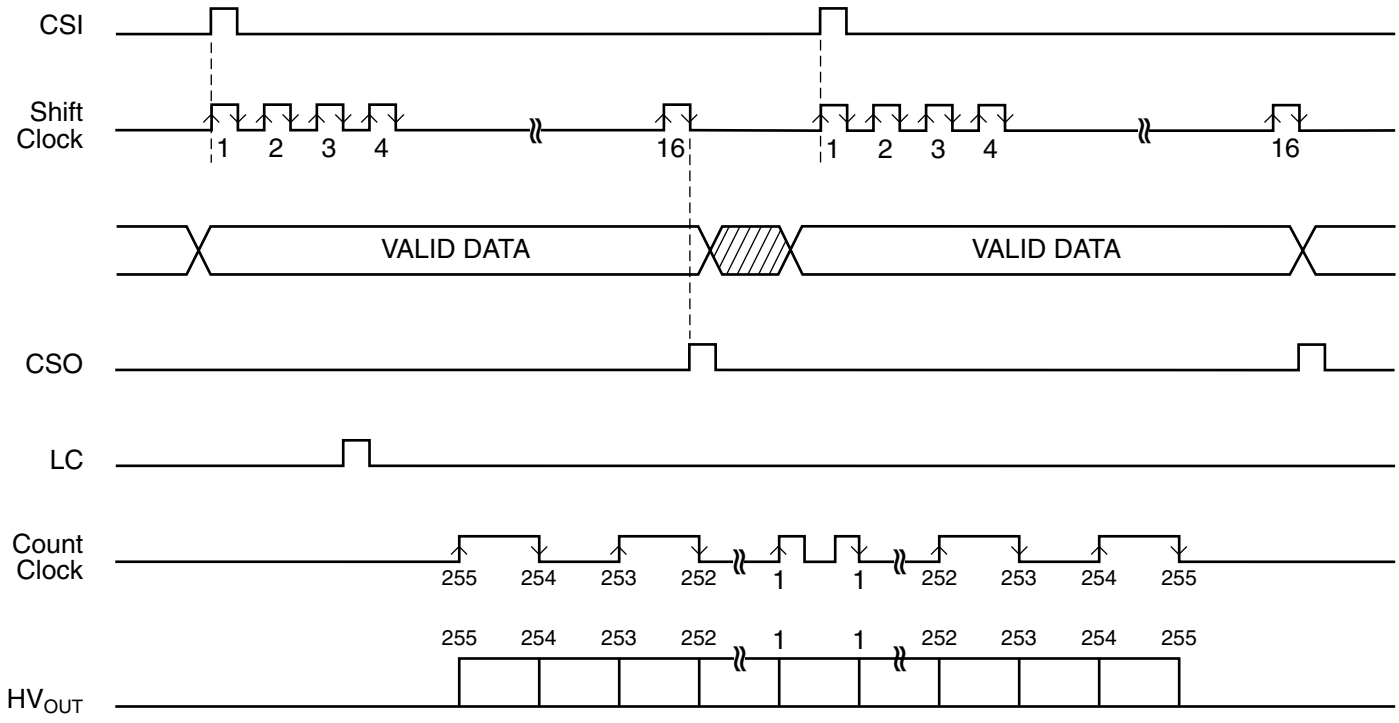


High Voltage Output

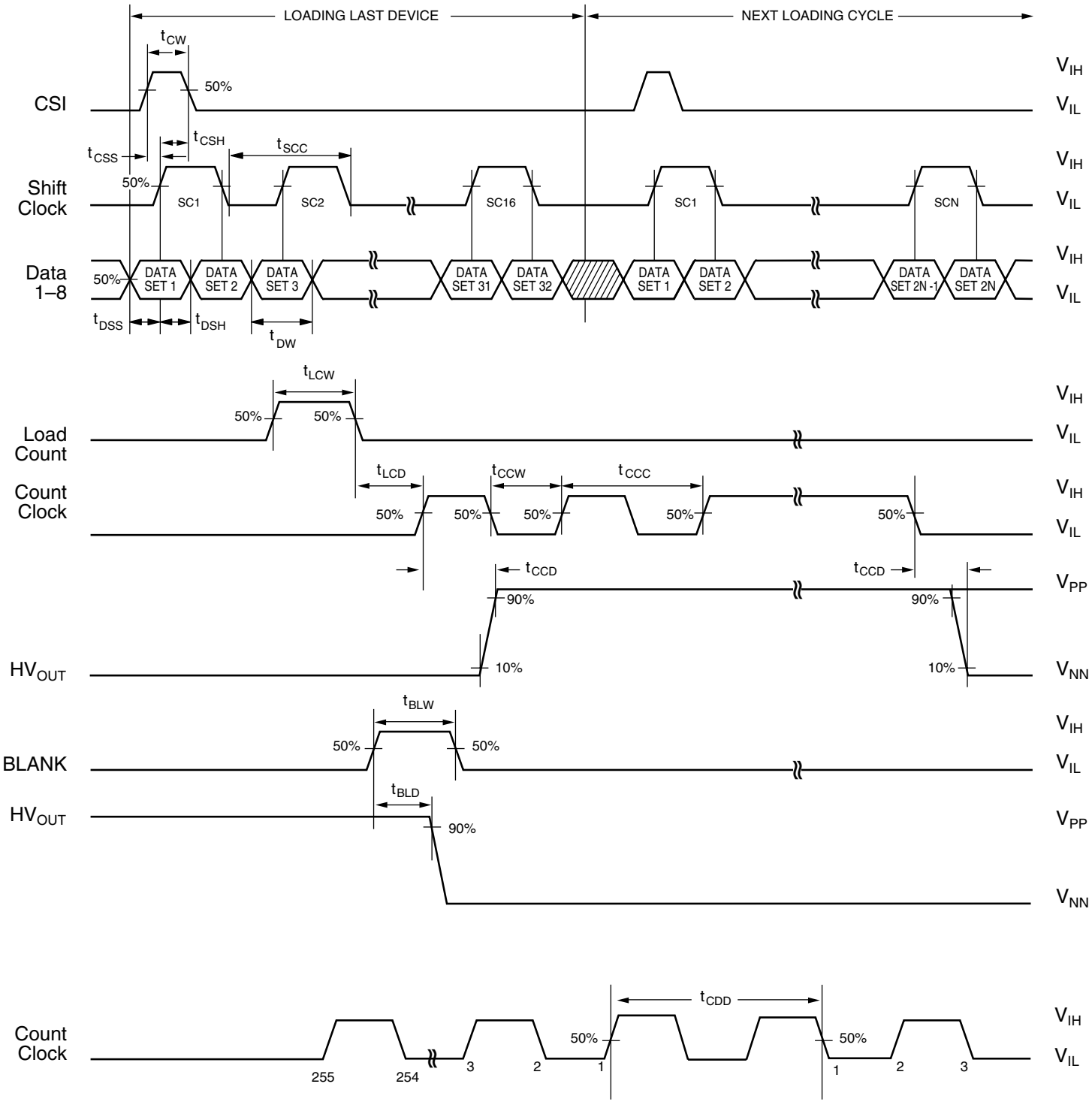
Functional Block Diagram



Timing Diagrams



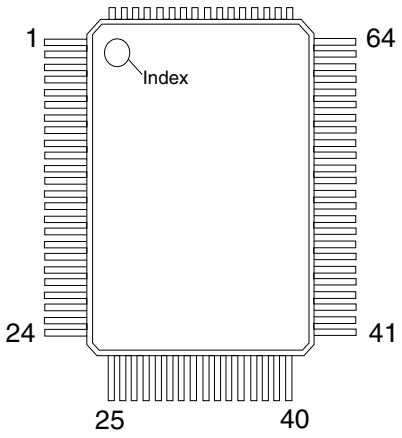
Timing Diagrams



Pin Configurations

Pin	Function	Pin	Function
1	N/C	33	Load Count
2	N/C	34	Shift Clock
3	N/C	35	$\overline{\text{Shift Clock}}$
4	$HV_{OUT}17$	36	D5
5	$HV_{OUT}18$	37	D6
6	$HV_{OUT}19$	38	D7
7	$HV_{OUT}20$	39	D8
8	$HV_{OUT}21$	40	V_{DD} (Digital)
9	$HV_{OUT}22$	41	V_{DD} (Analog)
10	$HV_{OUT}23$	42	GND (Analog)
11	$HV_{OUT}24$	43	V_{PP}
12	$HV_{OUT}25$	44	V_{NN}
13	$HV_{OUT}26$	45	N/C
14	$HV_{OUT}27$	46	$HV_{OUT}1$
15	$HV_{OUT}28$	47	$HV_{OUT}2$
16	$HV_{OUT}29$	48	$HV_{OUT}3$
17	$HV_{OUT}30$	49	$HV_{OUT}4$
18	$HV_{OUT}31$	50	$HV_{OUT}5$
19	$HV_{OUT}32$	51	$HV_{OUT}6$
20	GND (Digital)	52	$HV_{OUT}7$
21	GND (Digital)	53	$HV_{OUT}8$
22	V_{NN}	54	$HV_{OUT}9$
23	V_{PP}	55	$HV_{OUT}10$
24	CSI	56	$HV_{OUT}11$
25	CSO	57	$HV_{OUT}12$
26	Blank	58	$HV_{OUT}13$
27	D1	59	$HV_{OUT}14$
28	D2	60	$HV_{OUT}15$
29	D3	61	$HV_{OUT}16$
30	D4	62	N/C
31	Count Clock	63	N/C
32	N/C	64	N/C

Package Outline



top view

3-sided Plastic 64-pin Gullwing Package

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