TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

65,536 WORD × 32 BIT Synchronous Pipelined Burst SRAM

DESCRIPTION

The TC55V2325FF is a 2,097,152 bit synchronous pipelined burst SRAM that is organized as 65,536 words by 32 bits and designed for use in a secondary cache to support MPUs which have burst functions.

The TC55V2325FF integrates a 2-bit burst address counter and control logic with a 64K×32 static RAM. All inputs, except the output enable ($\overline{OE}$) input, are synchronous with the rising edge of the clock (CLK) input.

The read operation can be initiated with either the address status processor ($\overline{ADSP}$) input or the address status controller ($\overline{ADSC}$) input. Subsequent burst addresses can be generated internally and are controlled by the address advance ($\overline{ADV}$) input.

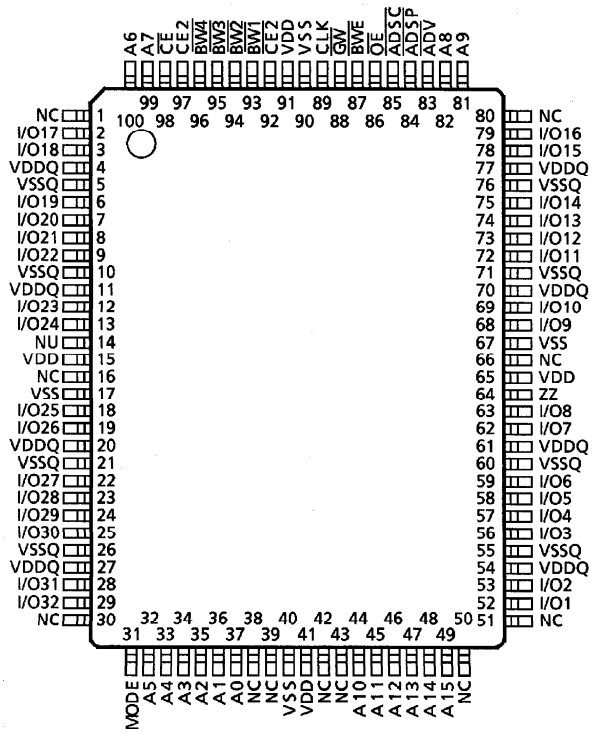
The write operation is internally self timed and is initiated by the rising edge of the clock (CLK) input. Byte Write Enables ($\overline{BW1}$ - $\overline{BW4}$) allow a one to four byte write operation according to their logic states.

The TC55V2325FF operates from a single 3.3V power supply and is packaged in a low profile 100pin plastic QFP (LQFP).

FEATURES

- Organization : 64K words × 32 bits
- Fast cycle time : 10ns min. (100MHz max.)
- Fast access time : 6ns max.
- Synchronous Burst Operation
- 2-bit burst address counter (Interleaved Burst or Linear Burst Sequences)
- Synchronous self-timed write (Global Write and Byte Write)
- Snooze mode pin (ZZ) for power down
- LVTTL compatible interface
- Package : 100pin LQFP(0.65mm pitch, 1.6mm height typ.) : LQFP100-P-1420-0.65K(Weight : 0.56g Typ.)

PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A15	Address Inputs
I/O1~I/O32	Data Inputs / Outputs
CLK	Clock Input
$\overline{CE}$, $\overline{CE2}$, CE2	Chip Enable Inputs
$\overline{ADSP}$	Address Status Processor Input
$\overline{ADSC}$	Address Status Controller Input
$\overline{ADV}$	Address Advance Input
$\overline{GW}$	Global Write Enable Input
$\overline{BWE}$	Byte Write Enable Input
$\overline{BW1}$~$\overline{BW4}$	Byte Write Enable Inputs
$\overline{OE}$	Output Enable Input
MODE	Mode Select Input
ZZ	Snooze Input
NU	Not Usable Input
V_{DD}, V_{DDQ}	Power
V_{SS}, V_{SSQ}	Ground
NC	No Connection

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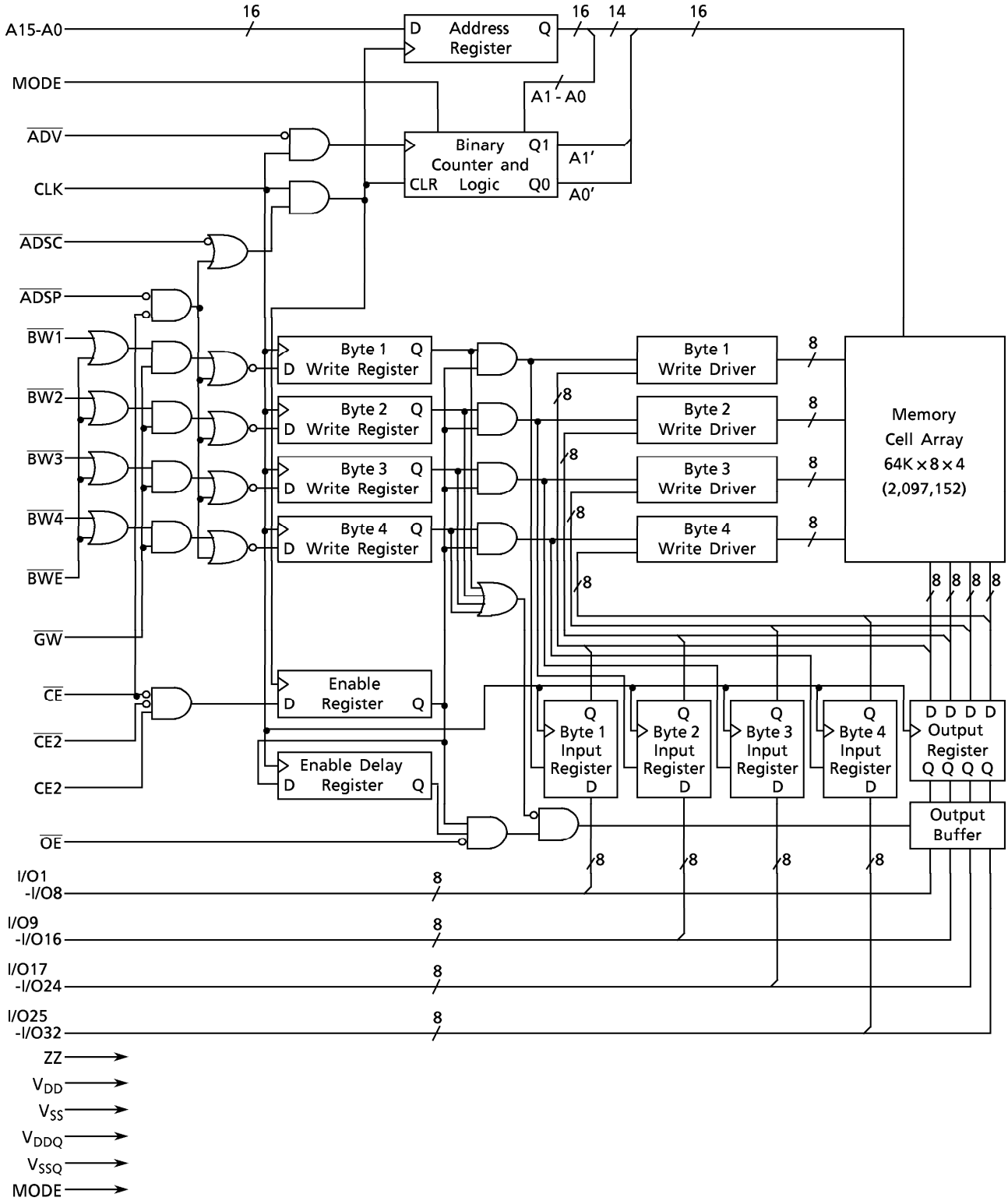
BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NUMBER	SYMBOL	TYPE	DESCRIPTION
37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48, 49	A0 - A15	Input (Synchronous)	Synchronous Address Inputs. These address inputs are registered on the rising edges of CLK. All address inputs must meet the setup and hold times for all rising edges of CLK when the chip is enabled.
93, 94, 95, 96	$\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$	Input (Synchronous)	Synchronous Byte Write Enables. These inputs are active low and control byte write operations when $\overline{BWE}$ is low. $\overline{BW1}$ controls I/O1 - 8. $\overline{BW2}$ controls I/O9 - 16. $\overline{BW3}$ controls I/O17 - 24. $\overline{BW4}$ controls I/O25 - 32. For byte write operations, if any of these four inputs are low, all outputs are in high impedance.
87	$\overline{BWE}$	Input (Synchronous)	Synchronous Byte Write Enable. This input is active low and controls byte write operations.
88	$\overline{GW}$	Input (Synchronous)	Synchronous Global Write. This input is active low and controls a 32bit write operation independent of the $\overline{BWE}$ and $\overline{BW1}$ - $\overline{BW4}$ inputs.
89	CLK	Input	Reference Clock. All synchronous input signals are registered on all rising edges of CLK. All synchronous signal timings are measured from the rising edges of CLK. All synchronous input signals must meet the setup and hold times referenced to the rising edges of CLK.
83	$\overline{ADV}$	Input (Synchronous)	Synchronous Burst Advance. This signal is active low and controls the internal burst address counter after the external address is loaded. When this signal is low, the internal burst address is advanced. When this signal is high, the internal burst address is not advanced. If a write operation initiated by $\overline{ADSP}$ is desired, this signal must be high to write the loaded address at the rising edge of the first clock after an assertion of $\overline{ADSP}$.
84	$\overline{ADSP}$	Input (Synchronous)	Synchronous Address Status Processor. This signal is active low. This signal controls the burst start by registering the new external address. The write enables ($\overline{GW}$, $\overline{BWE}$, $\overline{BW1}$ - $\overline{BW4}$) are ignored at the assertion of $\overline{ADSP}$ and a read operation is initiated. A subsequent operation is dependent on the write enables at the rising edge of the first clock after an assertion of $\overline{ADSP}$. This signal is ignored if $\overline{CE}$ is high.

PIN NUMBER	SYMBOL	TYPE	DESCRIPTION
85	$\overline{ADSC}$	Input (Synchronous)	Synchronous Address Status Controller. This signal is active low. This signal initiates a burst read or write depending on the write enables ($\overline{GW}$, $\overline{BWE}$, $\overline{BW1}$ - 4) by registering the new external address.
98	$\overline{CE}$	Input (Synchronous)	Synchronous Chip Enable. This signal is active low. This signal controls the chip status (enable or disable) and the internal use of $\overline{ADSP}$. This signal is sampled only when a new external address is loaded.
92	$\overline{CE2}$	Input (Synchronous)	Synchronous Chip Enable. This signal is active low. This signal controls the chip status (enable or disable). This signal is sampled only when a new external address is loaded. This input can be used for memory address depth expansion.
97	CE2	Input (Synchronous)	Synchronous Chip Enable. This signal is active high. This signal controls the chip status (enable or disable). This signal is sampled only when a new external address is loaded. This input can be used for memory address depth expansion.
86	$\overline{OE}$	Input (Asynchronous)	Asynchronous Output Enable. This signal is active low and controls all 32bit I/O output buffers. This signal must be high for the time write data is driven prior to the assertion of the byte write enables ($\overline{GW}$, $\overline{BWE}$, $\overline{BW1}$ - $\overline{BW4}$) following a read operation.
52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29	I/O1 - I/O32	Input / Output (Synchronous)	Synchronous Data Inputs / Outputs. Byte1 is I/O1 - I/O8, Byte2 is I/O9 - I/O16, Byte3 is I/O17 - I/O24, Byte4 is I/O25 - I/O32.
31	MODE	Input (Asynchronous)	Mode Select. This signal is used to select the burst sequence. If this signal is high or not connected, the burst sequence is Interleaved Burst. If this signal is low, the burst sequence is Linear Burst. This input is internally pulled up. Altering the input state while the device is operating is prohibited.

PIN NUMBER	SYMBOL	TYPE	DESCRIPTION
64	ZZ	Input (Asynchronous)	Snooze. This signal is active high and is used to place the device into sleep mode, which is a low power standby mode. If this signal is low or not connected, the device is in an active state. If this signal is high, the device is in a sleep state, and the memory data is retained. The device wakes up when a read or write operation is initiated by $\overline{ADSP}$ or $\overline{ADSC}$ after deasserting this signal. This input must be connected to V_{SS} when ZZ mode is not used.
14	NU	Input (Asynchronous)	Not Usable This signal must be high or not connected. This input is pulled up internally.
1, 16, 30, 38, 39, 42, 43, 50, 51, 66, 80	NC	—	No Connection. These inputs are not internally connected. Pin number 50 is reserved for future device expansion.
15, 41, 65, 91	V_{DD}	Supply	Power Supply.
17, 40, 67, 90	V_{SS}	Ground	Ground.
4, 11, 20, 27, 54, 61, 70, 77	V_{DDQ}	Supply	Output Buffer Power Supply.
5, 10, 21, 26, 55, 60, 71, 76	V_{SSQ}	Ground	Output Buffer Ground.

OPERATING MODE

(1) Synchronous Input Truth Table

OPERATION	CLK	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$ [4]	ZZ [1]	ADDRESS USED	I/O [5]	CURRENT [2]
Begin Burst Read	L→H	L	L	H	L	×	×	×	L	External Address	Dout (n)	I_{DDO1}
	L→H	L	L	H	H	L	×	H	L			
Continue Burst Read	L→H	×	×	×	H	H	L	H	L	Next Burst Address	Dout (n)	I_{DDO1}
	L→H	H	×	×	L [6]	H	L	H	L			
Suspend Burst Read	L→H	×	×	×	H	H	H	H	L	Current Burst Address	Dout (n)	I_{DDO2}
	L→H	H	×	×	L [6]	H	H	H	L			
Begin Burst Write	L→H	L	L	H	H	L	×	L	L	External Address	Din (p)	N/A
	L→H	×	×	×	H	H	H	L	L	Current Burst Address		
	L→H	H	×	×	L [6]	H	H	L	L			
Continue Burst Write	L→H	×	×	×	H	H	L	L	L	Next Burst Address	Din (p)	N/A
	L→H	H	×	×	L [6]	H	L	L	L			
Suspend Burst Write	L→H	×	×	×	H	H	H	L	L	Current Burst Address	Din (p)	N/A
	L→H	H	×	×	L [6]	H	H	L	L			
Deselected	L→H	H	×	×	×	L	×	×	L	None	Hi - Z (p)	I_{DDS2}
	L→H	L	H	×	L	×	×	×	L			
	L→H	L	×	L	L	×	×	×	L			
	L→H	L	H	×	H	L	×	×	L			
	L→H	L	×	L	H	L	×	×	L			
Snooze	L→H	×	×	×	×	×	×	×	H	None	Hi - Z (p)	I_{DDS3}

NOTE : 1. ZZ input is asynchronous, but is included in this table.
2. Consumption current does not include output buffer current.
3. H is logical High and L is logical Low. X is High or Low.
4. $\overline{WRITE}$ = L means any one or more byte write enable inputs ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$) and $\overline{BWE}$ are Low or $\overline{GW}$ is Low. $\overline{WRITE}$ = H means $\overline{GW}$ and $\overline{BWE}$ are High, or $\overline{GW}$ is High and $\overline{BWE}$ is Low and all byte write enable inputs are High.
5. (n) and (p) indicate the cycles affected by the synchronous control inputs. (n) is the next cycle, (p) is the present cycle.
6. When $\overline{CE}$ = H, $\overline{ADSP}$ is disabled ($\overline{ADSP}$ = X). $\overline{ADSP}$ = L to avoid redundancy with the previous truth table entry when $\overline{CE}$ = H and $\overline{ADSP}$ = H.

(2) Partial Truth Table for Write Enables (Synchronous Input)

OPERATION	CLK	$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$	I/O1 - I/O8	I/O9 - I/O16	I/O17 - I/O24	I/O25 - I/O32
Read	L→H	H	H	×	×	×	×	Dout (n)	Dout (n)	Dout (n)	Dout (n)
	L→H	H	L	H	H	H	H	Dout (n)	Dout (n)	Dout (n)	Dout (n)
Write	L→H	L	×	×	×	×	×	Din (p)	Din (p)	Din (p)	Din (p)
		H	L	L	L	L	L	Din (p)	Din (p)	Din (p)	Din (p)
		H	L	L	H	H	H	Din (p)	Hi - Z (p)	Hi - Z (p)	Hi - Z (p)
				H	L	H	H	Hi - Z (p)	Din (p)	Hi - Z (p)	Hi - Z (p)
				H	H	L	H	Hi - Z (p)	Hi - Z (p)	Din (p)	Hi - Z (p)
				H	H	H	L	Hi - Z (p)	Hi - Z (p)	Hi - Z (p)	Din (p)
				The other 11 combinations of $\overline{BW1}$ to $\overline{BW4}$ are also effective. $\overline{BW1}$ controls I/O1 - I/O8. $\overline{BW2}$ controls I/O9 - I/O16. $\overline{BW3}$ controls I/O17 - I/O24. $\overline{BW4}$ controls I/O25 - I/O32.						

NOTE : 1. (n) and (p) indicate the cycles affected by the synchronous control inputs. (n) is the next cycle, (p) is the present cycle.

(3) Asynchronous Truth Table

OPERATION	$\overline{OE}$	ZZ	I/O1 - I/O32
Pipelined Read	L	L	Dout (n)
	H	L	Hi - Z
Write	×	L	Din, Hi - Z
Deselected	×	L	Hi - Z
Snooze	×	H	Hi - Z

NOTE : 1. H is logical High and L is logical Low. X is High or Low.

(4) Write Pass-through Truth Table

Previous Cycle				Present Cycle											Next Cycle
Operation	Addr.	$\overline{WRITE}$	I/O	Operation	Addr.	$\overline{WRITE}$	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{OE}$	I/O	I/O
Write Cycle	Ak	L	Dn (Ak)	$\overline{ADSP}$ Initiated Read Cycle	Am	×	L	L	H	L	×	×	L	Qn (Ak)	Q1 (Am)
				$\overline{ADSC}$ Initiated Read Cycle	Am	H	L	L	H	H	L	×	L		
				Continue Read Cycle	×	H	×	×	×	H	H	L	L		Qn + 1 (Ak)
					×	H	H	×	×	L	H	L	L		

NOTE : 1. Dn (Ak) represents input data for the n-th burst address starting from address Ak.
2. Qn (Ak) represents output data from the n-th burst address starting from address Ak.
3. n = 1, 2, 3, or 4
4. $\overline{WRITE}$ = L means any one or more byte write enable inputs ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$) and $\overline{BWE}$ are Low or $\overline{GW}$ is Low. $\overline{WRITE}$ = H means $\overline{GW}$ and $\overline{BWE}$ are High, or $\overline{GW}$ is High and $\overline{BWE}$ is Low and all byte write enable inputs are High.

(5) Interleaved Burst Sequence (MODE input = NC or V_{DD})

Bit Order : A_{15} A_{14} ..... A_3 A_2 A_1 A_0
Lower 2 bits are internally generated from the external address.

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
XX ····· XX00	XX ····· XX01	XX ····· XX10	XX ····· XX11
XX ····· XX01	XX ····· XX00	XX ····· XX11	XX ····· XX10
XX ····· XX10	XX ····· XX11	XX ····· XX00	XX ····· XX01
XX ····· XX11	XX ····· XX10	XX ····· XX01	XX ····· XX00

The burst address wraps around to its initial state.

(6) Linear Burst Sequence (MODE input = V_{SS})

Bit Order : A_{15} A_{14} ..... A_3 A_2 A_1 A_0
Lower 2 bits are internally generated from the external address.

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
XX ····· XX00	XX ····· XX01	XX ····· XX10	XX ····· XX11
XX ····· XX01	XX ····· XX10	XX ····· XX11	XX ····· XX00
XX ····· XX10	XX ····· XX11	XX ····· XX00	XX ····· XX01
XX ····· XX11	XX ····· XX00	XX ····· XX01	XX ····· XX10

The burst address wraps around to its initial state.

(7) Stop Clock Mode for Power Down

TC55V2325FF gets in a low power standby mode by stopping a clock input.
TC55V2325FF can retain all state and data values even though the clock is not running.

In order to achieve the lowest power operation, the following signal states should be required.

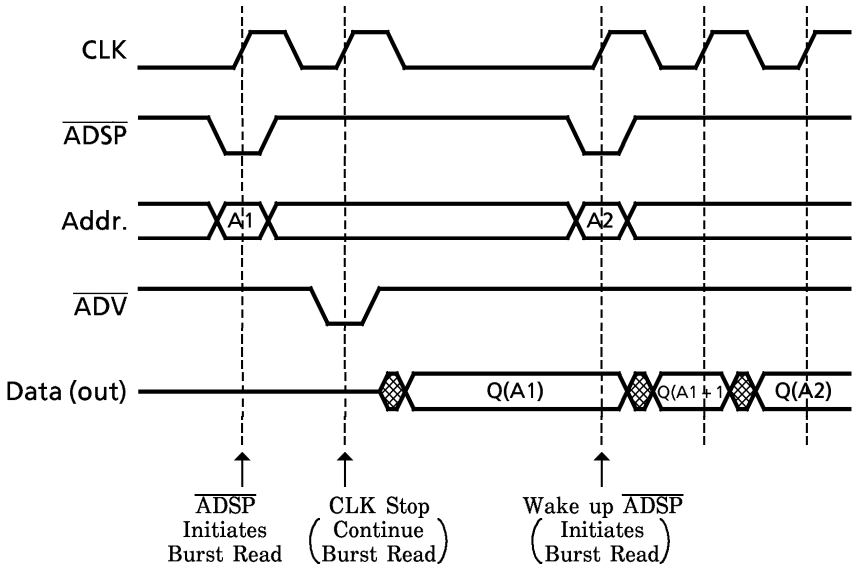
i) Clock is low state

ii) Control signals are inactive states (ex. $\overline{ADSP}$ is high state)

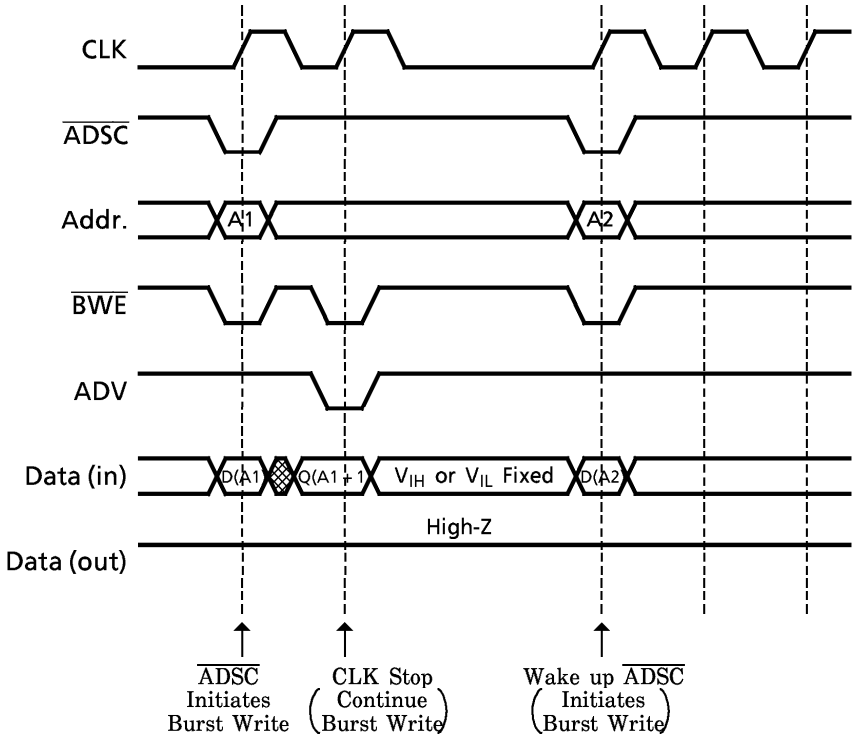
For lowest possible power consumption during stop-clock, the address should be driven to MOS level ($V_{IH} \geqq V_{DD}-0.2V$ or $V_{IL} \leqq 0.2V$), and the data input should be driven to MOS low level ($V_{IL} \leqq 0.2V$).

· Clock re-start sequence

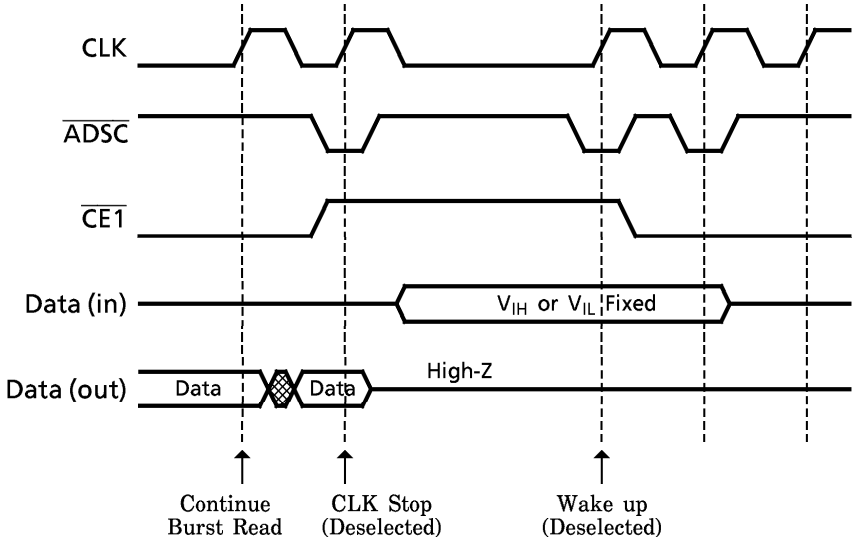
The device can be waked up by the first rising edge of the clock signal after having been in power down mode.



i) Stop Clock Timing for Read Operation



ii) Stop Clock Timing for Write Operation



iii) Stop Clock Timing for Deselect Operation

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	− 0.5~4.6	V
V_{DDQ}	Output Buffer Power Supply Voltage	− 0.5~V_{DD}	V
V_{IN}	Input Terminal Voltage	− 0.5 * ~4.6	V
$V_{I/O}$	Input / Output Terminal Voltage	− 0.5 * ~V_{DDQ} + 0.5**	V
P_D	Power Dissipation	1.2	W
T_{solder}	Soldering Temperature (10s)	260	°C
T_{strg}	Storage Temperature	− 65~150	°C
T_{opr}	Operating Temperature	− 10~85	°C

* : −1.5V with a pulse width of 20% · ^{t}KC min
** : V_{DDQ}+1.5V with a pulse width of 20% · ^{t}KC min

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	3.1	3.3	3.6	V
V_{DDQ}	Output Buffer Power Supply Voltage	3.1	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	−	V_{DD} + 0.3**	V
$V_{IH\,1}$	Input High Voltage for MODE and NU pins	V_{DD} − 0.3	V_{DD}	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	− 0.3 *	−	0.8	V
$V_{IL\,1}$	Input Low Voltage for MODE pin	− 0.3	0.0	0.3	V

* : −1.0V with a pulse width of 20% · ^{t}KC min
** : V_{DD}+1.0V with a pulse width of 20% · ^{t}KC min

DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, $V_{DD} = V_{DDQ} = 3.1V \sim 3.6V$)

SYMBOL	PARAMETER		TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current (Except MODE, ZZ pins)		$V_{IN} = 0 \sim V_{DD}$	–	–	±1	μA
I_{LO}	Output Leakage Current		Device Deselected or Output Deselected, $V_{OUT} = 0 \sim V_{DD}$	–	–	±1	μA
I_I	Input Current	MODE pin	$V_{IN} = V_{DD} \sim V_{DD} - 0.3V$	– 1	–	1	μA
			$V_{IN} = 0 \sim 0.3V$	– 100	–	1	
		ZZ pin	$V_{IN} = V_{DD} \sim 2.0V$	– 1	–	100	
			$V_{IN} = 0 \sim 0.8V$	– 1	–	20	
			$V_{IN} = 0 \sim 0.3V$	– 1	–	1	
V_{OH}	Output High Voltage		$I_{OH} = -8mA$	2.4	–	–	V
			$I_{OH} = -100\mu A$	$V_{DDQ} - 0.2$	–	–	
V_{OL}	Output Low Voltage		$I_{OL} = 8mA$	–	–	0.4	
			$I_{OL} = 100\mu A$	–	–	0.2	
I_{DDO1}	Operating Current		Device Selected, Iout = 0mA All inputs = V_{IH} / V_{IL} CLK ≧ t_{KC} min.	–	–	220	mA
I_{DDO2}	Operating Current (Idle)		Device Selected, Iout = 0mA $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≧ V_{IH} All inputs = V_{IH} / V_{IL}, CLK ≧ t_{KC} min.	–	–	190	mA
I_{DDS1}	Standby Current (CLK running)		Device Deselected, All inputs = V_{IH}/ V_{IL} CLK ≧ t_{KC} min.	–	–	55	mA
I_{DDS2}	Standby Current		Device Deselected, All inputs = V_{DD} – 0.2V or 0.2V CLK frequency = 0Hz	–	–	2	mA
I_{DDS3}	Snooze Current by ZZ pin		ZZ = V_{DD} – 0.2V, All inputs = V_{IH} / V_{IL} CLK ≧ t_{KC} min.	–	–	2	mA
I_{DDS4}	Snooze Current by Stop Clock Mode		ZZ ≦ 0.2V, Chip Deselected CLK ≦ 0.2V, $\overline{ADSP}$, $\overline{ADSC}$ = V_{DD} – 0.2V All inputs = V_{DD} – 0.2V or 0.2V	–	–	2	mA

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	5	pF
	Input Capacitance for MODE, ZZ pin	V_{IN} = GND	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = GND	6	pF

NOTE : This parameter is periodically sampled and is not 100% tested.

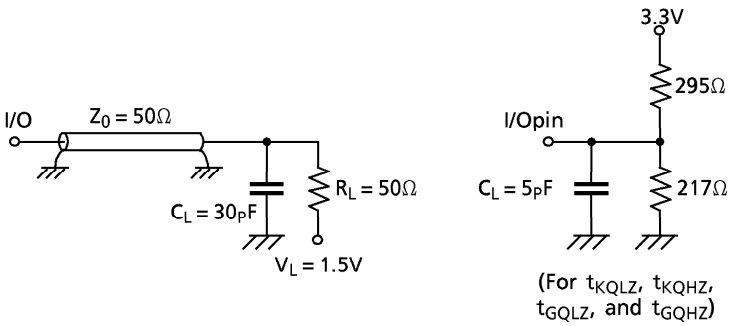
AC CHARACTERISTICS (Ta = 0~70°C, $V_{DD} = V_{DDQ} = 3.1V \sim 3.6V$)

SYMBOL	PARAMETER	TC55V2325FF - 100		UNIT
		MIN.	MAX.	
t_{KC}	CLK Cycle Time	10	–	ns
t_{KH}	CLK High Pulse Width	4	–	
t_{KL}	CLK Low Pulse Width	4	–	
t_{KQV}	Access Time from CLK	–	6	
t_{KQX}	Output Hold Time from CLK	2	–	
t_{KQLZ}	Output Enable Time from CLK	2	–	
t_{KQHZ}	Output Disable Time from CLK	2	5	
t_{GQV}	Access Time from $\overline{OE}$	–	6	
t_{GQLZ}	Output Enable Time from $\overline{OE}$	0	–	
t_{GQHZ}	Output Disable Time from $\overline{OE}$	2	5	
t_{AS}	Address Input Setup Time from CLK	2.5	–	
t_{AH}	Address Input Hold Time from CLK	0.5	–	
t_{ADSS}	$\overline{ADSP}$, $\overline{ADSC}$ Input Setup Time from CLK	2.5	–	
t_{ADSH}	$\overline{ADSP}$, $\overline{ADSC}$ Input Hold Time from CLK	0.5	–	
t_{AVS}	$\overline{ADV}$ Input Setup Time from CLK	2.5	–	
t_{AVH}	$\overline{ADV}$ Input Hold Time from CLK	0.5	–	
t_{WS}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW1}$ - $\overline{BW4}$ Input Setup Time from CLK	2.5	–	
t_{WH}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW1}$ - $\overline{BW4}$ Input Hold Time from CLK	0.5	–	
t_{CES}	$\overline{CE}$, $\overline{CE2}$, CE2 Input Setup Time from CLK	2.5	–	
t_{CEH}	$\overline{CE}$, $\overline{CE2}$, CE2 Input Hold Time from CLK	0.5	–	
t_{DS}	Data Setup Time from CLK	2.5	–	
t_{DH}	Data Hold Time from CLK	0.5	–	
t_{ZS}	ZZ Standby Time	5	–	
t_{ZR}	ZZ Recovery Time	8	–	
t_{ZHZ}	Output Disable Time from ZZ	0	20	

AC TEST CONDITIONS

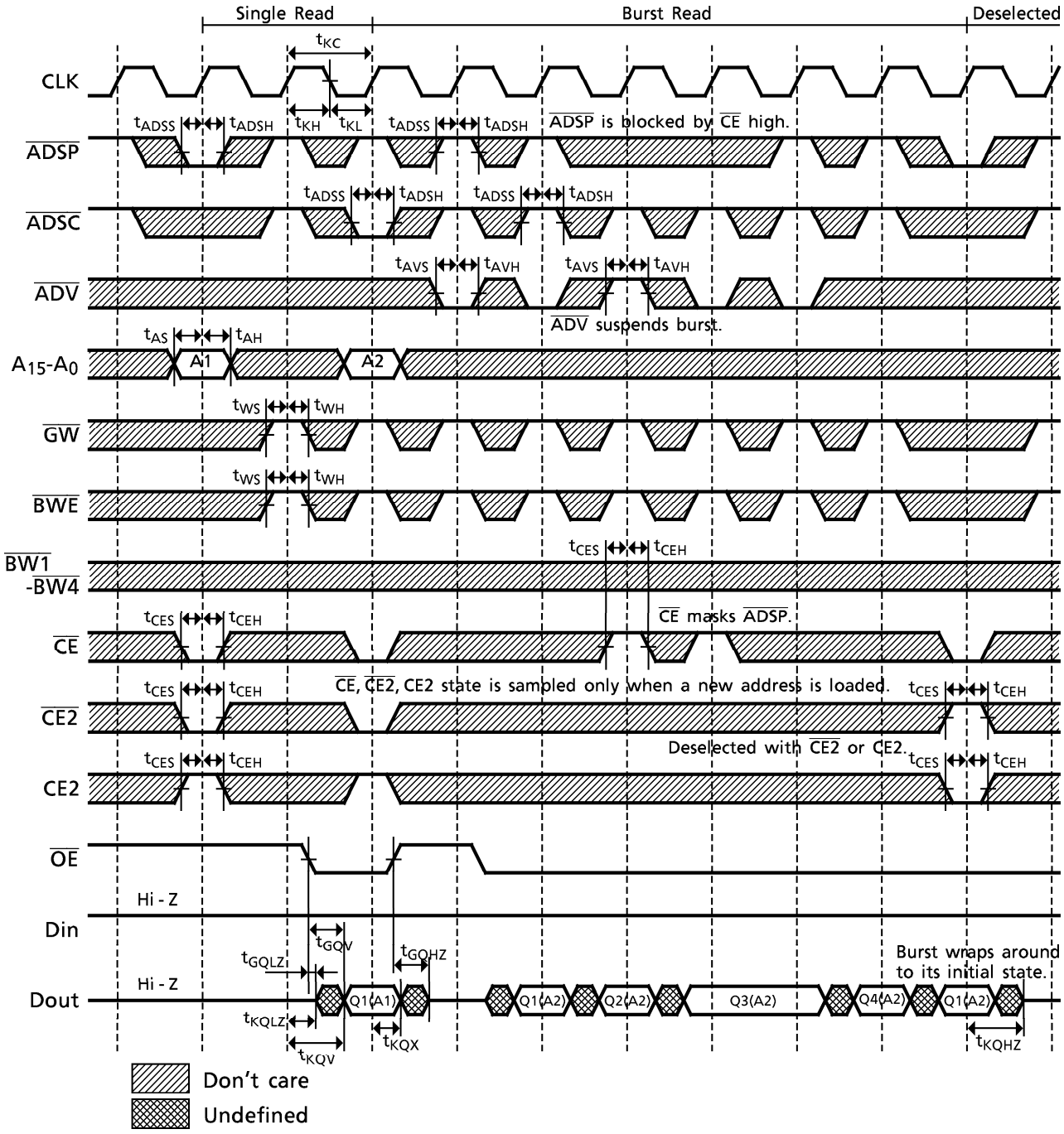
Input Pulse Level	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

Fig. 1



TIMING WAVEFORMS

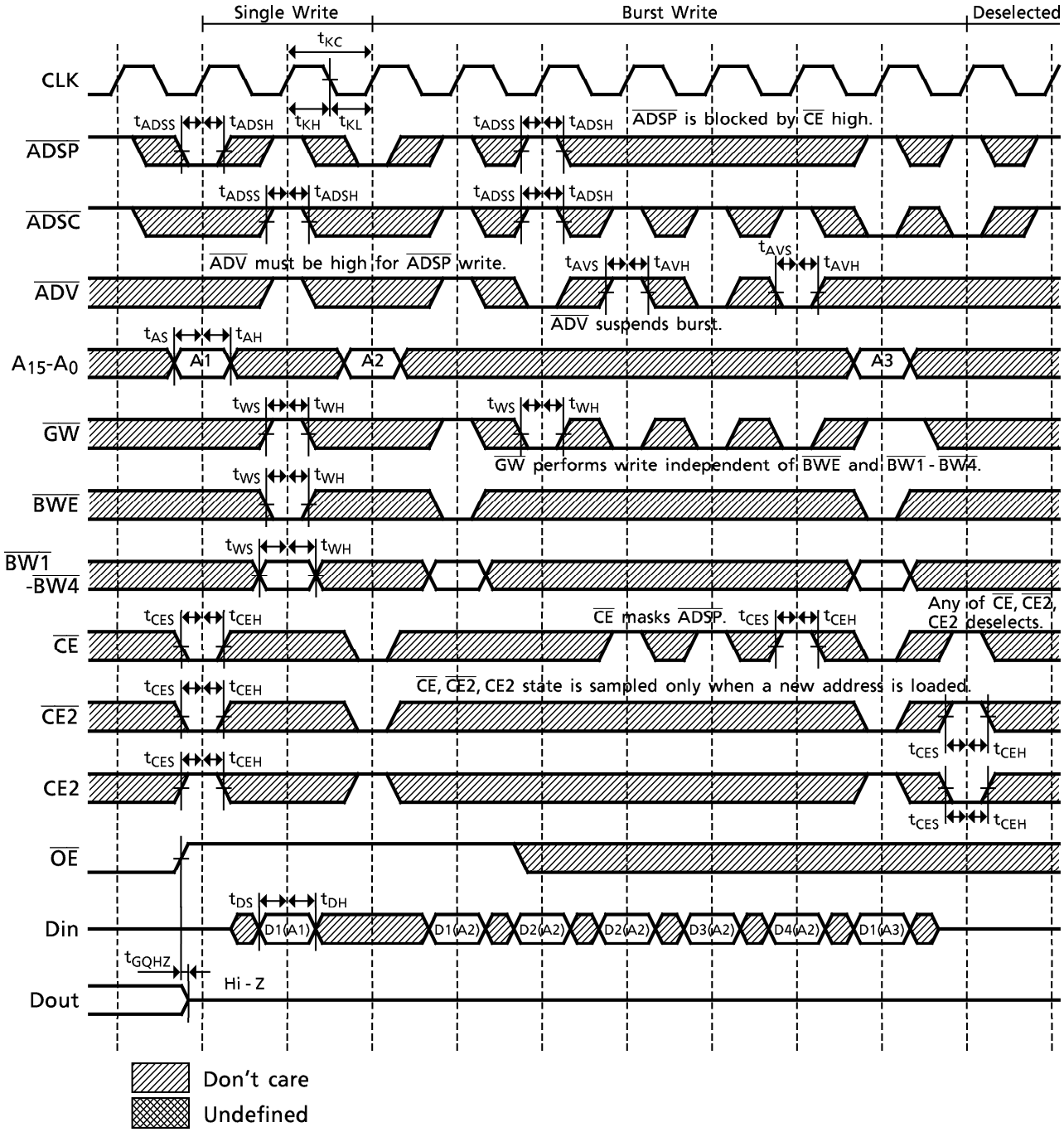
READ CYCLE (Pipeline)



Note

1. Q1(A2) represents output data from 1st burst address starting from address A2. Q2(A2) represents output data from 2nd burst address starting from address A2.
2. ZZ is Low.

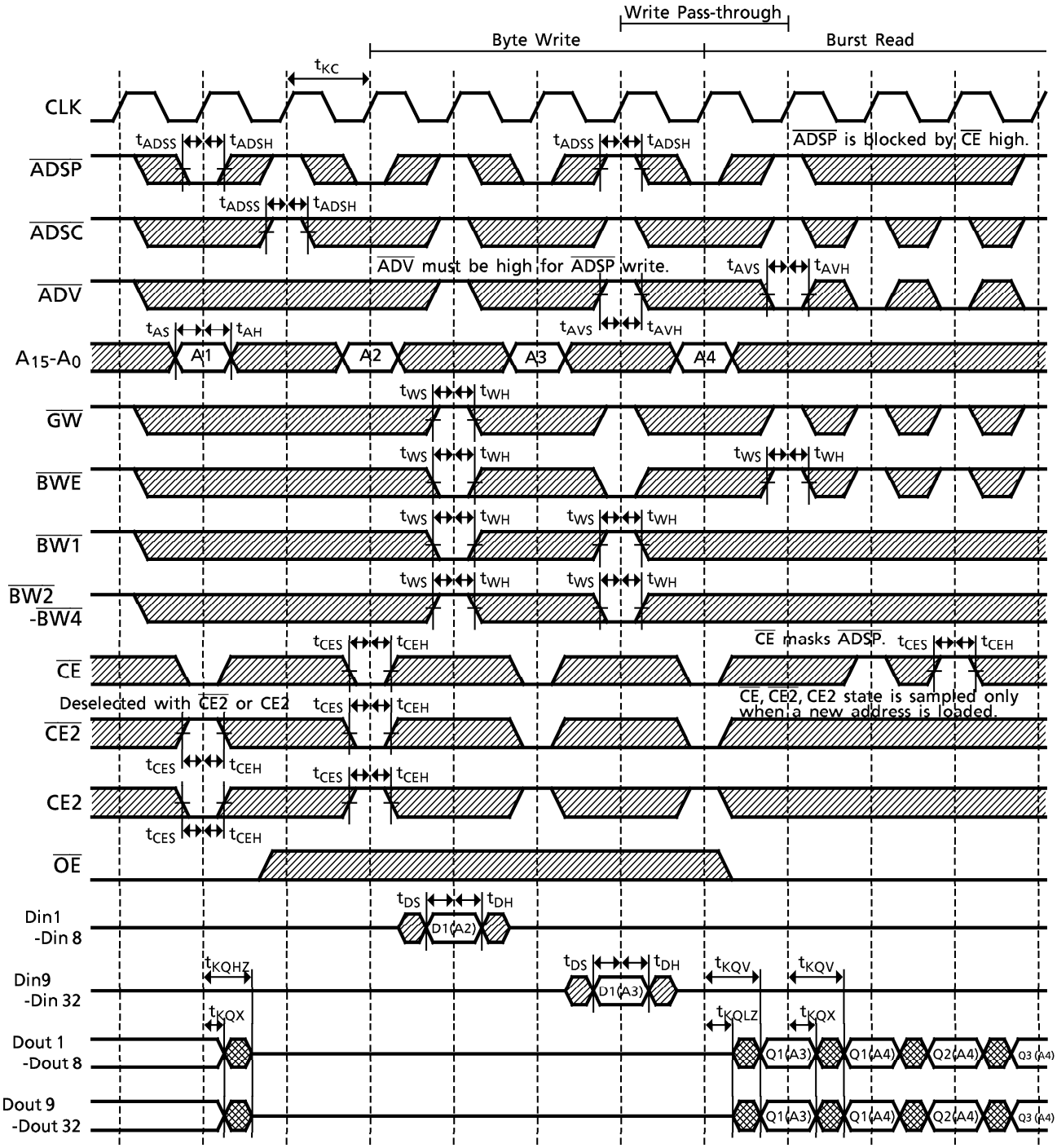
WRITE CYCLE (Pipeline)



Note

1. D1(A2) represents input data for 1st burst address starting from address A2. D2(A2) represents input data for 2nd burst address starting from address A2.
2. ZZ is Low.

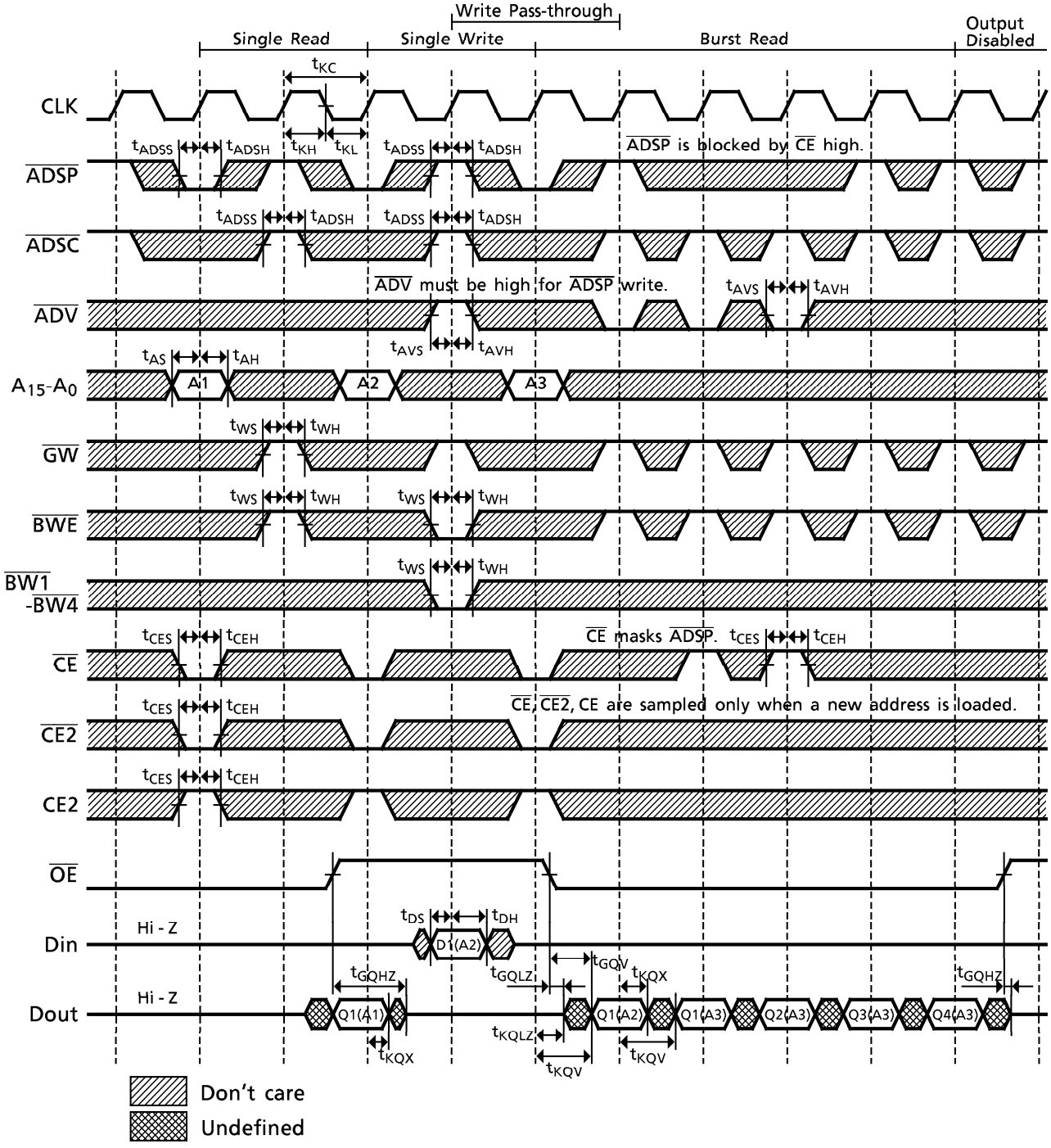
WRITE CYCLE (Pipeline : Byte Write Timing)



Note

1. ZZ is Low.

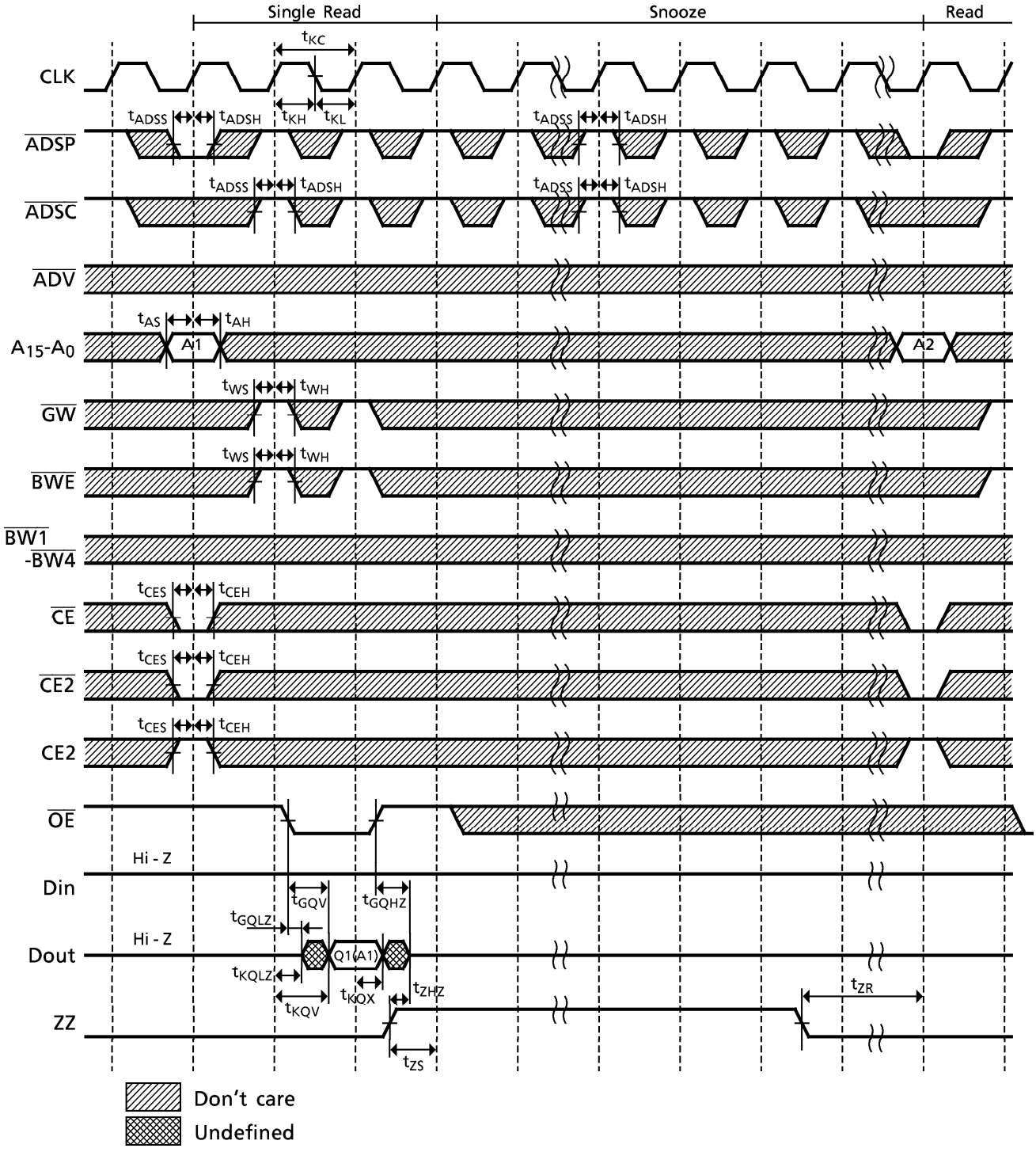
READ / WRITE CYCLE (Pipeline)



Note

1. When a write operation follows a read operation, $\overline{OE}$ must be driven high prior to the assertion of the byte write enables ($\overline{GW}$, $\overline{BWE}$, $\overline{BW1}$ - $\overline{BW4}$) and before input data is applied to avoid data bus contention.
2. ZZ is Low.

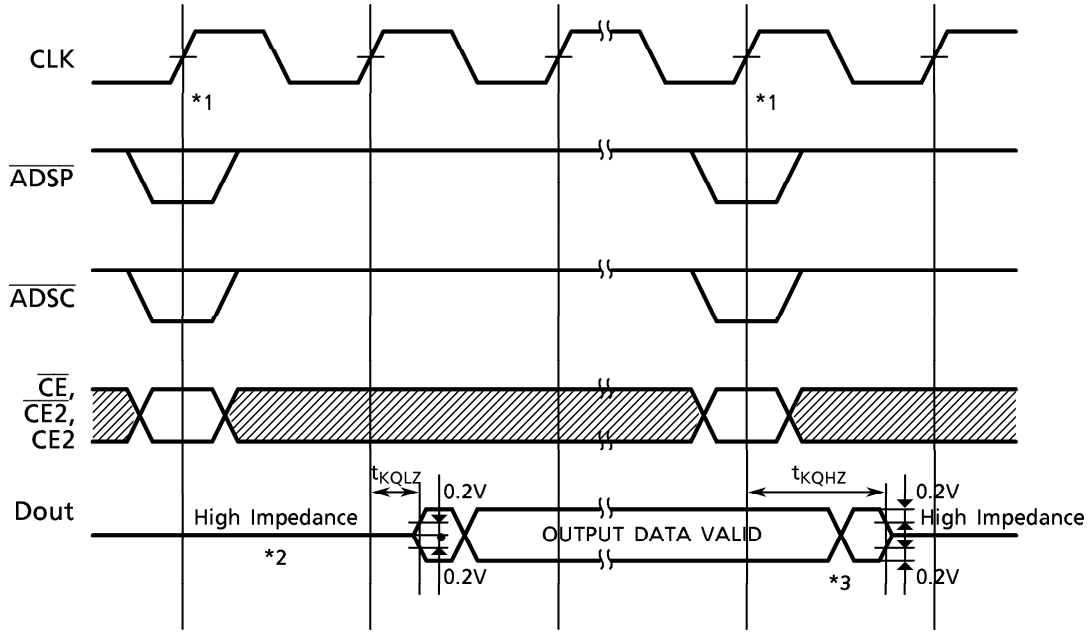
SNOOZE CYCLE (Pipeline)



NOTE : 1. Don't apply opposite phase data to the I/O pins when they are in the output state.

2. Output enable and output disable times are specified as follows with the output load shown in Figure 1.

(a) t_{KQLZ}, t_{KQHZ}

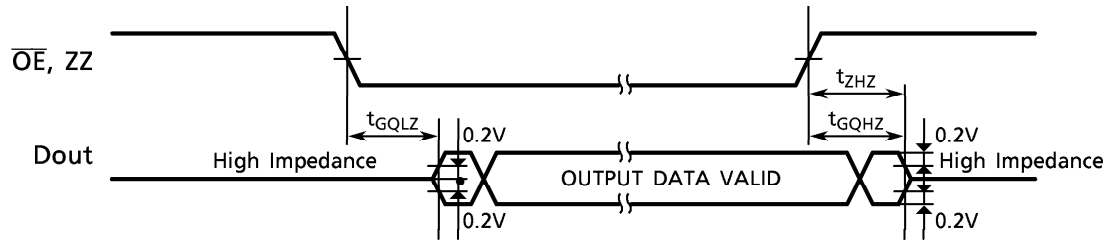


*1 : The input states are defined in the Synchronous Input Truth Table.

*2 : If the device was previously deselected, when the device is selected, the output remains in a high impedance state in the present clock cycle regardless of $\overline{OE}$ because of the output enable delay register. Valid data appears in the second clock cycle when $\overline{OE}$ is low.

*3 : When the device is deselected, the output goes into a high impedance state in the present clock cycle regardless of $\overline{OE}$.

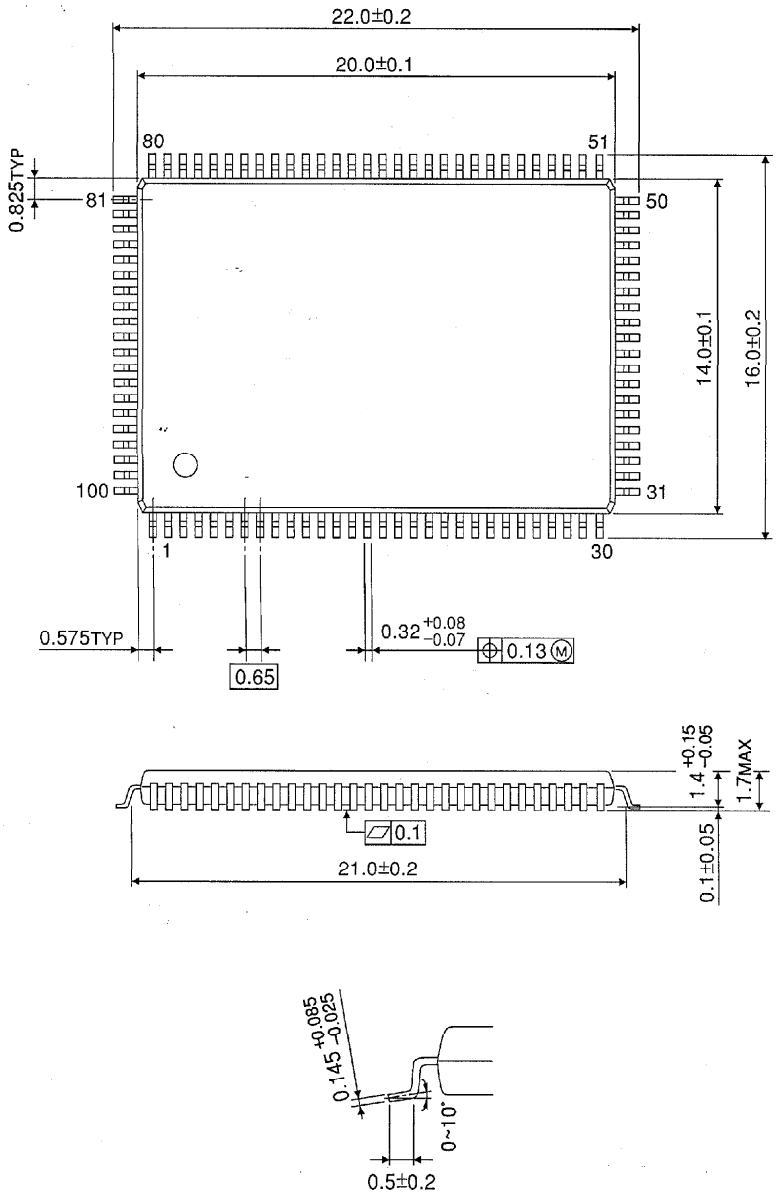
(b) t_{GQLZ}, t_{GQHZ}, t_{ZHZ}



OUTLINE DRAWINGS

Plastic LQFP (LQFP100-P-1420-0.65K)

Unit in mm



Weight : 0.56g (Typ.)