

# TrenchMOS™ transistor Standard level FET

PHT8N06T

## GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting. Using 'trench' technology the device features very low on-state resistance and has integral zener diodes giving ESD protection. It is intended for use in DC-DC converters and general purpose switching applications.

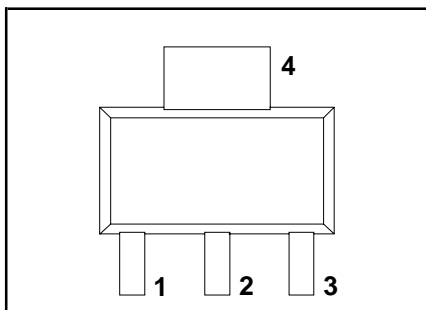
## QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$V_{DS}$	Drain-source voltage	55	V
$I_D$	Drain current	7.5	A
$P_{tot}$	Total power dissipation	1.8	W
$T_j$	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance $V_{GS} = 10\text{ V}$	80	mΩ

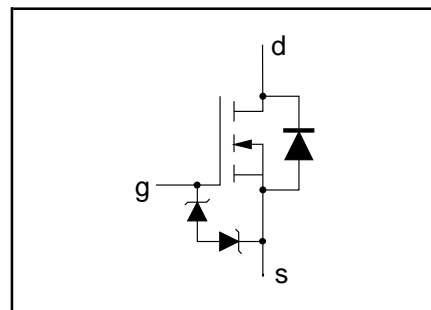
## PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

## PIN CONFIGURATION



## SYMBOL



## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	Drain-source voltage	-	-	55	V
$V_{DGR}$	Drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	20	V
$I_D$	Drain current (DC)	$T_{sp} = 25\text{ }^\circ\text{C}$	-	7.5	A
$I_D$	Drain current (DC)	On PCB in Fig.2 $T_{amb} = 25\text{ }^\circ\text{C}$	-	3.5	A
$I_D$	Drain current (DC)	On PCB in Fig.2 $T_{amb} = 100\text{ }^\circ\text{C}$	-	2.2	A
$I_{DM}$	Drain current (pulse peak value)	$T_{sp} = 25\text{ }^\circ\text{C}$	-	40	A
$P_{tot}$	Total power dissipation	$T_{sp} = 25\text{ }^\circ\text{C}$	-	8.3	W
$P_{tot}$	Total power dissipation	On PCB in Fig.2 $T_{amb} = 25\text{ }^\circ\text{C}$	-	1.8	W
$T_{stg}, T_j$	Storage & operating temperature	-	- 55	150	°C

## ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_C$	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

## TrenchMOS™ transistor Standard level FET

PHT8N06T

### THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-sp}$	From junction to solder point	Mounted on any PCB	12	15	K/W
$R_{th\ j-amb}$	From junction to ambient	Mounted on PCB of Fig.2	-	70	K/W

### STATIC CHARACTERISTICS

 $T_j = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.25\text{ mA}$ $T_j = -55^\circ\text{C}$	55 50	- -	- -	V V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 1\text{ mA}$ $T_j = 150^\circ\text{C}$	2 1.2	3 -	4 -	V V
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = 55\text{ V}; V_{GS} = 0\text{ V};$ $T_j = 150^\circ\text{C}$	-	0.05	10	$\mu\text{A}$
$I_{GSS}$	Gate source leakage current	$V_{GS} = \pm 10\text{ V}$ $T_j = 150^\circ\text{C}$	-	0.04	1	$\mu\text{A}$
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	$I_G = \pm 1\text{ mA};$ $T_j = 150^\circ\text{C}$	-	-	10	$\mu\text{A}$
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 5\text{ A}$ $T_j = 150^\circ\text{C}$	-	65	80	m $\Omega$
			-	-	148	m $\Omega$

### DYNAMIC CHARACTERISTICS

 $T_{mb} = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$g_{fs}$	Forward transconductance	$V_{DS} = 25\text{ V}; I_D = 5\text{ A}; T_j = 25^\circ\text{C}$	1	-	-	S
$Q_{g(tot)}$	Total gate charge	$I_D = 7\text{ A}; V_{DD} = 44\text{ V}; V_{GS} = 10\text{ V}$	-	13.5	-	nC
$Q_{gs}$	Gate-source charge		-	2.5	-	nC
$Q_{gd}$	Gate-drain (Miller) charge		-	5.5	-	nC
$C_{iss}$	Input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$	-	365	500	pF
$C_{oss}$	Output capacitance		-	110	135	pF
$C_{rss}$	Feedback capacitance		-	60	85	pF
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 30\text{ V}; I_D = 7\text{ A};$ $V_{GS} = 10\text{ V}; R_G = 10\ \Omega;$ $T_j = 25^\circ\text{C}$	-	9	14	ns
$t_r$	Turn-on rise time		-	15	25	ns
$t_{d\ off}$	Turn-off delay time		-	18	27	ns
$t_f$	Turn-off fall time		-	12	18	ns

### REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

 $T_j = -55$  to  $175^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{DR}$	Continuous reverse drain current	$T_{sp} = 25^\circ\text{C}$	-	-	7.5	A
$I_{DRM}$	Pulsed reverse drain current	$T_{sp} = 25^\circ\text{C}$	-	-	40	A
$V_{SD}$	Diode forward voltage	$I_F = 5\text{ A}; V_{GS} = 0\text{ V}$	-	0.85	1.1	V
$t_{rr}$	Reverse recovery time	$I_F = 5\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s};$ $V_{GS} = -10\text{ V}; V_R = 30\text{ V}$	-	38	-	ns
$Q_{rr}$	Reverse recovery charge		-	0.2	-	$\mu\text{C}$

---

TrenchMOS™ transistor  
Standard level FET

---

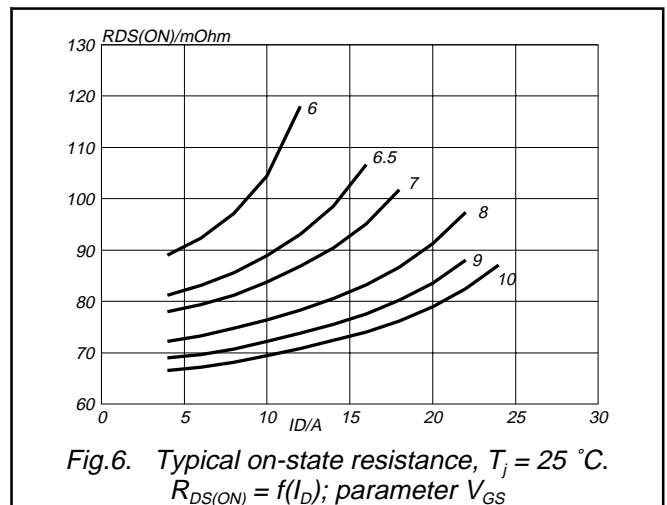
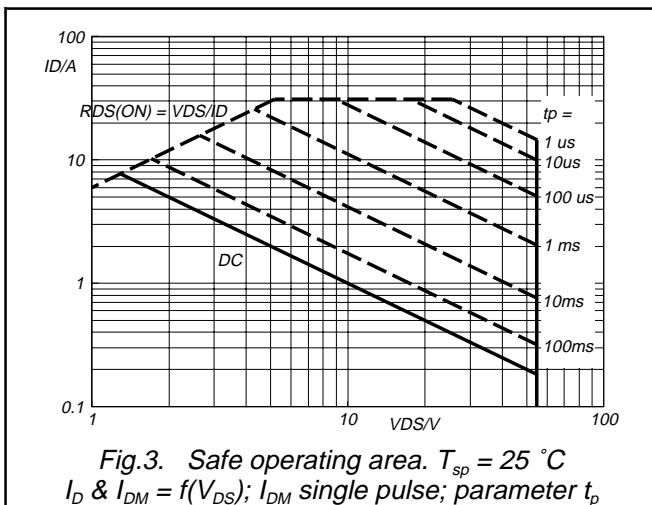
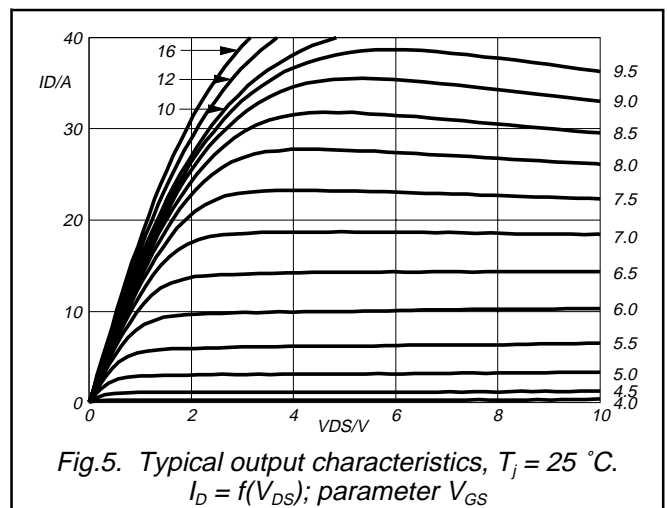
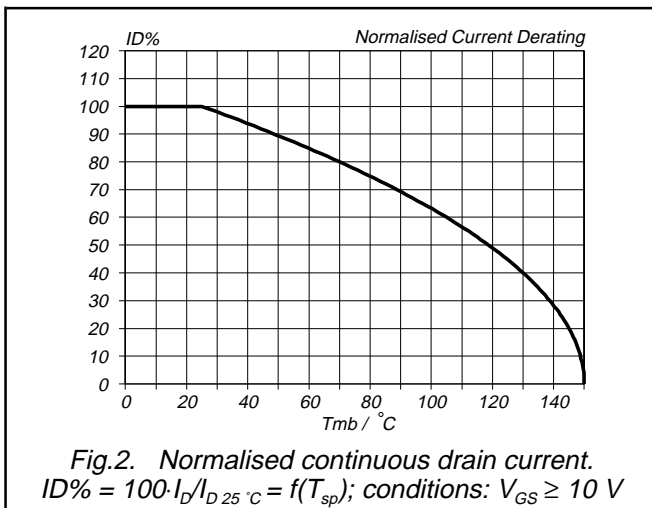
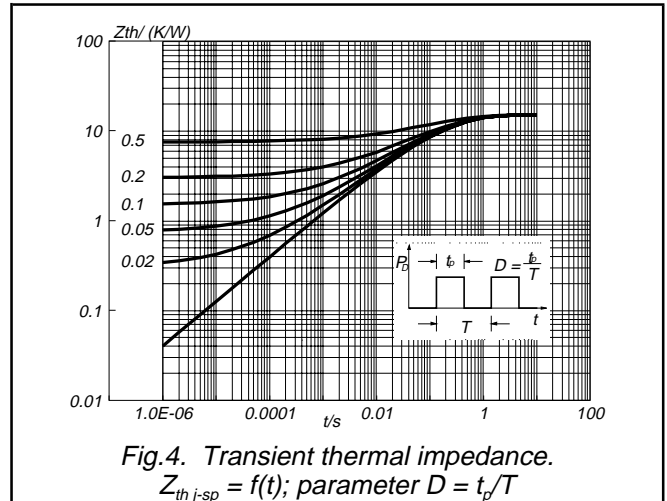
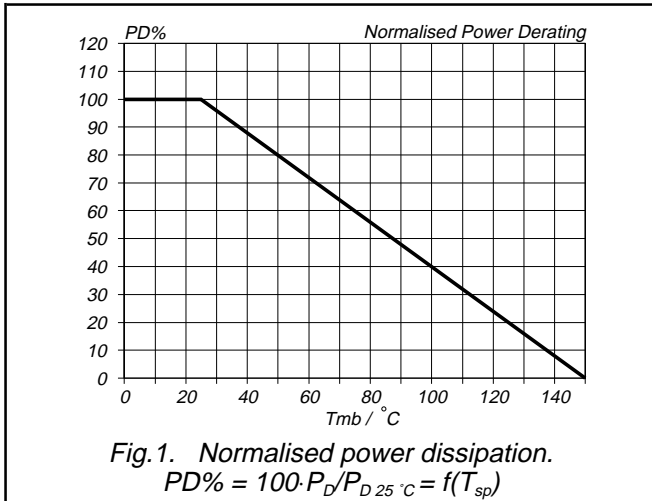
PHT8N06T

**AVALANCHE LIMITING VALUE**

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$W_{DSS}$	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 2.5 \text{ A}$ ; $V_{DD} \leq 25 \text{ V}$ ; $V_{GS} = 10 \text{ V}$ ; $R_{GS} = 50 \text{ } \Omega$ ; $T_{sp} = 25 \text{ } ^\circ\text{C}$	-	-	30	mJ

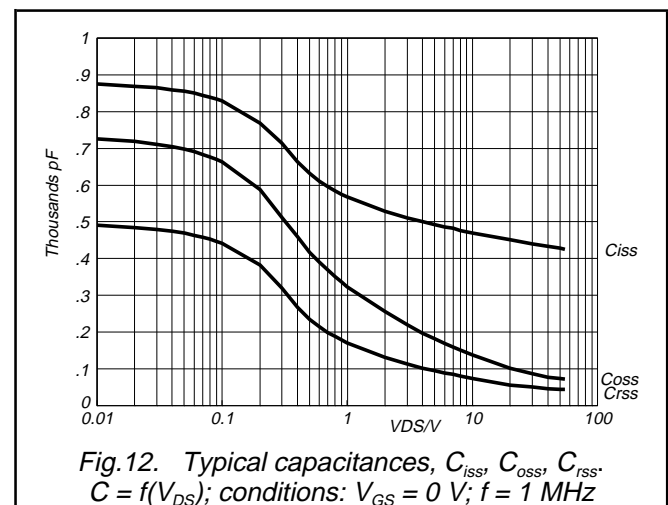
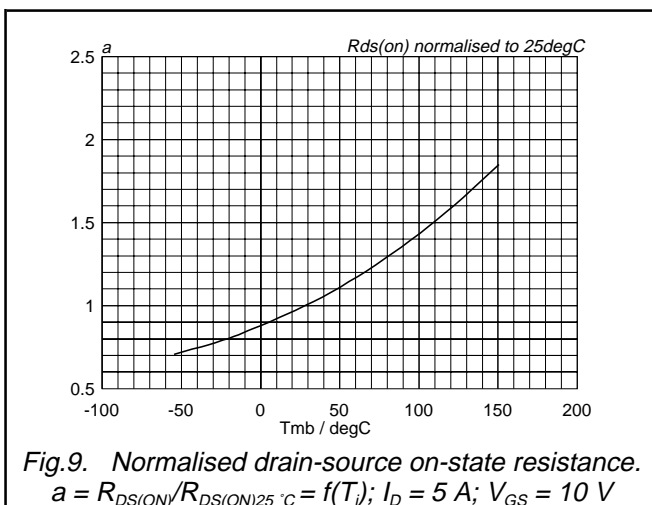
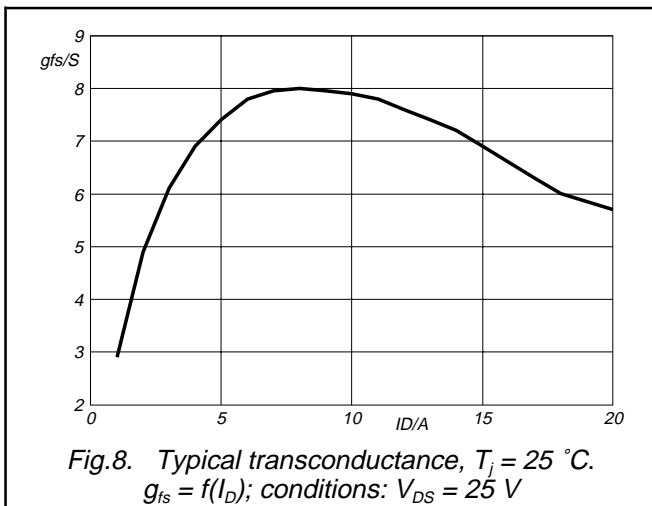
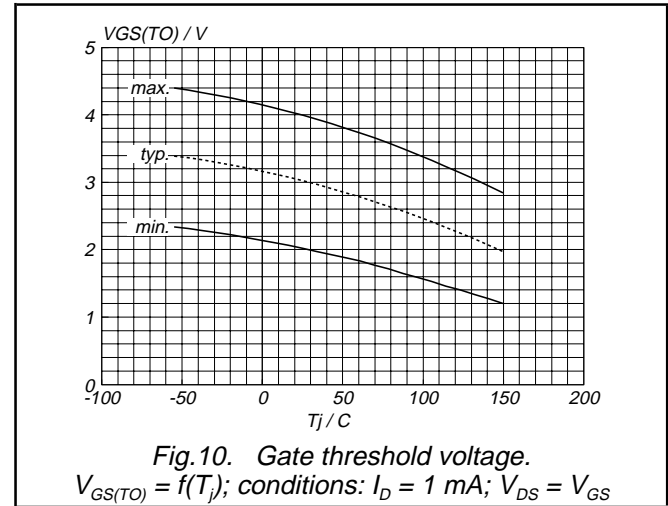
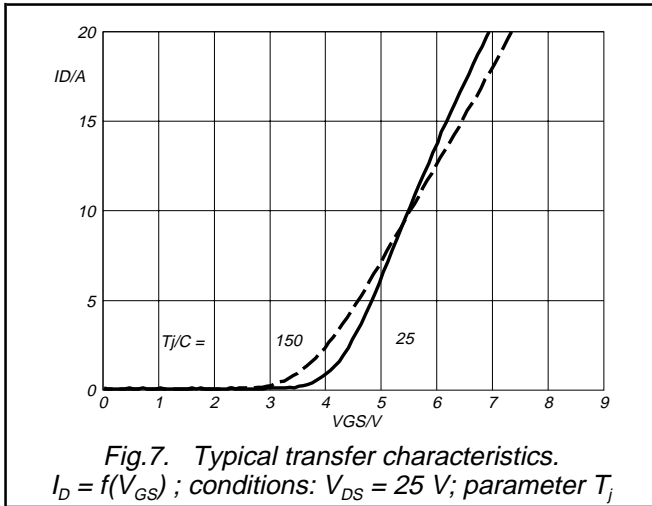
TrenchMOS™ transistor  
Standard level FET

PHT8N06T



TrenchMOS™ transistor  
Standard level FET

PHT8N06T



TrenchMOS™ transistor  
Standard level FET

PHT8N06T

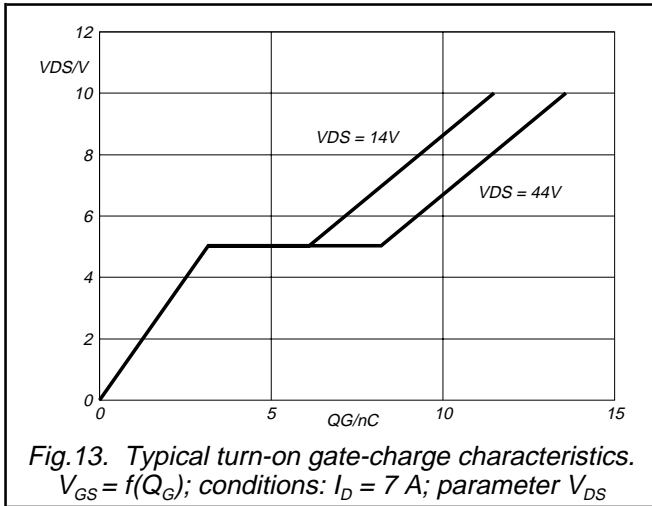


Fig.13. Typical turn-on gate-charge characteristics.  
 $V_{GS} = f(Q_G)$ ; conditions:  $I_D = 7\text{ A}$ ; parameter  $V_{DS}$

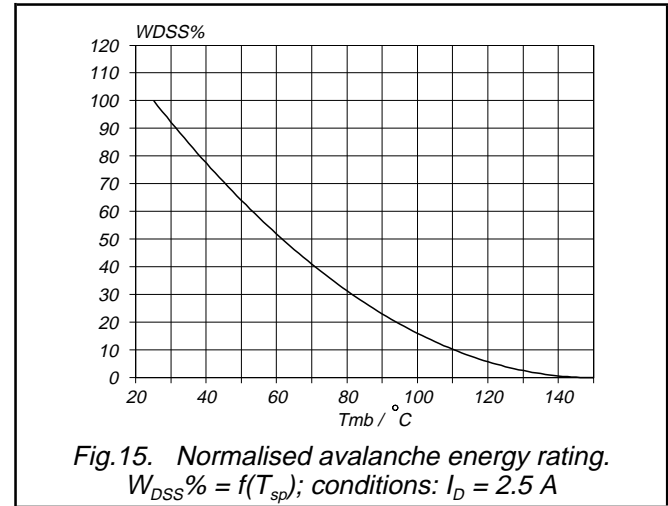


Fig.15. Normalised avalanche energy rating.  
 $W_{DSS}\% = f(T_{sp})$ ; conditions:  $I_D = 2.5\text{ A}$

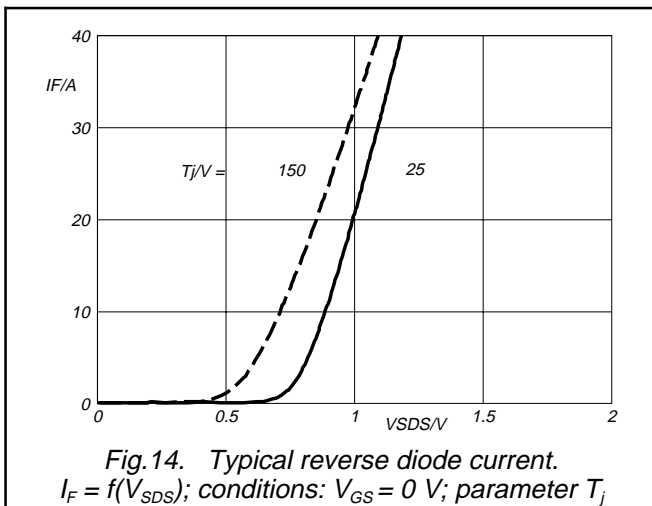


Fig.14. Typical reverse diode current.  
 $I_F = f(V_{SDS})$ ; conditions:  $V_{GS} = 0\text{ V}$ ; parameter  $T_j$

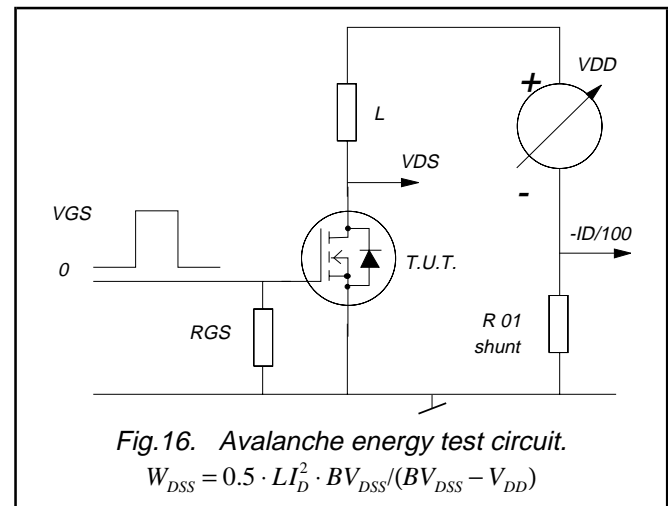


Fig.16. Avalanche energy test circuit.  
 $W_{DSS} = 0.5 \cdot L I_D^2 \cdot BV_{DSS} / (BV_{DSS} - V_{DD})$

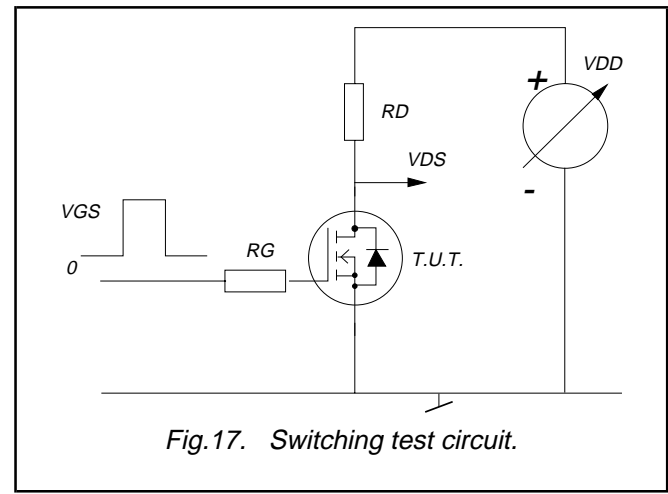
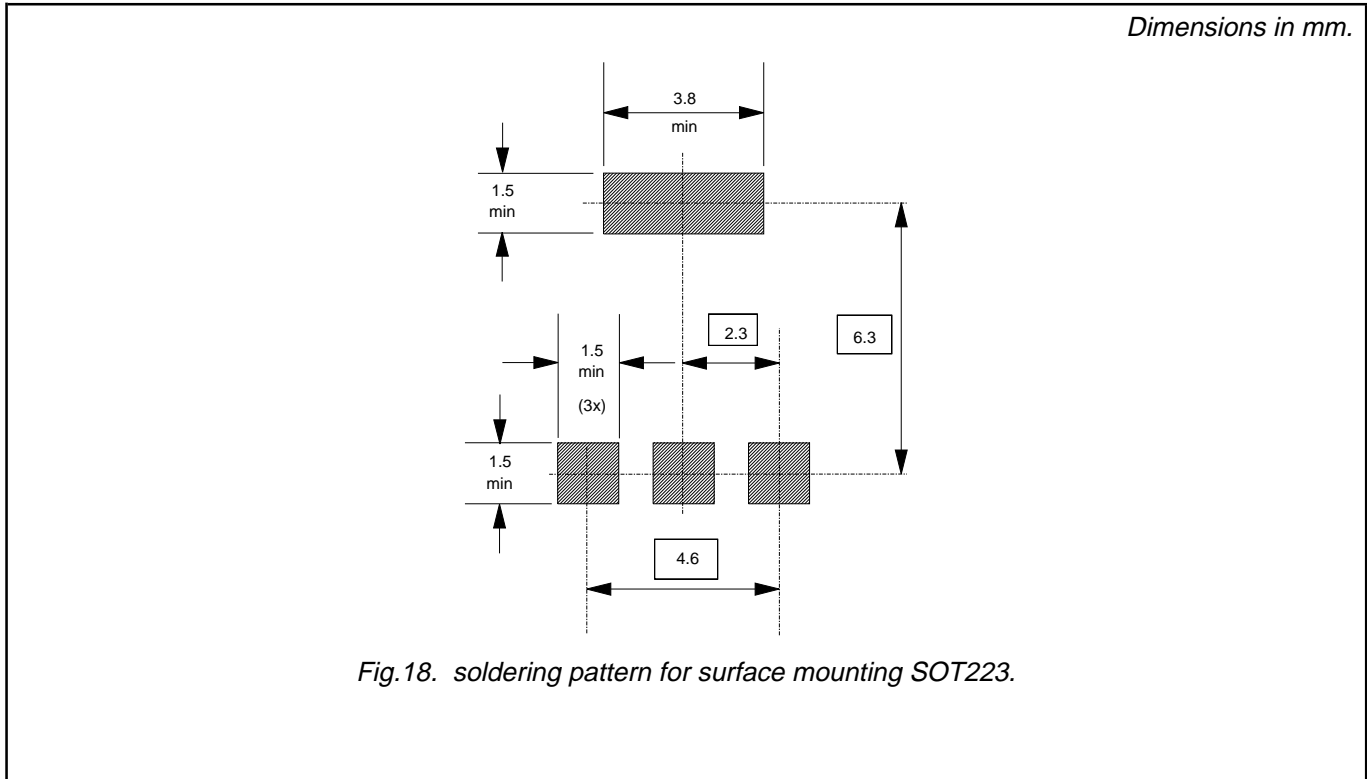


Fig.17. Switching test circuit.

TrenchMOS™ transistor  
Standard level FET

PHT8N06T

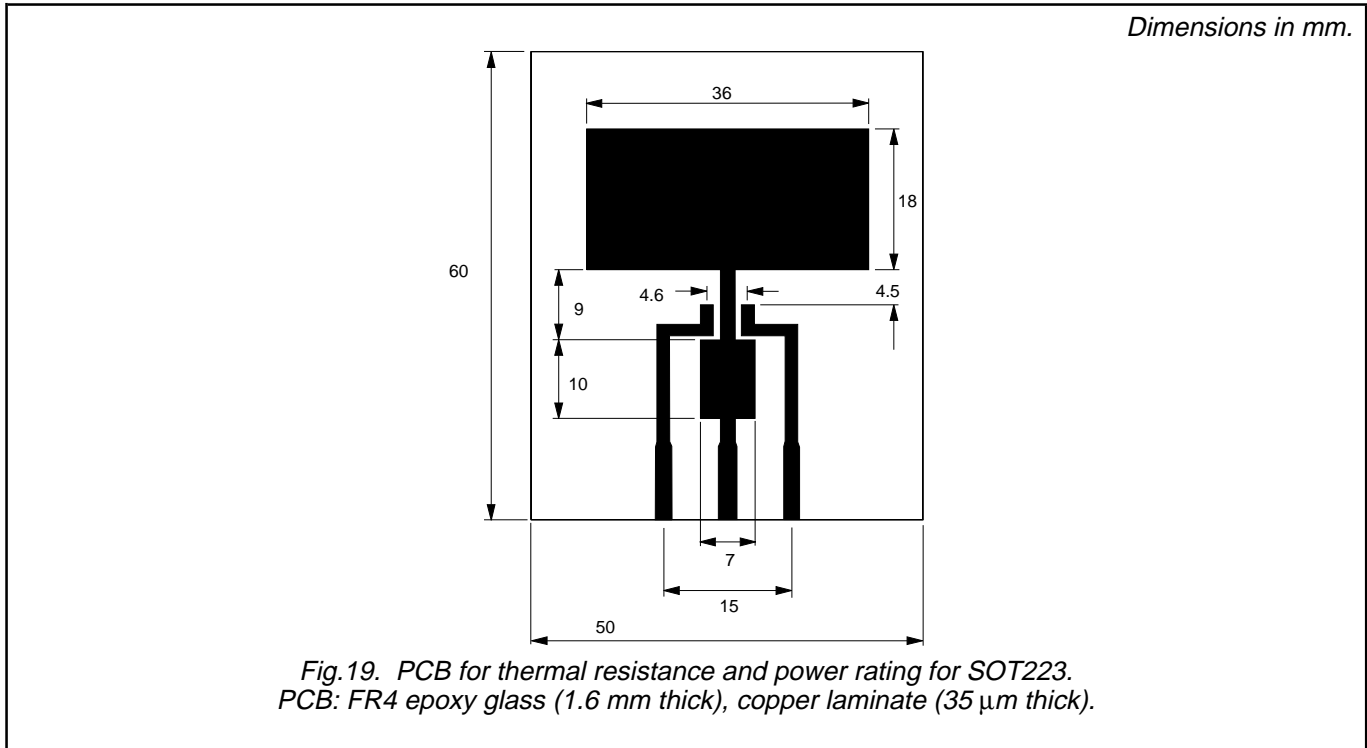
**MOUNTING INSTRUCTIONS**



**PRINTED CIRCUIT BOARD**

TrenchMOS™ transistor  
Standard level FET

PHT8N06T

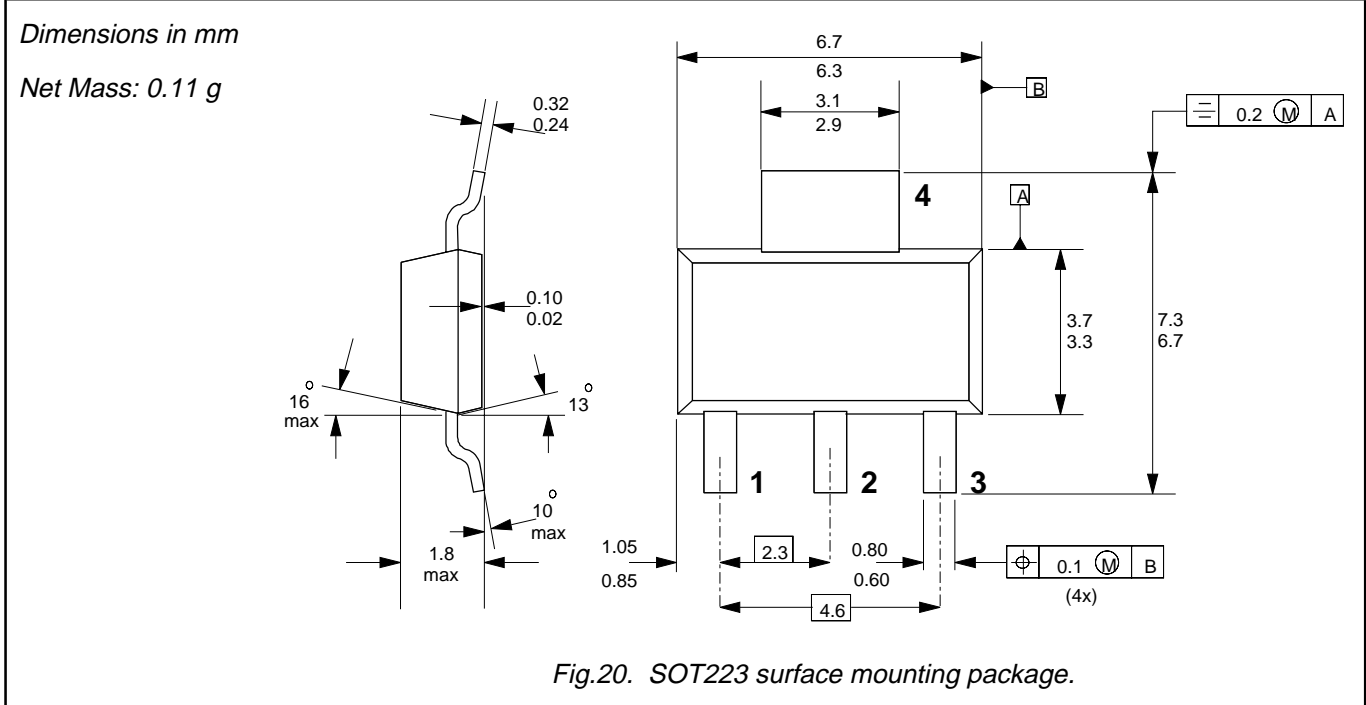




TrenchMOS™ transistor  
Standard level FET

PHT8N06T

**MECHANICAL DATA**



**Notes**

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to surface mounting instructions for SOT223 envelope.
3. Epoxy meets UL94 V0 at 1/8".

## TrenchMOS™ transistor Standard level FET

PHT8N06T

### DEFINITIONS

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	
<b>© Philips Electronics N.V. 1997</b>	
All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.	
The information presented in this document does not form part of any quotation or contract, it is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent or other industrial or intellectual property rights.	

### LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.